OP-07

Low Offset, Low Drift Operational Amplifier

The OP-07 has very low input offset voltage which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current and high open-loop gain. The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain applications.

The wide input voltage range of ±13V minimum combined with high CMRR of 110 dB and high input impedance provide high accuracy in the non-inverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

National Semiconductor

T-79-06-10

OP-07 Low Offset, Low Drift Operational Amplifier

General Description

The OP-07 has very low input offset voltage which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current and high open-loop gain. The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain applications.

The wide input voltage range of ±13V minimum combined with high CMRR of 110 dB and high input impedance provide high accuracy in the non-inverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variation in temperature is excellent.

The OP-07 is available in TO-99 metal can, ceramic or molded DIP.

For improved specifications, see the LM607.

Features

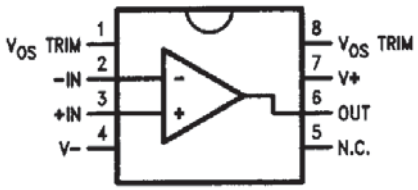
- Low V_{OS} — 75 μV Max
- Low V_{OS} Drift — 0.6 μV/°C Max
- Ultra-Stable vs Time — 1.0 μV/Month Max
- Low Noise — 0.6 μVp-p Max
- Wide Input Voltage Range — ±14V
- Wide Supply Voltage Range — ±3V to ±18V
- Fits 725/108A/308A, 741, AD510 Sockets
- Replaces the μA714

Applications

- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- Precision Reference Buffer
- Analog Computing Functions

Connection Diagrams

Dual-In-Line Package



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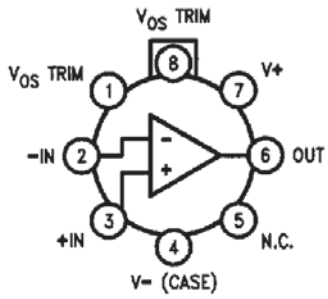
See NS Package Number J08A or N08E

Metal Can Package



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See NS Package Number H08C

Ordering Information

T_A = 25°C V_{OS}Max (μV)	H08C TO-99	Package J08A CERDIP	N08E Plastic	Operating Temperature Range
75	OP07EJ	OP07EZ	OP07EP	COM
75	OP07J*	OP07Z		MIL
150	OP07CJ	OP07CZ	OP07CP	COM
150	OP07DJ		OP07DP	COM

*Also available per SMD #8203602

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Internal Power Dissipation (Note 5)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 6)	±22V
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
J and Z Packages	−65°C to +150°C
P Package	−65°C to +125°C
Lead Temperature (Soldering, 60 sec.)	260°C
Junction Temperature	−65°C to +150°C

Operating Temperature Range

OP-07	−55°C to +125°C
OP-07E, OP-07C, OP-07D	0°C to +70°C

Electrical Characteristics

Unless otherwise specified, V_S = ±15V, T_A = 25°C. **Boldface** type refers to limits over −55°C ≤ T_A ≤ +125°C

Symbol	Parameter	Conditions	OP-07			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1) (Note 1)		30 **60**	75 **200**	µV
$\Delta V_{OS/t}$	Long-Term Input Offset Voltage Stability	(Note 2)		0.2	1.0	µV/Mo
I_{OS}	Input Offset Current			0.4 **1.2**	2.8 **5.6**	nA
I_B	Input Bias Current			±1.0 ±**2**	±3.0 ±**6**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6	μV_{p-p}
e_n	Input Noise Voltage Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30	pA_{p-p}
i_n	Input Noise Current Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance Differential-Mode	(Note 4)	20	60		MΩ
R_{INCM}	Input Resistance Common-Mode			200		GΩ
IVR	Input Voltage Range		±13.0 ±**13.0**	±14.0 ±**13.5**		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13V	110 **106**	126 **123**		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V		4 **5**	10 **20**	µV/V
A_{VO}	Large-Signal Voltage Gain	R_L ≥ 2 kΩ, V_O = ±10V R_L ≥ 2 kΩ, V_O = ±10V R_L ≥ 500Ω, V_O = ±0.5V, V_S = ±3V (Note 4)	200 **150** 150	500 **400** 400		V/mV
V_O	Output Voltage Swing	R_L ≥ 10 kΩ R_L ≥ 2 kΩ R_L ≥ 2 kΩ R_L ≥ 1 kΩ	±12.5 ±12.0 ±**12.0** ±10.5	±13.0 ±12.8 ±**12.6** ±12.0		V

Electrical Characteristics (Continued)

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $-55°C \le T_A \le +125°C$

Symbol	Parameter	Conditions	OP-07			Units
			Min	Typ	Max	
SR	Slew Rate	$R_L \ge 2\,k\Omega$ (Note 3)	0.1	0.3		V/μs
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		MHz
R_O	Open-Loop Output Resistance	$V_O = 0$, $I_O = 0$		60		Ω
P_d	Power Consumption	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load		75 4	120 6	mW
	Offset Adj. Range	$R_P = 20\,k\Omega$		±4		mV
TCV_{OS}	Average Input Offset Voltage Drift Without External Trim	(Note 3)		**0.3**	**1.3**	μV/°C
TCV_{OSn}	With External Trim	$R_P = 20\,k\Omega$ (Note 4)		**0.3**	**1.3**	
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**8**	**50**	pA/°C
TCI_B	Average Input Bias Drift	(Note 3)		**13**	**50**	pA/°C

Note 1: V_{OS} is measured approximately 0.5 second after application of power.

Note 2: Long-Term Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV. Parameter is sample tested.

Note 3: Sample tested.

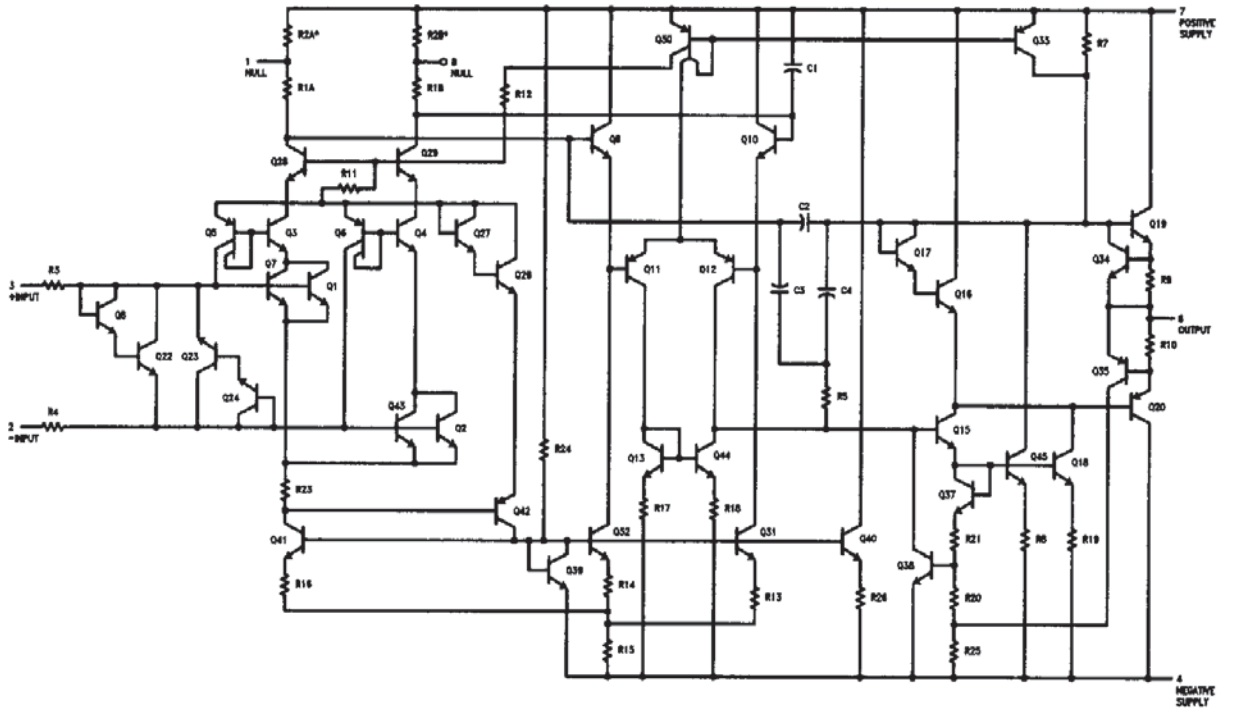
Note 4: Guaranteed by design.

Note 5: The typical θ_{JA} of the H08 (TO-99) package is 155°C/W, the J08 (CERDIP) package is 92° C/W and the N08 (Molded DIP) is 100° C/W. The typical θ_{JC} of the H08 package is 17.5° C/W. All numbers apply for packages soldered directly into an etched circuit board.

Note 6: For supply voltages of less than ±22V, the maximum input voltage is 0.5V beyond either supply.

Note 7: See RETSOPO7X for the OP07H military specifications.

Simplified Schematic



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*R2A and R2B are electronically trimmed on chip at the factory for minimum offset voltage.

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $0°C \le T_A \le 70°C$

Symbol	Parameter	Conditions	OP-07E			OP-07C			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1)		30 **45**	75 **130**		60 **85**	150 **250**	μV
$V_{OS/t}$	Long-Term V_{OS} Stability	(Note 2)		0.3	1.5		0.4	2.0	μV/Mo
I_{OS}	Input Offset Current			0.5 **0.9**	3.8 **5.3**		0.8 **1.6**	6.0 **8.0**	nA
I_B	Input Bias Current			±1.2 **±1.5**	±4.0 **±5.5**		±1.8 **±2.2**	±7.0 **±9.0**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6		0.38	0.65	μV_{p-p}
e_n	Input Noise Voltage Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30		15	35	pA_{p-p}
i_n	Input Noise Current Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance Differential-Mode	(Note 4)	15	50		8	33		MΩ
R_{INCM}	Input Resistance Common-Mode			160			120		GΩ
IVR	Input Voltage Range		±13.0	±14.0		±13	±14		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13V	106 **103**	123 **123**		100 **97**	120 **120**		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V V_S = ±3V to ±18V		5 **7**	20 **32**		7 **10**	32 **51**	μV/V
A_{VO}	Large Signal Voltage Gain	$R_L \ge 2 k\Omega$, V_O = ±10V $R_L \ge 2 k\Omega$ $R_L \ge 500\Omega$, V_O = ±0.5V, V_S = ±3V (Note 4)	200 **180** 150	500 **450** 400		120 **100** 100	400 **400** 400		V/mV
V_O	Output Voltage Swing	$R_L \ge 10 k\Omega$ $R_L \ge 2 k\Omega$ $R_L \ge 2 k\Omega$ $R_L \ge 1 k\Omega$	±12.5 ±12.0 **±12.0** ±10.5	±13.0 ±12.8 **±12.6** ±12.0		±12.0 ±11.5 **±11.0**	±13.0 ±12.8 **±12.6** ±12.0		V
SR	Slew Rate	$R_L \ge 2 k\Omega$ (Note 3)	0.1	0.3		0.1	0.3		V/μs
BW	Closed-Loop Bandwidth	A_{VCL} = +1 (Note 3)	0.4	0.6		0.4	0.6		MHz
R_O	Output Resistance	V_O = 0, I_O = 0		60			60		Ω
P_d	Power Consumption	V_S = ±15V, No Load V_S = ±3V, No Load		75 4	120 6		80 4	150 8	mW
	Offset Adj. Range	R_P = 20 kΩ		±4			±4		mV
TCV_{OS} TCV_{OSn}	Average Input Offset Voltage Drift Without External Trim With External Trim	(Note 4) R_P = 20 kΩ (Note 4)		**0.3** **0.3**	**1.3** **1.3**		**0.5** **0.4**	**1.8** **1.6**	μV/°C
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**8**	**35**		**12**	**50**	pA/°C
TCI_B	Average Input Bias Current Drift	(Note 3)		**13**	**35**		**18**	**50**	pA/°C

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $0°C \le T_A \le +70°C$

Symbol	Parameter	Conditions	OP-07D			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1)		60 **85**	150 **250**	µV
$V_{OS/t}$	Long-Term V_{OS} Stability	(Note 2)		0.5	3.0	µV/Mo
I_{OS}	Input Offset Current			0.8 **1.6**	6.0 **8.0**	nA
I_B	Input Bias Current			±2.0 **±3.0**	±12.0 **±14.0**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.38	0.65	µVp-p
e_n	Input Noise Voltage Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		10.5 10.3 9.8	20.0 13.5 11.5	nV/√Hz
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		15	35	pAp-p
i_n	Input Noise Current Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		0.35 0.15 0.13	0.90 0.27 0.18	pA/√Hz
R_{IN}	Input Resistance Differential-Mode	(Note 4)	7	31		MΩ
R_{INCM}	Input Resistance Common-Mode			120		GΩ
IVR	Input Voltage Range		±13	±14		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13V	94 **94**	110 **106**		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V		7 **10**	32 **51**	µV/V
A_{VO}	Large Signal Voltage Gain	$R_L \le 2$ kΩ, V_O = ±10V R_L = 2 kΩ, V_O = ±10V $R_L \ge 500Ω$, V_O = ±0.5V, V_S ±3V (Note 4)	120 **100**	400 **400** 400		V/mV
V_O	Output Voltage Swing	$R_L \ge 10$ kΩ $R_L \ge 2$ kΩ $R_L \ge 2$ kΩ $R_L \ge 1$ kΩ	±12.0 ±11.5 **±11.0**	±13.0 ±12.8 **±12.6** ±12.0		V
SR	Slew Rate	$R_L \ge 2$ kΩ (Note 3)	0.1	0.3		V/µs
BW	Closed-Loop Bandwidth	A_{VCL} = +1 (Note 3)	0.4	0.6		MHz
RO	Output Resistance	V_O = 0, I_O = 0		60		Ω
P_d	Power Consumption	V_S = ±15V, No Load V_S = ±3V, No Load		80 4	150 8	mW
	Offset Adj. Range	R_P = 20 kΩ		±4		mV
TCV_{OS}	Average Input Offset Voltage Drift Without External Trim	(Note 4)		**0.7**	**2.5**	µV/°C
TCV_{OSn}	With External Trim	R_P = 20 kΩ (Note 4)		**0.7**	**2.5**	µV/°C
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**12**	**50**	pA/°C
TCI_B	Average Input Bias Current Drift	(Note 3)		**18**	**50**	pA/°C

Note 1: V_{OS} is measured approximately 0.5 second after application of power.

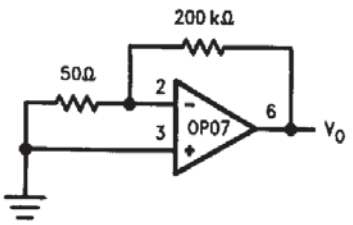
Note 2: Long-Term Offset Voltage Stability refers to the averaged trend line of V_{OS} vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV. Parameter is sample tested.

Note 3: Sample Tested.

Note 4: Guaranteed by design.

Test Circuits

Offset Voltage Test Circuit



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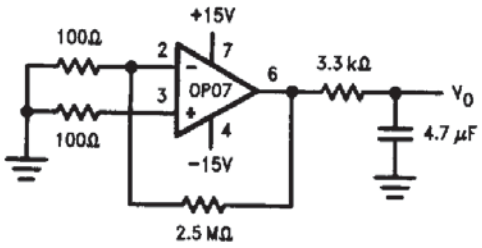
Low Frequency Noise Test Circuit



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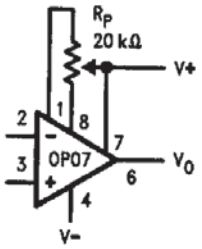
Optional Offset Nulling Circuit



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