

PIC16F688 Data Sheet

14-Pin Flash-Based, 8-Bit CMOS Microcontrollers with

Electrónica S.A. ae

www.agelectronica.com

© 2004 Microchip Technology Inc.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.



Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart and rfPIC are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

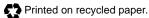
AmpLab, FilterLab, microID, MXDEV, MXLAB, PICMASTER, SEEVAL, SmartShunt and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Application Maestro, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICkit, PICDEM, PICDEM.net, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, rfLAB, Select Mode, SmartSensor, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2004, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.



QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV SO/TS 16949:2002 Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

DS41203B-page ii

Preliminary



14-Pin Flash-Based, 8-Bit CMOS Microcontrollers with nanoWatt Technology

High-Performance RISC CPU

- Only 35 instructions to learn:
 - All single-cycle instructions except branches
- Operating speed:
 - DC 20 MHz oscillator/clock input
 - DC 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features

- Precision Internal Oscillator:
 - Factory calibrated to ±1%
 - Software selectable frequency range of 8 MHz to 31 kHz
 - Software tunable
 - Two-Speed Start-up mode
 - Crystal fail detect for critical applications
 - Clock mode switching during operation for power savings
- Power saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and Extended temperature range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Detect (BOD) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection
- High-Endurance Flash/EEPROM cell:
 - 100,000 write Flash endurance
 - 1,000,000 write EEPROM endurance
 - Flash/Data EEPROM retention: > 40 years

Low-Power Features

- Standby Current:
 - 1 nA @ 2.0V, typical
- Operating Current:
 - 8.5 μA @ 32 kHz, 2.0V, typical
 - 100 μA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current:
 - 1 μA @ 2.0V, typical

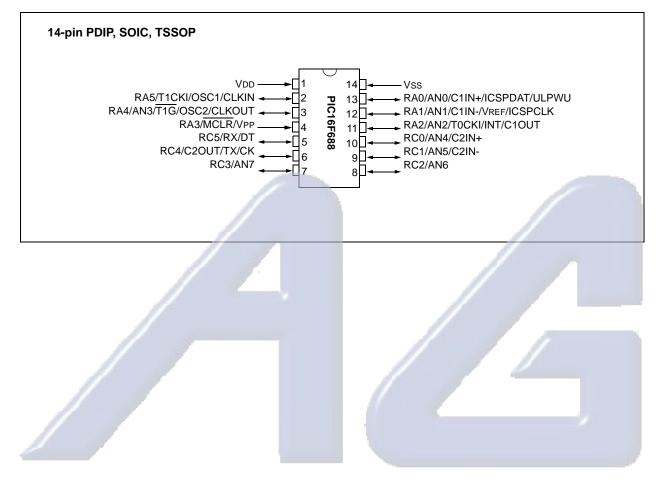
Peripheral Features

- 12 I/O pins with individual direction control:
 - High-current source/sink for direct LED drive
 - Interrupt-on-pin change
 - Individually programmable weak pull-ups
 - Ultra Low-Power Wake-up
- Analog comparator module with:
 - Two analog comparators
 - Programmable on-chip voltage reference (CVREF) module (% of VDD)
 - Comparator inputs and outputs externally accessible
- A/D Converter:
 - 10-bit resolution and 8 channels
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
- 16-bit timer/counter with prescaler
- External Gate Input mode
- Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
- Enhanced USART Module:
 - Supports RS-485, RS-232, and LIN 1.2
 - Auto baud detect
 - Auto-wake-up on Start bit
- In-Circuit Serial Programming[™] (ICSP[™]) via two pins

Device	Program Memory	Data M	lemory	I/O	10-bit A/D	Comparators	Timers 8/16-bit	
Device	Flash (words)	SRAM (bytes)	EEPROM (bytes)	20	(ch)	Comparators		
PIC16F688	4096	256 256		12	8	2	1/1	

© 2004 Microchip Technology Inc.

Pin Diagram



Electrónica S.A. de C.V.

DS41203B-page 2

© 2004 Microchip Technology Inc.

Table of Contents

1.0	Device Overview	5
2.0	Memory Organization	7
3.0	Clock Sources	
4.0	I/O Ports	. 31
5.0	Timer0 Module	
6.0	Timer1 Module with Gate Control	. 49
7.0	Comparator Module	. 53
8.0	Analog-to-Digital Converter (A/D) Module	. 63
9.0	Data EEPROM and Flash Program Memory Control	. 71
10.0	Enhanced Universal Asynchronous Receiver Transmitter (EUSART)	. 77
11.0	Special Features of the CPU	. 99
12.0	Instruction Set Summary	119
13.0	Development Support	129
14.0	Electrical Specifications	
15.0	DC and AC Characteristics Graphs and Tables	157
16.0	Packaging Information	159
	ndix A: Data Sheet Revision History	163
Appe	ndix B: Migrating from other PICmicro® Devices	163
Index	<	
On-li	ne Support	169
Syste	ems Information and Upgrade Hot Line	169
Read	ler Response	170
Prod	uct Identification System	171

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at docerrors@mail.microchip.com or fax the Reader Response Form in the back of this data sheet to (480) 792-4150. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

• The Microchip Corporate Literature Center; U.S. FAX: (480) 792-7277

When contacting a sales office or the literature center, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at www.microchip.com/cn to receive the most current information on all of our products.

^{© 2004} Microchip Technology Inc.

www.agelectronica.com

PIC16F688

NOTES:



Electrónica S.A. de C.V.

DS41203B-page 4

Preliminary

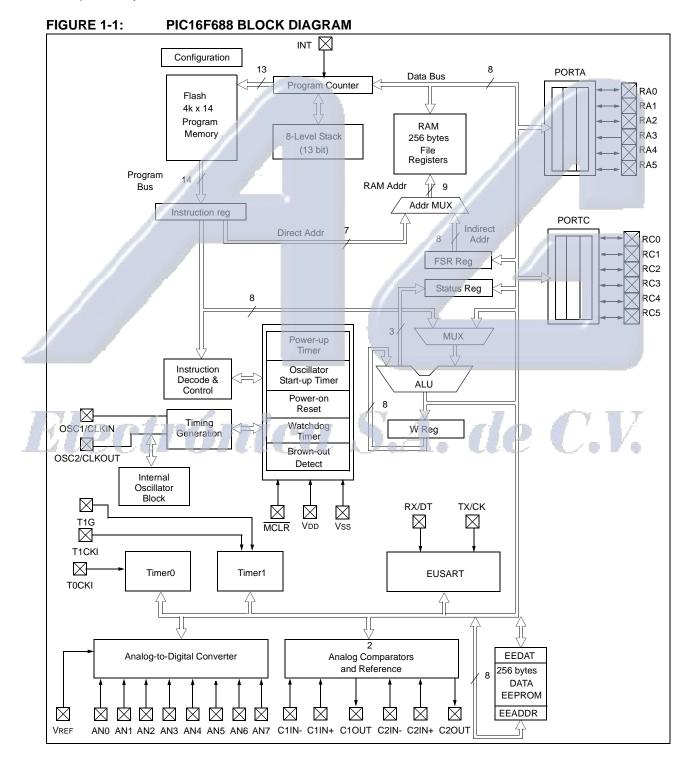
© 2004 Microchip Technology Inc.

www.agelectronica.com

1.0 DEVICE OVERVIEW

This document contains device specific information for the PIC16F688. Additional information may be found in the "*PICmicro*[®] *Mid-Range MCU Family Reference Manual*" (DS33023), downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this data sheet and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC16F688 is covered by this data sheet. It is available in 14-pin PDIP, SOIC and TSSOP packages. Figure 1-1 shows a block diagram of the PIC16F688 device. Table 1-1 shows the pinout description.



© 2004 Microchip Technology Inc.

www.agelectronica.com PIC16F688

TABLE 1-1: PIC16F688 PINOUT DESCRIPTIO
--

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/ICSPDAT/ULPWU	RA0	TTL	CMOS	PORTA I/O w/prog pull-up and interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	C1IN+	AN	—	Comparator 1 input
	ICSPDAT	TTL	CMOS	Serial Programming Data I/O
	ULPWU	AN	_	Ultra Low-Power Wake-up input
RA1/AN1/C1IN-/VREF/ICSPCLK	RA1	TTL	CMOS	PORTA I/O w/prog pull-up and interrupt-on-change
	AN1	AN	_	A/D Channel 1 input
	C1IN-	AN	_	Comparator 1 input
	VREF	AN		External Voltage Reference for A/D
	ICSPCLK	ST	-	Serial Programming Clock
RA2/AN2/T0CKI/INT/C1OUT	RA2	ST	CMOS	PORTA I/O w/prog pull-up and interrupt-on-change
	AN2	AN	_	A/D Channel 2 input
	TOCKI	ST		Timer0 clock input
	INT	ST		External Interrupt
	C1OUT		CMOS	Comparator 1 output
RA3/MCLR/Vpp	RA3	TTL	_	PORTA input with interrupt-on-change
	MCLR	ST		Master Clear w/internal pull-up
	VPP	HV		Programming voltage
RA4/AN3/T1G/OSC2/CLKOUT	RA4	TTL	CMOS	PORTA I/O w/prog pull-up and interrupt-on-change
	AN3	AN	_	A/D Channel 3 input
	T1G	ST		Timer1 gate
	OSC2	51	XTAL	Crystal/Resonator
	CLKOUT		CMOS	Fosc/4 output
RA5/T1CKI/OSC1/CLKIN				
KAS/TTOKI/OSOT/CERIN	RA5	TTL	CMOS	PORTA I/O w/prog pull-up and interrupt-on-change
	T1CKI	ST		Timer1 clock
	OSC1	XTAL		Crystal/Resonator
	CLKIN	ST		External clock input/RC oscillator connection
RC0/AN4/C2IN+	RC0	TTL	CMOS	PORTC I/O
manifer and	AN4	AN		A/D Channel 4 input
	C2IN+	AN		Comparator 2 input
RC1/AN5/C2IN-	RC1	TTL	CMOS	PORTC I/O
	AN5	AN		A/D Channel 5 input
	C2IN-	AN		Comparator 2 input
RC2/AN6	RC2	TTL	CMOS	PORTC I/O
	AN6	AN		A/D Channel 6 input
RC3/AN7	RC3	TTL	CMOS	PORTC I/O
	AN7	AN	_	A/D Channel 7 input
RC4/C2OUT/TX/CK	RC4	ST	CMOS	PORTC I/O
	C2OUT	—	CMOS	Comparator 2 output
	TX		CMOS	USART asynchronous output
	СК	ST	CMOS	USART asynchronous clock
RC5/RX/DT	RC5	ST	CMOS	Port C I/O
	RX	ST	CMOS	USART asynchronous input
	DT	ST	CMOS	USART asynchronous data
Vss	Vss	Power	—	Ground reference
Vdd	Vdd	Power		Positive supply

TTL = TTL compatible input

= Schmitt Trigger input with CMOS levels

HV = High Voltage

ST XTAL = Crystal

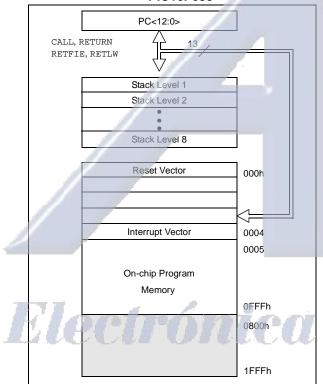
DS41203B-page 6

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16F688 has a 13-bit program counter capable of addressing a 4k x 14 program memory space. Only the first 4k x 14 (0000h-01FFF) for the PIC16F688 is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 4k x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).





2.2 Data Memory Organization

The data memory is partitioned into multiple banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). Bits RP0 and RP1 are bank select bits.

RP0	RP1	(Status<6:5>)
= 00:-	\rightarrow Bank C	1
= 01:-	→ Bank 1	
= 10:-	\rightarrow Bank 2	2
= 11:-	→ Bank 3	6

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are the General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank are mirrored in another bank for code reduction and quicker access.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 256 x 8 in the PIC16F688. Each register is accessed, either directly or indirectly, through the File Select Register (FSR) (see Section 2.4 "Indirect Addressing, INDF and FSR Registers").

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Tables 2-1, 2-2, 2-3 and 2-4). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

 $[\]ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

www.agelectronica.com PIC16F688

	File		File		File		File
	Address		Address		Address		Address
ndirect addr. ⁽¹⁾	00h	Indirect addr. (1)	80h	Indirect addr. (1)	100h	Indirect addr. (1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	PORTA	105h	TRISA	185h
	06h		86h		106h		186h
PORTC	07h	TRISC	87h	PORTC	107h	TRISC	187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
	0Dh		8Dh		10Dh	1 /	18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh		10Fh		18Fh
T1CON	10h	OSCTUNE	90h		110h		190h
BAUDCTL	11h	ANSEL	91h		111h	1	191h
SPBRGH	12h		92h		112h		192h
SPBRG	13h		93h		113h		193h
RCREG	14h		94h		114h		194h
TXREG	15h	WPUA	95h		115h		195h
TXSTA	16h	IOCA	96h		116h		196h
RCSTA	17h	EEDATH	97h		117h		197h
WDTCON	18h	EEADRH	98h		118h		198h
CMCON0	19h	VRCON	99h		119h		199h
CMCON1	1Ah	EEDAT	9Ah		11Ah		19Ah
	1Bh	EEADR	9Bh	10 M	11Bh		19Bh
1 1000	1Ch	EECON1	9Ch		11Ch 🥖	an a	19Ch
2 CC C	1Dh	EECON2 ⁽¹⁾	9Dh	K) al 1	11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
		General		General			
General		Purpose		Purpose			
Purpose Register		Register		Register			
ILEGISIEI		80 Bytes		80 Bytes			
96 Bytes		23 2,00	EFh	23 2,000			
-		accesses	F0h	accesses		accesses	
	7Fh	Bank 0	FFh	Bank 0	17Fh	Bank 0	1FFh
Bank 0		Bank1	1	Bank2		Bank3	
Daint		Baria		Baime		Darino	
	mented da	ta memory locatio	ns, read as	s'0'.			
-	physical re	-	,				

PIC16E688 SPECIAL FUNCTION REGISTERS FIGURE 2-2.

DS41203B-page 8

© 2004 Microchip Technology Inc.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOD Reset	Value on all other Resets ⁽¹⁾
Bank 0	•						•				
00h	INDF	Addressing	g this locatio	on uses conte	ents of FSR to	o address da	ta memory ((not a physic	al register)	xxxx xxxx	XXXX XXXX
01h	TMR0	Timer0 Mo	dule's regis	ter						xxxx xxxx	uuuu uuuu
02h	PCL	Program C	Counter's (P	C) Least Sig	nificant Byte					0000 0000	0000 0000
03h	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h	FSR	Indirect Da	ata Memory	XXXX XXXX	uuuu uuuu						
05h	PORTA	_	_	RA5	RA4	RA3	RA2	RA1	RA0	xx xx00	uu uuuu
06h	_	Unimplem	ented							—	_
07h	PORTC	_	_	RC5	RC4	RC3	RC2	RC1	RC0	xx xx00	uu uuuu
08h	—	Unimplem	ented							1	_
09h	_	Unimplem	ented	11						// -	—
0Ah	PCLATH	_	-	/ -	Write Buffer	for upper 5	bits of Progr	ram Counter		0 0000	0 0 <mark>000</mark>
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	T0IF	INTF	RAIF ⁽²⁾	0000 0000	0000 0000
0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000 0000	0000 0 <mark>000</mark>
0Dh	—	Unimplem	ented		—						
0Eh	TMR1L	Holding Re	egister for th	ie Least Sigr	ificant Byte o	of the 16-bit T	MR1			xxxx xxxx	uuuu u <mark>uuu</mark>
0Fh	TMR1H	Holding Re	egister for th	e Most Sign	ificant Byte of	the 16-bit T	MR1	11	1. Starten and 1. Sta	XXXX XXXX	uuuu uuuu
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	0000 0000	uuuu uuuu
11h	BAUDCTL	ABDOVF	RCIDL		SCKP	BRG16	-//	WUE	ABDEN	01-0 0-00	01-0 0-00
12h	SPBRGH	USART Ba	ud Rate Hi	gh Generato	r					0000 0000	0000 0000
13h	SPBRG	USART Ba	aud Rate Ge	enerator			111	27	1	0000 0000	0000 0000
14h	RCREG	USART Re	eceive Regi	ster			1			0000 0000	0000 0000
15h	TXREG	USART Tr	ansmit Regi	ster				/		0000 0000	0000 0000
16h	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
17h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	2000 000x	0000 000x
18h	WDTCON	—	_	_	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	0 1000	0 1000
19h	CMCON0	C2OUT	C10UT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
1Ah	CMCON1	_	_	_	_	_	—	T1GSS	C2SYNC	10	10
1Bh	_	Unimpleme	ented							_	—
1Ch	-	Unimplem	ented		0	101	1		3	EY.	Ŧ
1Dh	14	Unimplem	ented		COM W		1	6	800	_	7-
1Eh	ADRESH	Most Signi	ficant 8 bits	of the left sh	ifted A/D resu	ult or 2 bits o	f right shifte	d result		xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADFM	VCFG	—	CHS2	CHS1	CHS0	GO/DONE	ADON	00-0 0000	00-0 0000
-	•	-									

TABLE 2-1: PIC16F688 SPECIAL REGISTERS SUMMARY BANK 0

Legend: -= Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented
 Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: MCLR and WDT Reset does not affect the previous value data latch. The RAIF bit will be cleared upon reset but will set again if the mismatched exists.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOD Reset	Value on all other Resets ⁽¹⁾
INDF	Addressin register)	g this location	on uses cont	tents of FSR	data mem	ory (not a p	hysical	XXXX XXXX	XXXX XXXX	
OPTION_REG	RAPU INTEDG TOCS TOSE PSA PS2 PS1 PS0							1111 1111	1111 1111	
PCL	Program C	Counter's (P	C) Least Sig	nificant Byte	9				0000 0000	0000 0000
STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
FSR	Indirect Da	ata Memory	Address Po	inter					xxxx xxxx	uuuu uuuu
TRISA	-	-	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	11 1111	11 1111
_	Unimplem	ented		_					—	_
TRISC	_	-	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	11 1111	11 1111
_	Unimplem	ented	1							_
_	Unimplem	ented	115						14	_
PCLATH	_	/	// — · · ·	Write Buffe	r for upper	5 bits of Pro	ogram Coui	nter	0 0000	0 0000
INTCON	GIE	PEIE	TOIE	INTE	RAIE	T0IF	INTF	RAIF ⁽³⁾	0000 0000	0000 0000
PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE	0000 0000	0000 0000
_	Unimplem	ented	1					11	-	_
PCON	_//	_	ULPWUE	SBODEN	_		POR	BOD	01qq	0uuu
OSCCON	4	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 x000	-110 x000
OSCTUNE	14	_		TUN4	TUN3	TUN2	TUN1	TUNO	0 0000	u uuuu
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANSO	1111 1111	1111 1111
	Unimplem	ented				11-	—			
-//	Unimplem	ented							<u> </u>	_
11-	Unimplem	ented				11	S.F.		—	—
WPUA ⁽²⁾	- 1		WPUA5	WPUA4	/	WPUA2	WPUA1	WPUA0	11 -111	11 -111
IOCA	-	_	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	00 0000	00 0000
EEDATH	_	_	EEPROM	Data Registe	er				00 0000	0000 0000
EEADRH	_	_	_	_	EEPROM	Address R	egister		0000	0000 0000
VRCON	VREN	_	VRR	_	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000
EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
EECON1	EEPGD	-		_	WRERR	WREN	WR	RD	x x000	u q000
EECON2	EEPROM	Control 2 R	egister (not	a physical re	gister)	1		and the second		····
ADRESL					<u> </u>	the right sh	ifted result	3.90	xxxx xxxx	uuuu uuuu
ADCON1		ADCS2	ADCS1	ADCS0				CO.C	-000	-000
	Name	NameBit 7INDFAddressin register)OPTION_REGRAPUPCLProgram 0STATUSIRPFSRIndirect DTRISA——UnimplemTRISC——UnimplemPCLATH—PCLATH—INTCONGIEPIE1EEIE—UnimplemPCON—OSCCON—OSCTUNE—INTELANSFIMNSELANS7—UnimplemUnimplem—Unimplem—PCATH—PCON—OSCCON—OSCTUNE—IOSA—VRONVRENEEDATH—VRCONVRENEEDATH—VRCONVRENEEDATEEDAT7EECON1EEPGDEECON2EEPROMADRESLLeast Sign	NameBit 7Bit 6INDFAddressiver)OPTION_REGRAPUINTEDGPCLProgram Counter's (PSTATUSIRPRPIRP1FSRIndirect Data MemoryTRISA——UnimplementedTRISC——UnimplementedPCLATH——UnimplementedPCLATH——UnimplementedPCLATH——UnimplementedPCLATH——UnimplementedPCON—GSCCONIRCF2OSCCON—ANSELANS7ANSELANS7ANSELANS7MIDIE—IOCA——UnimplementedMPUA(2)—IOCA——UnimplementedMRCNVREN——IOCA——ICA——IOCA——ICA—ICA—ICA—ICA—ICA—ICAIOCAI—ICAIOCAI—ICAICAIICAIICAIICAIICAIICAIICAIICAIICAIICAIICAI	NameBit 7Bit 6Bit 5INDFAddressing this location uses contregister)OPTION_REGRAPUINTEDGTOCSPCLProgram Counter's (PC) Least SigSTATUSIRPRP1RP0FSRIndirect Data Memory Address PoTRISA——TRISA5—UnimplementedTRISC5—UnimplementedTRISC——TRISC5—UnimplementedTOIEPCLATH——PCLATH——INTCONGIEPEIEPIE1EEIEADIEPCON—ULPWUEOSCCONIRCF2IRCF1OSCTUNE———Unimplemented—MNSELANS7ANS6ANS5—Unimplemented—MUNIMPLE——VPUA(2)——MPUA(2)——WPUA(2)——WPUA(2)——WPUA(2)——WPUASIOCAIOCA——VRCONVREN—VRCONVREN—EEDATH——WPUAEEDAT6EEDAT5EECON1EEPGD—EECON2EEPROM Control 2 Register (notADRESLLeast Significant 2 bits of the left st	Name Bit 7 Bit 6 Bit 5 Bit 4 INDF Addressing this location uses contents of FSR register) OPTION_REG RAPU INTEDG TOCS TOSE PCL Program Counter's (PC) Least Significant Byte STATUS IRP RP1 RP0 TO FSR Indirect Data Memory Address Pointer TRISA4 — — TRISA5 TRISA4 — Unimplemented — TRISC5 TRISC4 — Unimplemented — Unimplemented PCLATH — — TRISC5 TRISC4 — Unimplemented PCIATH — — Write Buffe INTCON GIE PEIE TOIE INTE PIE1 EEIE ADIE RCIE C2IE — Unimplemented — — UNA ANS4 ANS4 <td< td=""><td>Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 INDF Addressing this location uses contents of FSR to address register) OPTION_REG RAPU INTEDG TOCS TOSE PSA PCL Program Counter's (PC) Least Significant Byte STATUS IRP RP1 RP0 TO PD FSR Indirect Data Memory Address Pointer TRISA4 TRISA3 — Unimplemented TRISA — — TRISC5 TRISC4 TRISC3 — Unimplemented — TRISC4 TRISC3 — Unimplemented — — Write Buffer for upper PCLATH — — — Write Buffer for upper INTCON GIE PEIE TOIE INTE RAIE PIE1 EEIE ADIE RCF2 IRCF1 IRCF0 OSTS OSCTUNE — — — — — — </td><td>Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 INDF Addressing this location uses contents of FSR to address data memory register) OPTION_REG RAPU INTEDG TOCS TOSE PSA PS2 PCL Program Counter's (PC) Least Significant Byte STATUS IRP RP1 RP0 TO PD Z FSR Indirect Data Memory Address Pointer TRISA — — TRISA TRISA3 TRISA2 — Unimplemented — TRISC5 TRISC4 TRISC3 TRISC2 — Unimplemented — — TRISC5 TRISC4 TRISC3 TRISC2 — Unimplemented — — Write Buffer for upper 5 bits of Printing TOIF PIE1 EEIE ADIE RCIE C2IE C1IE OSTE PCON — — Unimplemented — — — — OSCCON — IRCF2 IRCF1 IRCF0 OSTE HTS</td><td>Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 INDF Addressing this location uses contents of FSR to address data memory (not a pregister) OPTION_REG RAPU INTEDG TOCS TOSE PSA PS2 PS1 PCL Program Counter's (PC) Least Significant Byte STATUS IRP RP1 RP0 TO PD Z DC FSR Indirect Data Memory Address Pointer TRISA4 TRISA3 TRISA2 TRISA1 TRISA3 TRISA2 TRISA1 TRISC2 TRISC1 Unimplemented - Unimplemented - TRISC5 TRISC4 TRISC3 TRISC2 TRISC1 INTE - Unimplemented - - Write Buffer for upper 5 bits of Program Coull INTC0N GE PEIE TOIE INTE RAIE TOIF INTE PIE1 EEIE ADIE RCIE C2IE CIIE OSFIE TXIE PCON - - ULPWUE SBODEN -<td>Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 INDF Addressing this location uses contents of FSR to address data memory (not a physical register) OPTION_REG RAPU INTEOG TOSE PSA PS2 PS1 PS0 PCL Program Counter's (PC) Least Significant Byte STATUS IRP RP1 RP0 TO PD Z DC C FSR Indirect Data Memory Address Pointer TRISA — — TRISA TRISA TRISA TRISA TRISA TRISA TRISC3 TRISC3 TRISC2 TRISA TRISA — Unimplemented TRISC4 TRISC3 TRISC2 TRISC1 TRISC0 — Unimplemented TOE INTE RAIE TOIF INTF RAIF¹³ PIE1 EEIE ADIE PCIE CIE CIE CIE CIE TRISC3 TRISC2 TRISC1 TRISC0 PCLATH — — — Write</td><td>Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 Value on POR/BOD Reset INDF Addressing this location uses contents of FSR to address data memory (not a physical register) xxxx xxxx OPTION_REG RAPU INTEDG TOCS TOSE PSA PS2 PS1 PS0 11111 1111 PCL Program Counter's (PC) Least Significant Byte 0000</td></td></td<>	Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 INDF Addressing this location uses contents of FSR to address register) OPTION_REG RAPU INTEDG TOCS TOSE PSA PCL Program Counter's (PC) Least Significant Byte STATUS IRP RP1 RP0 TO PD FSR Indirect Data Memory Address Pointer TRISA4 TRISA3 — Unimplemented TRISA — — TRISC5 TRISC4 TRISC3 — Unimplemented — TRISC4 TRISC3 — Unimplemented — — Write Buffer for upper PCLATH — — — Write Buffer for upper INTCON GIE PEIE TOIE INTE RAIE PIE1 EEIE ADIE RCF2 IRCF1 IRCF0 OSTS OSCTUNE — — — — — —	Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 INDF Addressing this location uses contents of FSR to address data memory register) OPTION_REG RAPU INTEDG TOCS TOSE PSA PS2 PCL Program Counter's (PC) Least Significant Byte STATUS IRP RP1 RP0 TO PD Z FSR Indirect Data Memory Address Pointer TRISA — — TRISA TRISA3 TRISA2 — Unimplemented — TRISC5 TRISC4 TRISC3 TRISC2 — Unimplemented — — TRISC5 TRISC4 TRISC3 TRISC2 — Unimplemented — — Write Buffer for upper 5 bits of Printing TOIF PIE1 EEIE ADIE RCIE C2IE C1IE OSTE PCON — — Unimplemented — — — — OSCCON — IRCF2 IRCF1 IRCF0 OSTE HTS	Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 INDF Addressing this location uses contents of FSR to address data memory (not a pregister) OPTION_REG RAPU INTEDG TOCS TOSE PSA PS2 PS1 PCL Program Counter's (PC) Least Significant Byte STATUS IRP RP1 RP0 TO PD Z DC FSR Indirect Data Memory Address Pointer TRISA4 TRISA3 TRISA2 TRISA1 TRISA3 TRISA2 TRISA1 TRISC2 TRISC1 Unimplemented - Unimplemented - TRISC5 TRISC4 TRISC3 TRISC2 TRISC1 INTE - Unimplemented - - Write Buffer for upper 5 bits of Program Coull INTC0N GE PEIE TOIE INTE RAIE TOIF INTE PIE1 EEIE ADIE RCIE C2IE CIIE OSFIE TXIE PCON - - ULPWUE SBODEN - <td>Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 INDF Addressing this location uses contents of FSR to address data memory (not a physical register) OPTION_REG RAPU INTEOG TOSE PSA PS2 PS1 PS0 PCL Program Counter's (PC) Least Significant Byte STATUS IRP RP1 RP0 TO PD Z DC C FSR Indirect Data Memory Address Pointer TRISA — — TRISA TRISA TRISA TRISA TRISA TRISA TRISC3 TRISC3 TRISC2 TRISA TRISA — Unimplemented TRISC4 TRISC3 TRISC2 TRISC1 TRISC0 — Unimplemented TOE INTE RAIE TOIF INTF RAIF¹³ PIE1 EEIE ADIE PCIE CIE CIE CIE CIE TRISC3 TRISC2 TRISC1 TRISC0 PCLATH — — — Write</td> <td>Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 Value on POR/BOD Reset INDF Addressing this location uses contents of FSR to address data memory (not a physical register) xxxx xxxx OPTION_REG RAPU INTEDG TOCS TOSE PSA PS2 PS1 PS0 11111 1111 PCL Program Counter's (PC) Least Significant Byte 0000</td>	Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 INDF Addressing this location uses contents of FSR to address data memory (not a physical register) OPTION_REG RAPU INTEOG TOSE PSA PS2 PS1 PS0 PCL Program Counter's (PC) Least Significant Byte STATUS IRP RP1 RP0 TO PD Z DC C FSR Indirect Data Memory Address Pointer TRISA — — TRISA TRISA TRISA TRISA TRISA TRISA TRISC3 TRISC3 TRISC2 TRISA TRISA — Unimplemented TRISC4 TRISC3 TRISC2 TRISC1 TRISC0 — Unimplemented TOE INTE RAIE TOIF INTF RAIF ¹³ PIE1 EEIE ADIE PCIE CIE CIE CIE CIE TRISC3 TRISC2 TRISC1 TRISC0 PCLATH — — — Write	Name Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0 Value on POR/BOD Reset INDF Addressing this location uses contents of FSR to address data memory (not a physical register) xxxx xxxx OPTION_REG RAPU INTEDG TOCS TOSE PSA PS2 PS1 PS0 11111 1111 PCL Program Counter's (PC) Least Significant Byte 0000

PIC16F688 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1 **TABLE 2-2:**

- = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation. Legend:

Note 1:

2: RA3 pull-up is enabled when pin is configured as MCLR in the Configuration Word register.

MCLR and WDT Reset does not affect the previous value data latch. The RAIF bit will be cleared upon reset but will set again if the 3: mismatched exists.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOD Reset	Value on all other Resets ⁽¹⁾
Bank 2											
100h	INDF	Addressing register)	g this locatio	on uses cor	itents of FSF	R to address	s data memo	ory (not a pł	nysical	XXXX XXXX	XXXX XXXX
101h	TMR0	Timer0 Mc	odule's regis	ter						XXXX XXXX	uuuu uuuu
102h	PCL	Program C	Counter's (P	0000 0000	0000 0000						
103h	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
104h	FSR	Indirect Da	ata Memory	Address Po	ointer					XXXX XXXX	uuuu uuuu
105h	PORTA	-	_	RA5	RA4	RA3	RA2	RA1	RA0	xx xx00	uu uuuu
106h	-	Unimplem	ented							_	-
107h	PORTC	-	_	RC5	RC4	RC3	RC2	RC1	RC0	xx xx00	uu uuuu
108h	-	Unimplem	ented	11	-					<u></u>	_
109h	_	Unimplem	ented	1993. 1993					1		—
10Ah	PCLATH	_	4	_	Write Buff	er for upper	5 bits of Pro	ogram Coun	iter	0 0000	0 0 <mark>000</mark>
10Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	T0IF	INTF	RAIF ⁽²⁾	0000 0000	0000 0000
10Ch	_	Unimplem	ented	-	_						
10Dh	_	Unimplem	Unimplemented								
10Eh	_	Unimplem	ented					15		-	
10Fh		Unimplem	ented					11	4	_	_
110h	//	Unimplem	ented						1		
111h	H	Unimplem	ented				11	/ _			
112h	1/-	Unimplem	ented				del -				
113h 🦪	- 11	Unimplem	ented				1	1	No. of Concession, Name	-	
114h		Unimplem	ented			/		1		_	
115h		Unimplem	ented							— ,	
116h	64	Unimplem	ented								
117h		Unimplem	ented							_	
118h	-	Unimplem	ented								
119h	_	Unimplem	ented							_	_
11Ah	_	Unimplem	ented							_	_
11Bh	_	Unimplem	ented			100			30	-	
11Ch	Ch #h 1	Unimplem	ented	NI AL	AND I	1	10	11	and the second	- T	1 A
11Dh	E/E/	Unimplem	ented			L V				U -/m	
11Eh	-	Unimplem	ented				0			_	
11Fh	_	Unimplem	ented							_	_

Legend:

- = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: MCLR and WDT Reset does not affect the previous value data latch. The RAIF bit will be cleared upon reset but will set again if the mismatched exists.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOD Reset	Value on all other Resets ⁽¹⁾
Bank 3											
180h	INDF	Addressing register)	g this locatio	XXXX XXXX	xxxx xxxx						
181h	OPTION_REG	RAPU INTEDG TOCS TOSE PSA PS2 PS1 PS0									1111 1111
182h	PCL	Program C	Counter's (P	C) Least Sig	nificant Byte	9				0000 0000	0000 0000
183h	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
184h	FSR	Indirect Da	ata Memory	Address Po	inter					xxxx xxxx	uuuu uuuu
185h	TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	11 1111	11 1111
186h	—	Unimplem	ented							—	—
187h	TRISC	_	_	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	11 1111	11 1111
188h	_	Unimplem	ented	11							
189h	—	Unimplem	Unimplemented								_
18Ah	PCLATH	_		/_	Write Buffe	r for upper	5 bits of Pro	ogram Cou	nter	0 0000	0 0000
18Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	T0IF	INTF	RAIF ⁽²⁾	0000 0000	0000 0000
18Ch	_	Unimplem	Unimplemented								_
18Dh	_	Unimplem	ented	1					11		_
190h	—	Unimplem	ented	1					1	-	_
191h	—	Unimplem	ented							J# _	
192h	—	Unimplem	ented							_	—
193h		Unimplem	ented					11	1	4	
194h	- //	Unimplem	ented						1	11-	_
195h	-4//	Unimplem	ented				di la			V	_
196h	14	Unimplem	ented				11	S.		_	—
19Ah	11-	Unimplem	ented							—	_
19Bh 📝	/ _ /	Unimplem	ented							_	_
199h		Unimplem	ented			r.					_
19Ah	-	Unimplem	ented							_	_
19Bh		Unimplem	ented							_	- 35
19Ch	_	Unimplem	ented							_	_
19Dh	_	Unimplem	ented							_	—
19Eh		Unimplem	ented			. المعربي			-		_
19Fh		Unimplem	ented		-		1 1		-		7 💷 🔏

TABLE 2-4: PIC16F688 SPECIAL FUNCTION REGISTERS SUMMARY BANK 3

Legend: -= Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: MCLR and WDT Reset does not affect the previous value data latch. The RAIF bit will be cleared upon reset but will set again if the mismatched exists.

8

2.2.2.1 Status Register

The Status register, shown in Register 2-1, contains:

- · the arithmetic status of the ALU
- · the Reset status
- the bank select bits for data memory (SRAM)

The Status register can be the destination for any instruction, like any other register. If the Status register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the Status register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the Status register as '000u uluu' (where u = unchanged). It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the Status register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (see Section 12.0 "Instruction Set Summary").

- Note 1: Bits IRP and RP1 (Status<7:6>) are not used by the PIC16F688 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.
 - 2: The <u>C</u> and <u>DC</u> bits operate as a Borrow and <u>Digit</u> Borrow out bit, respectively, in subtraction. See the <u>SUBLW</u> and <u>SUBWF</u> instructions for examples.

	CTATUS	OTATUC	DECISTE			h 102h 0	D 4026)						
REGISTER 2-1:	R/W-0	R/W-0	R/W-0	R-1	SS: 03h, 8 3 R-1	R/W-x	R/W-x	R/W-x					
	IRP	RP1	RP0	ТО	PD	Z	DC	C					
bit 7	1 = Bank 2,		ct bit (used fo	r indirect addr	ressing)			bit 0					
bit 6-5	00 = Bank (01 = Bank 1 10 = Bank 2	RP<1:0>: Register Bank Select bits (used for direct addressing) 00 = Bank 0 (00h-7Fh) 01 = Bank 1 (80h-FFh) 10 = Bank 2 (100h-17Fh) 11 = Bank 3 (180h-1FFh)											
bit 4	TO: Time-or												
Bie bit 3	0 = A WDT PD : Power- 1 = After po	time-out occu	irred the CLRWDT i			le	C.	V.					
bit 2			0	operation is z operation is r									
bit 1	 0 = The result of an arithmetic or logic operation is not zero DC: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) For borrow, the polarity is reversed. 1 = A carry-out from the 4th low-order bit of the result occurred 0 = No carry-out from the 4th low-order bit of the result 												
bit 0	C : Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred												
Note 1: For borrow, the polarity is reversed. A subtraction is executed by adding the two complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded w either the high or low-order bit of the source register.													

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

© 2004 Microchip Technology Inc.

www.agelectronica.com

2.2.2.2 Option Register

The Option register is a readable and writable register, which contains various control bits to configure:

- TMR0/WDT prescaler
- External RA2/INT interrupt
- TMR0
- Weak pull-ups on PORTA

Note: To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT by setting PSA bit to '1' (Option<3>). See Section 5.4 "Prescaler".

REGISTER 2-2:	OPTION_I	reg – op [.]	TION REG	STER (AD	DRESS: 8	1h OR 181	i h)

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RAPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0
	bit 7							bit 0
bit 7		ORTA Pull-up						
		A pull-ups ar A pull-ups ar		v individual	nort latch va			
bit 6		nterrupt Edg		y in larvia dan		liues		
bit 0		pt on rising e		/INT pin			1	
	0 = Interru	pt on falling	edge of RA2	2/INT pin			1	
bit 5	2011 C C C C C C C C C C C C C C C C C C	R0 Clock So		bit			r	
		tion on RA2/ al instruction						
bit 4		R0 Source E	•					
DIL 4		nent on high-	•		TOCKI pin	7 4		
		nent on low-t						
bit 3		caler Assign						
		aler is assign						
bit 2.0		aler is assign			9			
bit 2-0		Prescaler Ra			_			
	BI	T VALUE T	MR0 RATE	WDT RAT	E			
		000	1:2	1:1			1	V TET
Klor	1796	001 010	1:4 1:8	1:2 1:4	- 4	614	2 🌔	' I /
		011	1:16	1:8 1:16	K Lø			(@ . 1 7 - @ :
		100	1:64	1:32				
		110	1:128	1:64				
		111	1 : 256	1 : 128				
	Legend:							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, PORTA change and external RA2/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON – INTERRUPT CONTROL REGISTER (ADDRESS: 0Bh OR 8Bh)

		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF
		bit 7	1					1	bit 0
	bit 7	1 = Enable	I Interrupt E s all unmasi es all interru	ked interru <mark>p</mark> t	ts				
	bit 6	1 = Enable	s all unmas	upt Enable t ked peripher eral interrup	ral interrupts				
	bit 5	1 = Enable	0 Overflow s the TMR0 es the TMR0		able bit			/	
	bit 4	1 = Enable	s the RA2/II	al Interrupt E NT external NT extern <mark>a</mark> l	interrupt				
	bit 3	1 = Enable	s the PORT	Interrupt Er A change in A change in	terrupt				
	bit 2	1 = TMR0	register has	Interrupt Fla overflowed not overflow	(must be cle	ared in soft	ware)		1
Ele	bit 1 PCU bit 0	1 = The RA 0 = The RA RAIF: POR 1 = When a	A2/INT exter A2/INT exter RTA Change at least one	nal interrupt Interrupt Fla of the PORT	did not occu	s changed s	<i>le</i>		software)
					o be enable				
		2:			mer0 rolls ov aring T0IF b		is unchange	ed on Reset	and should
		Legend:							
		R = Reada	ble bit	W = W	/ritable bit	U = Unim	plemented	bit, read as '	0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

 $[\]ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

2.2.2.4 PIE1 Register

The PIE1 register contains the interrupt enable bits, as shown in Register 2-4.

Note:	Bit PEIE (INTCON<6>) must be set to
	enable any peripheral interrupt.

REGISTER 2-4:	PIE1 – PEI	RIPHERAL	INTERRU	IPT ENABI	LE REGIST	ER 1 (ADD	DRESS: 80	;h)
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE
	bit 7							bit 0
bit 7		Vrite Compl						
		s the EE wri es the EE wr						
bit 6		Converter In						
		s the A/D co es the A/D co						
bit 5		RT Receive						
DIT 5		s the USAR						
		es the USAR					1	
bit 4		parator 2 In					1	
		s the Compa						_ 0
		es the Comp						
bit 3		parator 1 In s the Comp						
		es the Comp				7 4		
bit 2	OSFIE: Os	cillator Fail	Interrupt En	able bit	1			
		s the oscilla						
		es the oscilla						
bit 1		RT Transmi						1
		s the USAR						
bit 0		imer1 Overf						
TTI	1 = Enable	s the Timer	overflow in	terrupt				Y 📲 🗶
Liec	0 = Disable	es the Timer	1 overflow in	hterrupt	Ale	ue	5 U	n Ve
	Legend:							
	R = Reada	ble bit	W = W	/ritable bit	U = Unim	plemented	bit, read as	'0'
	- n = Value	at POR	'1' = B	it is set	'0' = Bit is	s cleared	x = Bit is u	nknown

1

2.2.2.5 PIR1 Register

The PIR1 register contains the interrupt flag bits, as shown in Register 2-5.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1 – PERIPHERAL INTERRUPT REQUEST REGISTER 1 (ADDRESS: 0Ch)

		R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0
		EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF
		bit 7						1	bit 0
bi	it 7		ROM Write C						
			te operation						
h	it 6		te operation		impleted or n	as not been	staned		
D	11.0		Interrupt Flag	-				/	
			nversion has		eted or has r	not been sta	rted		111
bi	it 5 🥢	RCIF: USA	RT Receive	Interrupt F	lag bit				-0
		1 = The US	SART receive	buffer is f	ull				
		0 = The US	SART receive	buffer is e	empty		. J		
bi	it 4	C2IF: Com	parator 2 Inte	errupt Fla <mark>g</mark>	bit	S.			
			rator 2 outpu			e cleared in	software)		
1			rator 2 outpu						
D	it 3	•	parator 1 Inte			a alaorad in	a officiar of		
			rator 1 outpu rator 1 outpu			e cleared in	sonware)		199
bi	it 2	•	cillator Fail In		0				
			oscillator fai		•	anged to INT	OSC (must	be cleared	in software)
	and to		clock opera		C 1	<u>ا</u>	all some	N.	T Z
bi	it 1		RT Transmit					1. Ja	1.
			ART transm ART transm						
h	it O		mer1 Overflo						
			register over	•	•	d in softwar	e)		
			has not over				-)		
		Legend:							
		R = Reada	ble bit	W = V	Vritable bit	U = Unim	plemented l	bit, read as	'0'

- n = Value at POR

'1' = Bit is set

x = Bit is unknown

'0' = Bit is cleared

www.agelectronica.com

2.2.2.6 **PCON Register**

The Power Control (PCON) register (See Table 12-2) contains flag bits to differentiate between a:

- Power-on Reset (POR)
- Brown-out Detect (BOD)
- Watchdog Timer Reset (WDT)
- External MCLR Reset

The PCON register also controls the Ultra Low-Power Wake-up and software enable of the BOD.

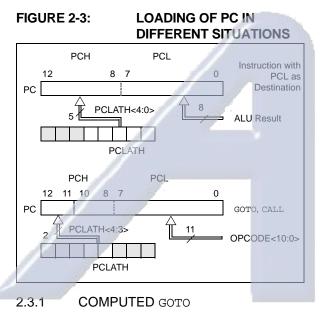
The PCON register bits are shown in Register 2-6.

REGISTER 2-6:	PCON – P	OWER CO	ONTROL R	EGISTER (ADDRES	S: 8Eh)		
	U-0	U-0	R/W-0	R/W-1	U-0	U-0	R /W-0	R/W-x
	—	H	ULPWUE	SBODEN	_		POR	BOD
	bit 7		1					bit 0
bit 7-6	Unimplem							
bit 5	ULPWUE:	Ultra Low-F	ower Wake-	up Enable b	oit			1.00
			ake-up enab				1	
			ake-up disab					
bit 4	SBODEN:	Software B	OD Enable b	_{oit} (1)				
	1 = BOD er					1		
	0 = BOD di	sabled						
bit 3-2	Unimplem	ented: Rea	d as '0'					
bit 1	POR: Powe	er-on Reset	: St atus bit					
	1 = No Pov						-	
				nust be set ir	n software a	fter a Powe	er-on Reset o	ccurs)
bit 0			ct Status bit					
			ect occurred		in coffwore	offer o Drei		
The second second	0 = A Brow	n-out Detec	ct occurred (must de set	in software	anter a Brov	wn-out Detec	(occurs)
Elec	Note 1:	BODEN<1	:0> = 01 in th	ne Configura	tion Word re	egister for th	is bit to contr	ol the BOD.
	Legend:							
	P – Peada	hla hit	$\lambda \Lambda = \lambda \Lambda$	/ritable bit	II – I Inin	nlemented	hit road as	'O'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.3 PCL and PCLATH

The program counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL (PCLATH<4:0> \rightarrow PCH). The lower example in Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> \rightarrow PCH).



A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note AN556, *"Implementing a Table Read"* (DS00556).

2.3.2 STACK

The PIC16F688 family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no Status bits to indicate stack overflow or stack underflow conditions.
2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

S.A. de C.V.

2.4 Indirect Addressing, INDF and **FSR Registers**

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (Status<7>), as shown in Figure 2-4.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAM	PLE 2	-1:	INDIRECT ADDRESSING
M	IOVLW	0x20	;initialize pointer
M	IOVWF	FSR	;to RAM
NEXT C	LRF	INDF	clear INDF register;
I	NCF	FSR	;inc pointer
E	BTFSS	FSR,4	;all done?
G	GOTO	NEXT	;no clear next
CONTIN	NUE		;yes continue

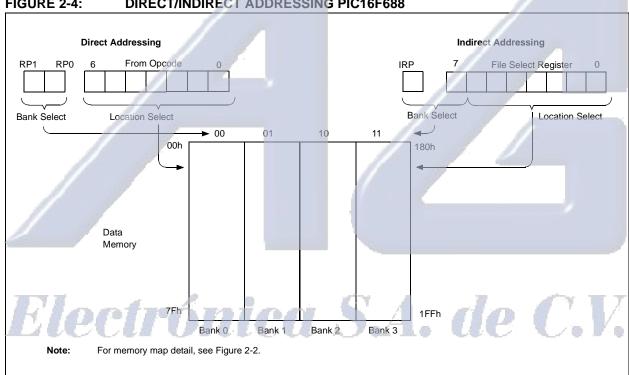


FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC16F688

3.0 CLOCK SOURCES

3.1 Overview

The PIC16F688 has a wide variety of clock sources and selection features to allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 3-1 illustrates a block diagram of the PIC16F688 clock sources.

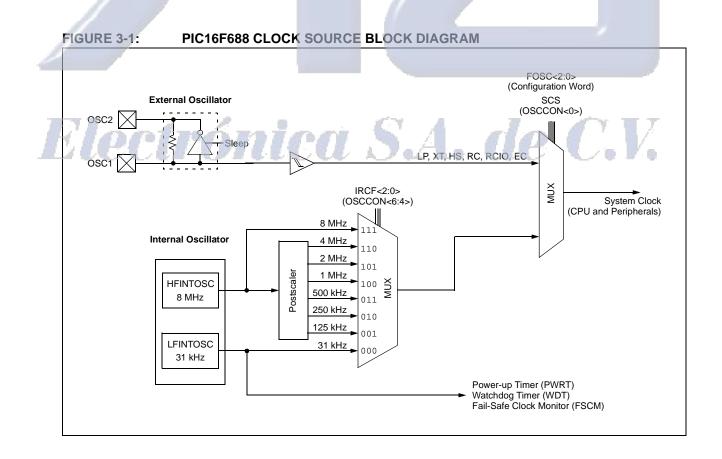
Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators, and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured from one of two internal oscillators, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal via software.
- Two-Speed Clock Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch to the Internal Oscillator.

The PIC16F688 can be configured in one of eight clock modes.

- 1. EC External clock with I/O on RA4.
- 2. LP Low gain Crystal or Ceramic Resonator Oscillator mode.
- 3. XT Medium gain Crystal or Ceramic Resonator Oscillator mode.
- 4. HS High gain Crystal or Ceramic Resonator mode.
- 5. RC External Resistor-Capacitor (RC) with Fosc/4 output on RA4.
- RCIO External Resistor-Capacitor with I/O on RA4.
- 7. INTRC Internal oscillator with Fosc/4 output on RA4 and I/O on RA5.
- 8. INTRCIO Internal oscillator with I/O on RA4 and RA5.

Clock source modes are configured by the FOSC<2:0> bits in the Configuration Word register (see **Section 11.0 "Special Features Of The CPU"**). The internal clock can be generated by two oscillators. The HFINTOSC is a high-frequency calibrated oscillator. The LFINTOSC is a low-frequency uncalibrated oscillator.



© 2004 Microchip Technology Inc.

3.2 Clock Source Modes

Clock source modes can be classified as external or internal.

- External clock modes rely on external circuitry for the clock source. Examples are oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes), and Resistor-Capacitor (RC mode) circuits.
- Internal clock sources are contained internally within the PIC16F688. The PIC16F688 has two internal oscillators: the 8 MHz High-Frequency Internal Oscillator (HFINTOSC) and 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit (see **Section 3.5 "Clock Switching**").

3.3 External Clock Modes

3.3.1 OSCILLATOR START-UP TIMER (OST)

If the PIC16F688 is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from the OSC1 pin, following a Power-on Reset (POR) and the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the PIC16F688. When switching between clock sources a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 3-1.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see Section 3.6 "Two-Speed Clock Start-up Mode").

Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	LFINTOSC HFINTOSC	31 kHz 125 kHz–8 MHz	(1)
Sleep/POR	EC, RC	DC – 20 MHz	5 μs-10 μs (approx.) CPU Start-up ⁽¹⁾
LFINTOSC (31 kHz)	EC, RC	DC – 20 MHz	
Sleep/POR	LP, XT, HS	31 kHz–20 MHz	1024 Clock Cycles (OST)
LFINTOSC (31 kHz)	HFINTOSC	1 <mark>25 kH</mark> z–8 MHz	1 μs (approx.)

TABLE 3-1: OSCILLATOR DELAY EXAMPLES

Note 1: The 5 µs to 10 µs start-up delay is based on a 1 MHz system clock.

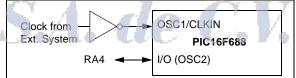
3.3.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 pin and the RA5 pin is available for general purpose I/O. Figure 3-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC16F688 design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 3-2:

EXTERNAL CLOCK (EC) MODE OPERATION



3.3.3 LP, XT, HS MODES

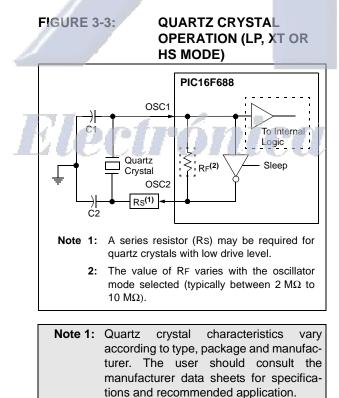
The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to the OSC1 and OSC2 pins (Figure 3-1). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is best suited to drive resonators with a low drive level specification, for example, tuning fork type crystals.

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification, for example, low-frequency/AT-cut quartz crystal resonators.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting, for example, high-frequency/AT-cut quartz crystal resonators or ceramic resonators.

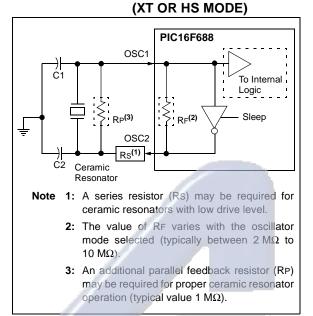
Figure 3-3 and Figure 3-4 show typical circuits for quartz crystal and ceramic resonators, respectively.



2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

FIGURE 3-4:

CERAMIC RESONATOR OPERATION



S.A. de C.V.

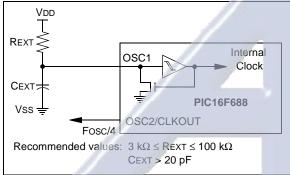
© 2004 Microchip Technology Inc.

3.3.4 EXTERNAL RC MODES

The External Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes, RC and RCIO.

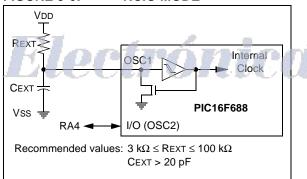
In RC mode, the RC circuit connects to the OSC1 pin. The OSC2/CLKOUT pin outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 3-5 shows the RC mode connections.

FIGURE 3-5: RC MODE



In RCIO mode, the RC circuit is connected to the OSC1 pin. The OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 4 of PORTA (RA4). Figure 3-6 shows the RCIO mode connections.

FIGURE 3-6: RCIO MODE



The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- · component tolerances
- · packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

3.4 Internal Clock Modes

The PIC16F688 has two independent, internal oscillators that can be configured or selected as the system clock source.

- The HFINTOSC (High-Frequency Internal Oscillator) is factory calibrated and operates at 8 MHz. The frequency of the HFINTOSC can be user adjusted ±12% via software using the OSCTUNE register (Register 3-1).
- The LFINTOSC (Low-Frequency Internal Oscillator) is uncalibrated and operates at approximately 31 kHz.

The system clock speed can be selected via software using the Internal Oscillator Frequency Select (IRCF) bits.

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit (see **Section 3.5 "Clock Switching**").

3.4.1 INTRC AND INTRCIO MODES

The INTRC and INTRCIO modes configure the internal oscillators as the system clock source when the device is programmed using the Oscillator Selection (FOSC) bits in the Configuration Word register (Register 11-1).

In **INTRC** mode, the OSC1 pin is available for general purpose I/O. The OSC2/CLKOUT pin outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTRCIO** mode, the OSC1 and OSC2 pins are available for general purpose I/O.

3.4.2 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 8 MHz internal clock source. The frequency of the HFINTOSC can be altered approximately $\pm 12\%$ via software using the OSCTUNE register (Register 3-1).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). One of seven frequencies can be selected via software using the IRCF bits (see Section 3.4.4 "Frequency Select Bits (IRCF)").

The HFINTOSC is enabled by selecting any frequency between 8 MHz and 125 kHz (IRCF \neq 000) as the system clock source (SCS = 1), or when Two-Speed Start-up is enabled (IESO = 1 and IRCF \neq 000).

The HF Internal Oscillator (HTS) bit (OSCCON<2>) indicates whether the HFINTOSC is stable or not.

3.4.2.1 **OSCTUNE** Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-1).

The OSCTUNE register has a tuning range of ±12%. The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number. Due to process variation, the monotonicity and frequency step cannot be specified.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. The HFINTOSC clock will stabilize within 1 ms. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM), and peripherals, are not affected by the change in frequency.

REGISTER 3-1:	OSCTUNE	– OSCILL	ATOR TU	NING RESI	STOR (AD	DRESS: 9	90h)	
	U-0	U- 0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	1-	_	TUN4	TUN3	TUN2	TUN1	TUN0
	bit 7							bit 0
bit 7-5	Unimpleme	nted: Read	as '0'					
bit 4-0	TUN<4:0>:	Frequency	Tuning bit <mark>s</mark>					
	01111 = Ma	ximum freq	uency					
	01110 =					1		
	•							- 0
	00001 =							
	00000 = Os	cillator mod	ule is run <mark>n</mark> i	ing at the cal	ibrated freq	uency.		
	11111 =							
	•				100			
	•							
2	10000 = Mi	nimum frequ	lency					
	Legend:							
	R = Readab	le bit	W = W	/ritable bit	U = Unim	plemented	bit, read as '	0'
1171 - Jack State	- n = Value a	at POR	'1' = B	it is set	<u>(</u> '0' = Bit is	s cleared	x = Bit is u	nknown
<i>Lieci</i>	rol	uc	a	J.A	l. (10	U.	V

^{© 2004} Microchip Technology Inc.

3.4.3 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated (approximate) 31 kHz internal clock source.

The output of the LFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). 31 kHz can be selected via software using the IRCF bits (see **Section 3.4.4 "Frequency Select Bits (IRCF)**"). The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF = 000) as the system clock source (SCS = 1), or when any of the following are enabled:

- Two-Speed Start-up (IESO = 1 and IRCF = 000)
- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The LF Internal Oscillator (LTS) bit (OSCCON<1>) indicates whether the LFINTOSC is stable or not.

3.4.4 FREQUENCY SELECT BITS (IRCF)

The output of the 8 MHz HFINTOSC and 31 kHz LFINTOSC connect to a postscaler and multiplexer (see Figure 3-1). The Internal Oscillator Frequency select bits, IRCF<2:0> (OSCCON<6:4>), select the frequency output of the internal oscillators. One of eight frequencies can be selected via software:

- 8 MHz
- 4 MHz (Default after Reset)
- 2 MHz
- 1 MHz
- 500 kHz
- 250 kHz
- 125 kHz
- 31 kHz

Note:	Following any Reset, the IRCF bits are set
	to '110' and the frequency selection is set
	to 4 MHz. The user can modify the IRCF
	bits to select a different frequency.

3.4.5 HF AND LF INTOSC CLOCK SWITCH TIMING

When switching between the LFINTOSC and the HFINTOSC, the new oscillator may already be shut down to save power. If this is the case, there is a 10 μ s delay after the IRCF bits are modified before the frequency selection takes place. The LTS/HTS bits will reflect the current active status of the LFINTOSC and the HFINTOSC oscillators. The timing of a frequency selection is as follows:

- 1. IRCF bits are modified.
- If the new clock is shut down, a 10 µs clock start-up delay is started.
- 3. Clock switch circuitry waits for a falling edge of the current clock.
- 4. CLKOUT is held low and the clock switch circuitry waits for a rising edge in the new clock.
- 5. CLKOUT is now connected with the new clock. HTS/LTS bits are updated as required.
- 6. Clock switch is complete.

ectrónica S.A. de C.V.

If the internal oscillator speed selected is between 8 MHz and 125 kHz, there is no start-up delay before the new frequency is selected. This is because the old and the new frequencies are derived from the HFINTOSC via the postscaler and multiplexer.

3.5 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bit.

3.5.1 SYSTEM CLOCK SELECT (SCS) BIT

The System Clock Select (SCS) bit (OSCCON<0>) selects the system clock source that is used for the CPU and peripherals.

- When SCS = 0, the system clock source is determined by configuration of the FOSC<2:0> bits in the Configuration Word register (CONFIG).
- When SCS = 1, the system clock source is chosen by the internal oscillator frequency selected by the IRCF bits. After a Reset, SCS is always cleared.
 - Note: Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bit. The user can monitor the OSTS (OSCCON<3>) to determine the current system clock source.

3.5.2 OSCILLATOR START-UP TIME-OUT STATUS BIT

The Oscillator Start-up Time-out Status (OSTS) bit (OSCCON<3>) indicates whether the system clock is running from the external clock source, as defined by the FOSC bits, or from internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes.

3.6 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.

This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

Note: Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit (OSCCON<3>) to remain clear. When the PIC16F688 is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) is enabled (see Section 3.3.1 "Oscillator Start-up Timer (OST)"). The OST timer will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as the OST is counting. When the OST count reaches 1024 and the OSTS bit (OSCCON<3>) is set, program execution switches to the external oscillator.

3.6.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO = 1 (CONFIG<10>) Internal/External Switch Over bit.
- SCS = 0.
- FOSC configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after PWRT has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured to be anything other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

3.6.2 TWO-SPEED START-UP SEQUENCE

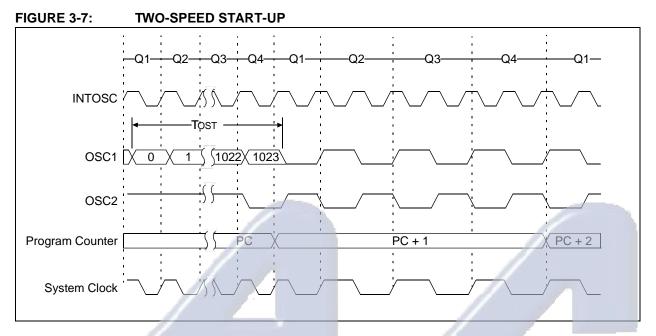
- 1. Wake-up from Power-on Reset or Sleep.
- Instructions begin execution by the internal oscillator at the frequency set in the IRCF bits (OSCCON<6:4>).
- 3. OST enabled to count 1024 clock cycles.
- 4. OST timed out, wait for falling edge of the internal oscillator.
- 5. OSTS is set.
- 6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
- 7. System clock is switched to external clock source.

3.6.3 CHECKING EXTERNAL/INTERNAL CLOCK STATUS

Checking the state of the OSTS bit (OSCCON<3>) will confirm if the PIC16F688 is running from the external clock source as defined by the FOSC bits in the Configuration Word (CONFIG) or the internal oscillator.

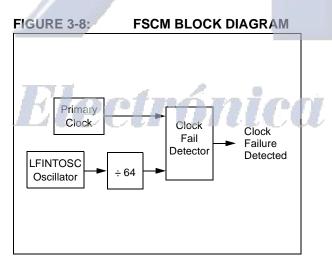
www.agelectronica.com

PIC16F688



3.7 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) is designed to allow the device to continue to operate in the event of an oscillator failure. The FSCM can detect oscillator failure at any point after the device has exited a Reset or Sleep condition and the Oscillator Start-up Timer (OST) has expired.



The FSCM function is enabled by setting the FCMEN bit in the Configuration Word (CONFIG). It is applicable to all external clock options (LP, XT, HS, EC, RC or IO modes).

In the event of an external clock failure, the FSCM will set the OSFIF bit (PIR1<2>) and generate an oscillator fail interrupt if the OSFIE bit (PIE1<2>) is set. The device will then switch the system clock to the internal oscillator. The system clock will continue to come from the internal oscillator unless the external clock recovers and the Fail-Safe condition is exited. The frequency of the internal oscillator will depend upon the value contained in the IRCF bits (OSCCON<6:4>). Upon entering the Fail-Safe condition, the OSTS bit (OSCCON<3>) is automatically cleared to reflect that the internal oscillator is active and the WDT is cleared. The SCS bit (OSCCON<0>) is not updated. Enabling FSCM does not affect the LTS bit.

The FSCM sample clock is generated by dividing the INTRC clock by 64. This will allow enough time between FSCM sample clocks for a system clock edge to occur. Figure 3-8 shows the FSCM block diagram.

On the rising edge of the sample clock, the monitoring latch (CM = 0) will be cleared. On a falling edge of the primary system clock, the monitoring latch will be set (CM = 1). In the event that a falling edge of the sample clock occurs, and the monitoring latch is not set, a clock failure has been detected. The assigned internal oscillator is enabled when FSCM is enabled as reflected by the IRCF.

Note: Two-Speed Start-up is automatically enabled when the Fail-Safe Clock Monitor mode is enabled.

Note: Primary clocks with a frequency ≤ ~488 Hz will be considered failed by the FSCM. A slow starting oscillator can cause an FSCM interrupt.

DS41203B-page 28

 $\ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

3.7.1 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, the execution of a SLEEP instruction, or a modification of the SCS bit. While in Fail-Safe condition, the PIC16F688 uses the internal oscillator as the system clock source. The IRCF bits (OSCCON<6:4>) can be modified to adjust the internal oscillator frequency without exiting the Fail-Safe condition.

The Fail-Safe condition must be cleared before the OSFIF flag can be cleared.

Sample Clock System Clock Output		Oscillator Failure	
CM Output (Q)			Failure
OSCFIF			Detected
	†		
	CM Test	CM Test	CM Test
	e system clock is normally at a muc s example have been chosen for cla		le clock. The relative frequencies in

FIGURE 3-9: FSCM TIMING DIAGRAM

3.7.2 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect oscillator failure at any point after the device has exited a Reset or Sleep condition and the Oscillator Start-up Timer (OST) has expired. If the external clock is EC or RC mode, monitoring will begin immediately following these events.

For LP, XT or HS mode the external oscillator may require a start-up time considerably longer than the FSCM sample clock time, a false clock failure may be detected (see Figure 3-9). To prevent this, the internal oscillator is automatically configured as the system clock and functions until the external clock is stable (the OST has timed out). This is identical to Two-Speed Start-up mode. Once the external oscillator is stable, the LFINTOSC returns to its role as the FSCM source.

Note: Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the OSTS bit (OSCCON<3>) to verify the oscillator start-up and system clock switchover has successfully completed. **S.A. de C.V.**

^{© 2004} Microchip Technology Inc.

OSCCON – OSCILLATOR CONTROL REGISTER (ADDRESS: 8Fh) REGISTER 3-2: R/W-1 R/W-1 R/W-0 U-0 R-1 R-0 R-0 R/W-0 SCS IRCF2 IRCF1 IRCF0 OSTS⁽¹⁾ HTS LTS bit 7 bit 0 bit 7 Unimplemented: Read as '0' bit 6-4 IRCF<2:0>: Internal Oscillator Frequency Select bits 000 = 31 kHz001 = 125 kHz010 = 250 kHz011 = 500 kHz100 = 1 MHz101 = 2 MHz110 = 4 MHz 111 = 8 MHz bit 3 OSTS: Oscillator Start-up Time-out Status bit 1 = Device is running from the external system clock defined by FOSC<2:0> 0 = Device is running from the internal system clock (HFINTOSC or LFINTOSC) HTS: HFINTOSC (High Frequency - 8 MHz to 125 kHz) Status bit bit 2 1 = HFINTOSC is stable 0 = HFINTOSC is not stable bit 1 LTS: LFINTOSC (Low Frequency - 31 kHz) Stable bit 1 = LFINTOSC is stable 0 = LFINTOSC is not stable SCS: System Clock Select bit bit 0 1 = Internal oscillator is used for system clock 0 = Clock source defined by FOSC<2:0> Note 1: Bit resets to '0' with Two-Speed Start-up and LP, XT or HS selected as the Oscillator mode or Fail-Safe mode is enabled.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD	Value on all other Resets
0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE	0000 0000	0000 0000
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS ⁽²⁾	HTS	LTS	SCS	-110 x000	-110 x000
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	0 0000	u uuuu
2007h ⁽¹⁾	CONFIG	CPD	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	_	_

Legend: x = unknown, u = unchanged, ---- = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

Note 1: See Register 11-1 for operation of all Configuration Word bits.

2: See Register 3-2 for details.

4.0 I/O PORTS

There are as many as twelve general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

Note:	Additional information on I/O ports may be
	found in the "PICmicro® Mid-Range MCU
	Family Reference Manual" (DS33023).

4.1 PORTA and the TRISA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). The exception is RA3, which is input only and its TRISA bit will always read as '1'. Example 4-1 shows how to initialize PORTA.

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the port data latch. RA3 reads '0' when MCLRE = 1.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

Note: The ANSEL (91h) and CMCON0 (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 4-1: INITIALIZING PORTA

BCF	STATUS, RPO	;Bank 0
CLRF	PORTA	;Init PORTA
MOVLW	07h	;Set RA<2:0> to
MOVWF	CMCON0	;digital I/O
BSF	STATUS, RPO	;Bank 1
CLRF	ANSEL	;digital I/O
MOVLW	0Ch	;Set RA<3:2> as inputs
MOVWF	TRISA	;and set RA<5:4,1:0>
		;as outputs
BCF	STATUS, RPO	;Bank 0

4.2 Additional Pin Functions

Every PORTA pin on the PIC16F688 has an interrupton-change option and a weak pull-up option. PORTA also provides an Ultra Low-Power Wake-up option. The next three sections describe these functions.

4.2.1 WEAK PULL-UPS

Each of the PORTA pins, except RA3, has an individually configurable internal weak pull-up. Control bits WPUAx enable or disable each pull-up. Refer to Register 4-3. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the RAPU bit (Option<7>). A weak pull-up is automatically enabled for RA3 when configured as MCLR and _disabled when RA3 is an I/O. There is no software control of the MCLR pull-up.

S.A. de C.V.

REGISTER 4-1: PORTA – PORTA REGISTER (ADDRESS: 05h OR 105h)

			ADDILLOO		511)		
U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-0	R/W-0
_		RA5	RA4	RA3	RA2	RA1	RA0
bit 7			•			•	bit 0
•							
Legend:							
R = Reada	ble bit	VV = V	Vritable bit	U = Unimp	lemented b	it, read as '	0'
- n = Value	at POR	'1' = E	Bit is set	'0' = Bit is (cleared	x = Bit is ur	nknown

© 2004 Microchip Technology Inc.

bit 7-6: bit 5-0:

Preliminary



	U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
	bit 7						1	bit (
bit 7-6:	Unimplem	ented: Rea	ad as '0'					
bit 5-0:	TRISA<5:0	0> : PORTA	Tri-State Co	ntrol bits				
		1 = PORTA pin configured as an input (tri-stated)0 = PORTA pin configured as an output						
	Note 1:	TRISA<3>	always read	ds '1'.				
	2:	TRISA<5:	4> always re	ads '1' in X	T, HS and LP (OSC modes	s.	
	Legend:			1			11	
	R = Reada	able bit	VV = V	/ritable bit	U = Unimp	lemented b	oit, read as '	0'
	- n = Value	e at POR	'1' = B	it is set	'0' = Bit is	cleared	x = Bit is ur	nknown
EGISTER 4-3:				•	DDRESS: 95			
	U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
	<u></u>		WPUA5	WPUA4		WPUA2	WPUA1	WPUA0
	bit 7							bit (
	Dit 1							
hit 7.0		anted. Doc				1. 6		
bit 7-6	Unimplem	ented: Rea		tor bito		1		
bit 7-6 bit 5-4	Unimplem WPUA<5:4	4>: Weak P	ad as '0' 'ull-up Regis	ter bits				
	Unimplem WPUA<5:4 1 = Pull-up	4>: Weak P enabled		ter bits				
	Unimplem WPUA<5:4 1 = Pull-up 0 = Pull-up	4>: Weak P enabled	Pull-up Regis	ter bits				
bit 5-4	Unimplem WPUA<5:4 1 = Pull-up 0 = Pull-up Unimplem	4>: Weak P enabled disabled ented: Rea	Pull-up Regis					
bit 5-4 bit 3	Unimplem WPUA<5:4 1 = Pull-up 0 = Pull-up Unimplem	4>: Weak P o enabled o disabled nented: Rea 0>: Weak P	'ull-up Regis [.] ad as '0'					
bit 5-4 bit 3	Unimplem WPUA<5:4 1 = Pull-up 0 = Pull-up Unimplem WPUA<2:0	4>: Weak P o enabled o disabled nented: Rea 0>: Weak P o enabled	'ull-up Regis [.] ad as '0'			_		
bit 5-4 bit 3	Unimplem WPUA<5:4 1 = Pull-up 0 = Pull-up Unimplem WPUA<2:0 1 = Pull-up	4>: Weak P o enabled o disabled nented: Rea 0>: Weak P o enabled o disabled	Pull-up Regis ad as '0' Pull-up Regis	ter bits	individual pull	-ups to be e	enabled.	
bit 5-4 bit 3	Unimplem WPUA<5:4 1 = Pull-up 0 = Pull-up Unimplem WPUA<2:0 1 = Pull-up 0 = Pull-up	4>: Weak P o enabled o disabled nented: Rea 0>: Weak P o enabled o disabled Global RA	Pull-up Regis ad as '0' Pull-up Regis PU must be pull-up devid	ter bits enabled for	individual pull- atically disable-			mode
bit 5-4 bit 3	Unimplem WPUA<5:4 1 = Pull-up 0 = Pull-up Unimplem WPUA<2:0 1 = Pull-up 0 = Pull-up 0 = Pull-up Note 1: 2:	4>: Weak P o enabled o disabled nented: Rea 0>: Weak P o enabled o disabled Global RA The weak (TRISA = The RA3 p	Pull-up Regis ad as '0' Pull-up Regis PU must be pull-up devic 0).	ter bits enabled for ce is automa abled when		d if the pin	is in output	

R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.2.2 INTERRUPT-ON-CHANGE

Each of the PORTA pins is individually configurable as an interrupt-on-change pin. Control bits IOCAx enable or disable the interrupt function for each pin. Refer to Register 4-4. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set the PORTA Change Interrupt Flag bit (RAIF) in the INTCON register.

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

- Any read or write of PORTA. This will end the a) mismatch condition, then
- Clear the flag bit RAIF. b)

A mismatch condition will continue to set flag bit RAIF. Reading PORTA will end the mismatch condition and allow flag bit RAIF to be cleared. The latch holding the last read value is not affected by a MCLR nor BOD Reset. After these Resets, the RAIF flag will continue to be set if a mismatch is present.

If a change on the I/O pin should occur Note: when the read operation is being executed (start of the Q2 cycle), then the RAIF interrupt flag may not get set.

REGISTER 4-4: IOCA - INTERRUPT-ON-CHANGE PORTA REGISTER (ADDRESS: 96h)

	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W- 0	R/W-0
		_	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0
	bit 7					1		bit 0
						1		
bit 7-6	Unimplem	ented: Rea	d as '0'					
bit 5-0	IOCA<5:0>	>: Interrupt-o	on-change F	ORTA Conti	rol bits			
		ot-on-chang			1			
	0 = Interrup	ot-on-chang	e disabled					
	Note 1:	Global Interrecognized		le (GIE) mu	ist be enab	oled for indiv	vidual interr	rupts to be
	2:	IOCA<5:4>	always rea	ds '1' in XT,	HS and LP	OSC modes		
11.11	Legend:			17 I	4	.7	AN C	
HIOPH	R = Reada	ble bit	W = W	/ritable bit	U = Unin	nplemented l	bit, read as	0'
LIVUUU	- n = Value	at POR	/ * 	it is set	'0' = Bit i	s cleared	x = Bit is u	nknown

4.2.3 ULTRA LOW-POWER WAKE-UP

The Ultra Low-Power Wake-up (ULPWU) on RA0 allows a slow falling voltage to generate an interrupton-change on RA0 without excess current consumption. The mode is selected by setting the ULPWUE bit (PCON<5>). This enables a small current sink which can be used to discharge a capacitor on RA0.

To use this feature, the RA0 pin is configured to output '1' to charge the capacitor, interrupt-on-change for RA0 is enabled, and RA0 is configured as an input. The ULPWUE bit is set to begin the discharge and a SLEEP instruction is performed. When the voltage on RA0 drops below VIL, an interrupt will be generated which will cause the device to wake-up. Depending on the state of the GIE bit (INTCON<7>), the device will either jump to the interrupt vector (0004h) or execute the next instruction when the interrupt event occurs. See Section 4.2.2 "INTERRUPT-ON-CHANGE" and Section 11.5.3 "PORTA Interrupt" for more information.

This feature provides a low-power technique for periodically waking up the device from Sleep. The time-out is dependent on the discharge time of the RC circuit on RA0. See Example 4-2 for initializing the Ultra Low-Power Wake-up module.

The series resistor provides overcurrent protection for the RA0 pin and can allow for software calibration of the time-out. (see Figure 4-1). A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired interrupt delay. This technique will compensate for the affects of temperature, voltage and component accuracy. The Ultra Low-Power Wake-up peripheral can also be configured as a simple programmable low voltage detect or temperature sensor.

Note: For more information, refer to Application Note AN879, "Using the Microchip Ultra Low-Power Wake-up Module" (DS00879).

EXAMPLE 4-2: ULTRA LOW-POWER WAKE-UP INITIALIZATION

BCF	STATUS, RPO	;Bank 0
BSF	PORTA, 0	Set RAO data latch
MOVLW	н / 7 /	Turn off
	/	
MOVWF	CMCON0	; comparators
BSF	STATUS, RPO	;Bank 1
BCF	ANSEL,0	;RA0 to digital I/O
BCF	TRISA,0	;Output high to
CALL	CapDelay	; charge capacitor
BSF	PCON,ULPWUE	;Enable ULP Wake-up
BSF	IOCA,0	;Select RA0 IOC
BSF	TRISA,0	;RAO to input
MOVLW	B'10001000'	;Enable interrupt
MOVWF	INTCON	; and clear flag
SLEEP		;Wait for IOC

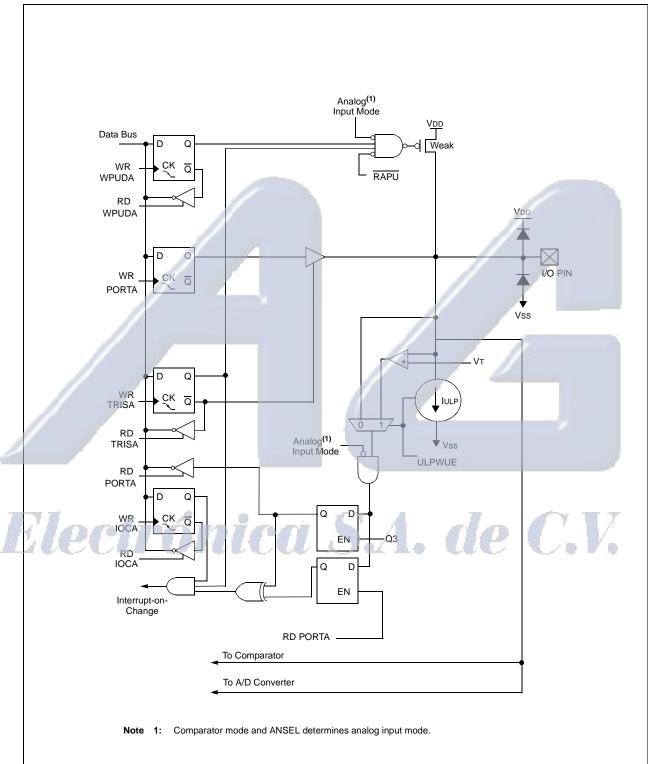


S.A. de C.V.

DS41203B-page 34

PIC16F688





 $[\]ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

www.agelectronica.com **PIC16F688**

4.2.4 PIN DESCRIPTIONS AND DIAGRAMS

Each PORTA pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the A/D, refer to the appropriate section in this data sheet.

RA0/AN0/C1IN+/ICSPDAT/ULPWU 4.2.4.1

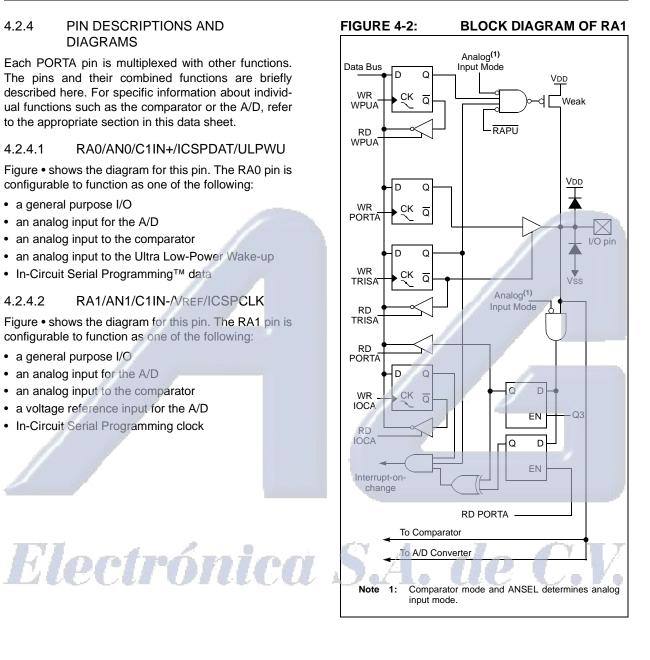
Figure • shows the diagram for this pin. The RA0 pin is configurable to function as one of the following:

- a general purpose I/O
- · an analog input for the A/D
- an analog input to the comparator
- an analog input to the Ultra Low-Power Wake-up
- In-Circuit Serial Programming[™] data

4.2.4.2 RA1/AN1/C1IN-/VREF/ICSPCLK

Figure • shows the diagram for this pin. The RA1 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D
- an analog input to the comparator
- a voltage reference input for the A/D
- In-Circuit Serial Programming clock



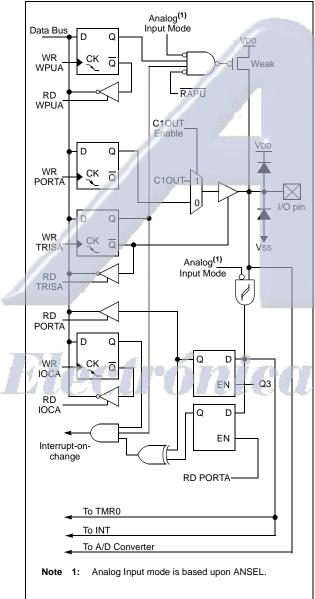
4.2.4.3 RA2/AN2/T0CKI/INT/C1OUT

Figure 4-3 shows the diagram for this pin. The RA2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D
- the clock input for TMR0
- an external edge triggered interrupt
- a digital output from the comparator

FIGURE 4-3:

BLOCK DIAGRAM OF RA2

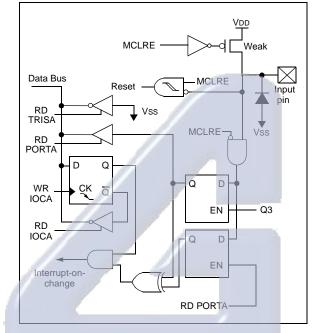


4.2.4.4 RA3/MCLR/VPP

Figure 4-4 shows the diagram for this pin. The RA3 pin is configurable to function as one of the following:

- a general purpose input
- · as Master Clear Reset with weak pull-up

FIGURE 4-4: BLOCK DIAGRAM OF RA3



S.A. de C.V.

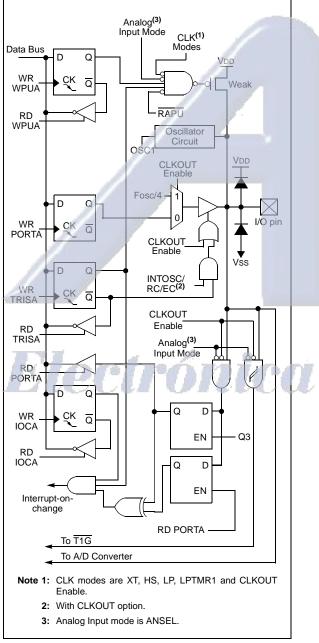
^{© 2004} Microchip Technology Inc.

RA4/AN3/T1G/OSC2/CLKOUT 4.2.4.5

Figure 4-5 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- a general purpose I/O
- · an analog input for the A/D
- · a TMR1 gate input
- · a crystal/resonator connection
- · a clock output

FIGURE 4-5: **BLOCK DIAGRAM OF RA4**



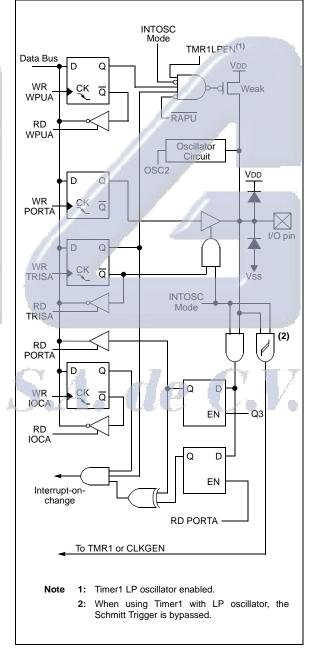
4.2.4.6 RA5/T1CKI/OSC1/CLKIN

Figure 4-6 shows the diagram for this pin. The RA5 pin is configurable to function as one of the following:

- a general purpose I/O
- a TMR1 clock input
- · a crystal/resonator connection
- a clock input



BLOCK DIAGRAM OF RA5



Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD	Value on all other Resets
05h/105h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	xx xx00	uu uu00
0Bh/8Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
19h	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
81h	OPTION_REG	RAPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h/185h	TRISA	_	_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	11 1111	11 1111
91h	ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
95h	WPUA	_	—	WPUA5	WPUA4	_	WPUA2	WPUA1	WPUA0	11 -111	11 -111
96h	IOCA	-	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	00 0000	00 0000

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.



Electrónica S.A. de C.V.

PIC16F688

4.3 PORTC

PORTC is a general purpose I/O port consisting of 6 bidirectional pins. The pins can be configured for either digital I/O or analog input to A/D converter or comparator. For specific information about individual functions such as the EUSART or the A/D, refer to the appropriate section in this data sheet.

Note:	The ANSEL (91h) and CMCON0 (19h)
	registers must be initialized to configure
	an analog channel as a digital input. Pins
	configured as analog inputs will read '0'.

EXAMPLE 4-3: INITIALIZING PORTC

		- 1 0
BCF	STATUS, RPO	;Bank 0
CLRF	PORTC	;Init PORTC
MOVLW	07h	;Set RC<4,1:0> to
MOVWF	CMCON0	;digital I/O
BSF	STATUS, RPO	;Bank 1
CLRF	ANSEL	;digital I/O
MOVLW	0Ch	;Set RC<3:2> as inputs
MOVWF	TRISC	;and set RC<5:4,1:0>
		;as outputs
BCF	STATUS, RPO	;Bank 0

4.3.1 RC0/AN4/C2IN+

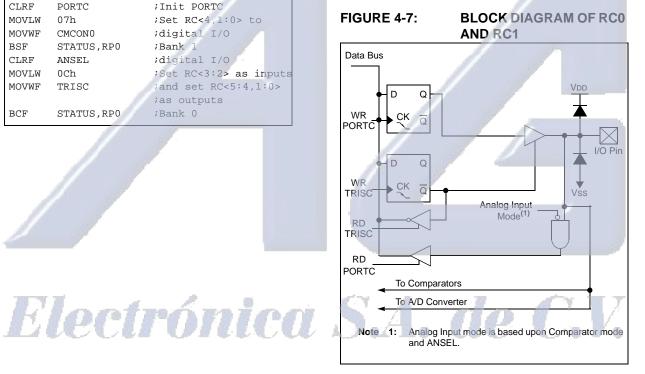
The RC0 is configurable to function as one of the following:

- a general purpose I/O
- · an analog input for the A/D Converter
- · an analog input to the comparator

RC1/AN5/C2IN-4.3.2

The RC1 is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D Converter
- · an analog input to the comparator



DS41203B-page 40

X

I/O Pin

Vss

8

4.3.3 RC2/AN6

The RC2 is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D Converter

RC3/AN7 4.3.4

The RC3 is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D Converter

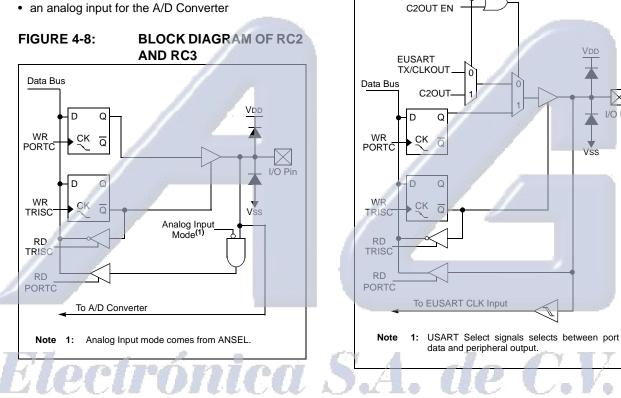
4.3.5 RC4/C2OUT/TX/CK

The RC4 is configurable to function as one of the following:

- a general purpose I/O
- · a digital output from the comparator
- a digital I/O for the EUSART

USART Select(1)





© 2004 Microchip Technology Inc.

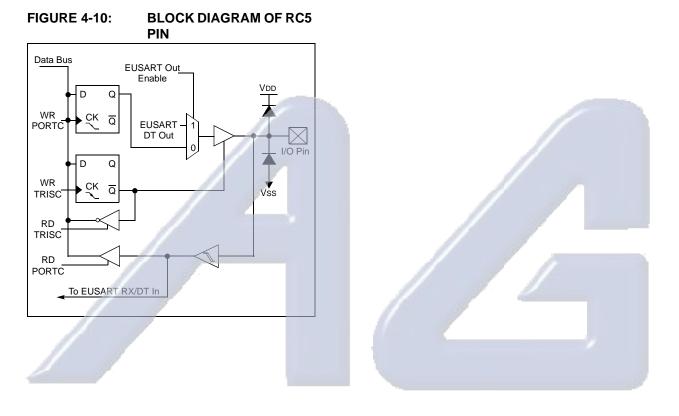
www.agelectronica.com

4.3.6 RC5/RX/DT

PIC16F688

The RC5 is configurable to function as one of the following:

- a general purpose I/O
- a digital I/O for the EUSART



Electrónica S.A. de C.V.

DS41203B-page 42

GISTER 4-5:	PORTC – PO	RTC R	EGISTER (ADDRESS	: 07h OR ⁻	107h)		
	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-0	R/W-0
	_		RC5	RC4	RC3	RC2	RC1	RC0
	bit 7							bit
bit 7-6:	Unimplement	t ed : Rea	d as '0'					
bit 5-0:	PORTC<5:0>:		I Purpose I/0) Pin bits				
	1 = Port pin is 0 = Port pin is							
	Legend:							-
	R = Readable	bit	W = W	ritable bit		•	bit, read as	
	- n = Value at	POR	'1' = Bi	t is set	'0' = Bit is	s cleared	x = Bit is u	nknown
GISTER 4-6:	TRISC – POF	RTC TR	I-STATE RI R/W-1	E GISTER (R/W-1	ADDRESS	5: 87h OR R/W-1	187h) R/W-1	R/W-1
	0-0	0-0	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC
	bit 7		111303	111004		TRIGGZ	TRIBET	bit
bit 7-6:	Unimplement	ted: Rea	d as '0'			1		
bit 5-0:	TRISC<5:0>:	PORTC	Tri-State Cor	ntrol bits				
	1 = PORTC pi 0 = PORTC pi				ed)			
	Legend:							
	R = Readable	bit	W = W	ritable bit	U = Unim	plemented	bit, read as	0'
				and the second se		s cleared		

TABLE 4-2:	SUMMARY OF REGISTERS	S ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit	Bit 0	Value on: POR, BOD	Value on all other Resets
07h	PORTC	—	_	RC5	RC4	RC3	RC2	RC1	RC0	xx xx00	uu uu00
19h	CMCON0	C2OUT	C10UT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	11 1111	11 1111
91h	ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

 $[\]ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

www.agelectronica.com

PIC16F688

NOTES:



Electrónica S.A. de C.V.

DS41203B-page 44

Preliminary

© 2004 Microchip Technology Inc.

www.agelectronica.com

5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 5-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

Note:	Additional information on the Timer0
	module is available in the "PICmicro® Mid-
	Range MCU Family Reference Manual"
	(DS33023).

5.1 Timer0 Operation

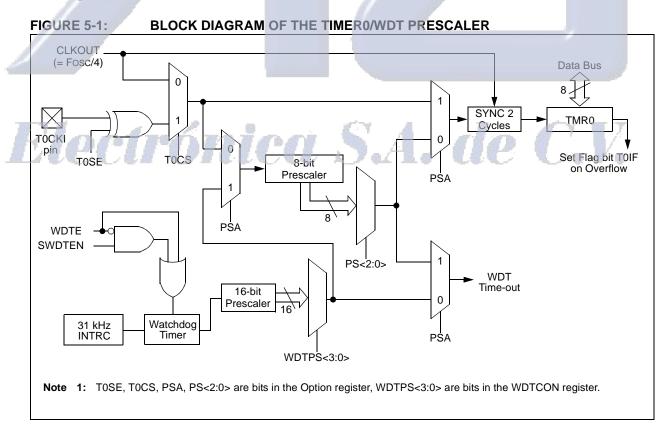
Timer mode is selected by clearing the TOCS bit (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION_REG<5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin RA2/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION_REG<4>). Clearing the T0SE bit selects the rising edge.

Note: Counter mode has specific external clock requirements. Additional information on these requirements is available in the *"PICmicro® Mid-Range MCU Family Reference Manual"* (DS33023).

5.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit (INTCON<2>). The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from Sleep, since the timer is shut off during Sleep.



^{© 2004} Microchip Technology Inc.

5.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2 Tosc (and a small RC delay of 20 ns) and low for at least 2 Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

Note: The ANSEL (91h) and CMCON0 (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

101

110

111

1:64

1:128

1:256

	d as analog i							
REGISTER 5-1:	OPTION I	REG - OP		SISTER (AD	DRESS: 8	1h OR 181	h)	
		R/W-1 .	R/W-1	R/W-1	R/W-1	R/ W-1	R/W-1	R/W-1
	RAPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0
	bit 7							bit 0
bit 7		RTA Pull-up						
		A pull-ups ar A pull-ups ar		oy individual	port latch va	lues in WPL	JA register	
bit 6		nterrupt Edg						
		ot on rising e ot on falling						
bit 5		R0 Clock So		t bit				
		ion on RA2/ I instruction		(CLKOUT)				
bit 4		R0 Source E						
				sition on RA2 sition on RA2			1	Y III Y
bit 3		caler Assign		SILION UNIXAZ		680	> 🖉 -	11/1
LIVEL	1 = Presca	ler is assign	ed to the V		K LO			(B B
		U		ïmer0 module	e			
bit 2-0	PS<2:0>:	Prescaler Ra						
	1	Bit Value T	MR0 Rate	WDT Rate ⁽¹)			
		000 001	1:2 1:4	1:1 1:2				
		010	1:4 1:8	1:2				
		011	1:16	1:8				
		100	1:32	1:16				

Note 1: A dedicated 16-bit WDT postscaler is available for the PIC16F688. See Section 11.7 "Watchdog Timer (WDT)" for more information.

1:32

1:64

1:128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

DS41203B-page 46

© 2004 Microchip Technology Inc.

5.4 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as "prescaler" throughout this data sheet. The prescaler assignment is controlled in software by the control bit PSA (OPTION_REG<3>). Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS<2:0> bits (OPTION_REG<2:0>).

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x...etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer.

5.4.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on-the-fly" during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 5-1 and Example 5-2) must be executed when changing the prescaler assignment from Timer0 to WDT.

EXAMPLE 5-1: CHANGING PRESCALER (TIMER0 \rightarrow WDT)

BCF CLRWDT	STATUS, RPO	;Bank 0 ;Clear WDT
CLRF	TMR0	;Clear TMR0 and
		; prescaler
BSF	STATUS, RPO	;Bank 1
MOVLW	b'00101111'	;Required if desired
MOVWF	OPTION_REG	; PS2:PS0 is
CLRWDT		; 000 or 001
		;
MOVLW	b'00101xxx'	;Set postscaler to
MOVWF	OPTION_REG	; desired WDT rate
BCF	STATUS, RPO	;Bank 0

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 5-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 5-2:

CHANGING PRESCALER (WDT→TIMER0)

11	;Clear WDT and
STATUS, RPO	; prescaler ;Bank 1
b'xxxx0xxx'	;Select TMR0, ; prescale, and
1	; clock source
OPTION_REG STATUS,RPO	; ;Bank 0
	b'xxxx0xxx' OPTION_REG

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
01h	TMR0	Timer0 M	lodule regi	ster / 💶		79 Q.C				xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
81h	OPTION_REG	RAPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h/185h	TRISA	_	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	11 1111	11 1111

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

Legend: -= Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

www.agelectronica.com

PIC16F688

NOTES:



Electrónica S.A. de C.V.

DS41203B-page 48

Preliminary

© 2004 Microchip Technology Inc.

www.agelectronica.com

6.0 TIMER1 MODULE WITH GATE CONTROL

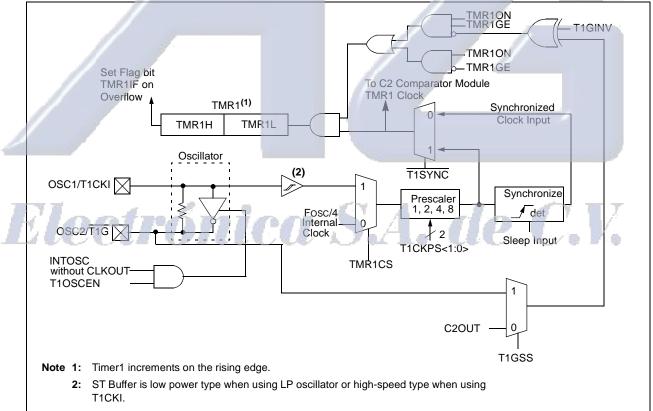
The PIC16F688 has a 16-bit timer. Figure 5-1 shows the basic block diagram of the Timer1 module. Timer1 has the following features:

- 16-bit timer/counter (TMR1H:TMR1L)
- Readable and writable
- Internal or external clock selection
- Synchronous or asynchronous operation
- Interrupt-on-overflow from FFFFh to 0000h
- Wake-up upon overflow (Asynchronous mode)
- · Optional external enable input
 - Selectable gate source: T1G or C2 output (T1GSS)
 - Selectable gate polarity (T1GINV)
- · Optional LP oscillator

The Timer1 Control register (T1CON), shown in Register 6-1, is used to enable/disable Timer1 and select the various features of the Timer1 module.

Note:	Additional information on timer modules is									
	available in the "PICmicro® Mid-Range									
	MCU Family Reference Manual'	'								
	(DS33023).									





www.agelectronica.com

^{© 2004} Microchip Technology Inc.

6.1 **Timer1 Modes of Operation**

Timer1 can operate in one of three modes:

16-bit timer with prescaler

PIC16F688

- 16-bit synchronous counter
- 16-bit asynchronous counter

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized the microcontroller system clock or run to asynchronously.

In Counter and Timer modules, the counter/timer clock can be gated by the Timer1 gate, which can be selected as either the $\overline{T1G}$ pin or Comparator 2 output.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

Note:	In Counter mode, a falling edge must be
	registered by the counter prior to the first
	incrementing rising edge.

6.2 **Timer1 Interrupt**

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit (PIR1<0>) is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 Interrupt Enable bit (PIE1<0>)
- PEIE bit (INTCON<6>)
- GIE bit (INTCON<7>)

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

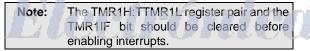


FIGURE 6-2:

6.3 **Timer1 Prescaler**

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits (T1CON<5:4>) control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

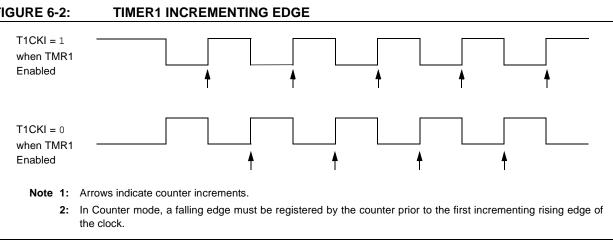
6.4 **Timer1 Gate**

Timer1 gate source is software configurable to be the T1G pin or the output of Comparator 2. This allows the device to directly time external events using $\overline{T1G}$ or analog events using Comparator 2. See CMCON1 (Register 7-2) for selecting the Timer1 gate source. This feature can simplify the software for a Delta-Sigma A/D converter and many other applications. For more information on Delta-Sigma A/D converters, see the Microchip web site (www.microchip.com).

Note: TMR1GE bit (T1CON<6>) must be set to use either T1G or C2OUT as the Timer1 gate source. See Register 7-2 for more information on selecting the Timer1 gate source.

Timer1 gate can be inverted using the T1GINV bit (T1CON<7>), whether it originates from the T1G pin or Comparator 2 output. This configures Timer1 to measure either the active-high or active-low time between events.

S.A. de C.V.



© 2004 Microchip Technology Inc.

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N
	bit 7	I		1				bit 0
bit 7	T1GINV:	Fimer1 Gate	Invert bit ⁽¹⁾					
		1 gate is inve 1 gate is not						
bit 6	<u>If TMR10</u> This bit is <u>If TMR10</u>	ignored. <u>N = 1:</u>						
	1 = Timer 0 = Timer	1 is on if Tim 1 is on	ier1 gate is i	not active				
bit 5-	11 = 1:8 F 10 = 1:4 F 01 = 1:2 F	1:0>: Timer Prescale Valu Prescale Valu Prescale Valu Prescale Valu	ne ne	k Prescale S	Select bits			
bit 3	If INTOSC 1 = LP os	cillator is ena cillator is off	KOUT osci <mark>ll</mark>	ator is active	<u>a:</u>			
bit 2	T1SYNC: TMR1CS	Timer1 Exte <u>= 1:</u>			onization Co	ntrol bit		
	0 = Synch <u>TMR1CS</u>		nal clock inp		ock.			
bit 1		Timer1 Cloo al clock fror		elect bit (on the risir	ng edge)	300		
bit 0				Set	1. (le	C.	V .

Note 1: T1GINV bit inverts the Timer1 gate logic, regardless of source.

2: TMR1GE bit must be set to use either T1G pin or C2OUT, as selected by the T1GSS bit (CMCON1<1>), as a Timer1 gate source.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

 $[\]circledast$ 2004 Microchip Technology Inc.

6.5 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt-on-overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see Section 6.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode").

Note: The ANSEL (91h) and CMCON0 (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

6.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Examples in the "*PICmicro[®] Mid-Range MCU Family Reference Manual*" (DS33023) show how to read and write Timer1 when it is running in Asynchronous mode.

6.6 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins OSC1 (input) and OSC2 (amplifier output). It is enabled by setting control bit, T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 32 kHz. It will continue to run during Sleep. It is primarily intended for a 32 kHz crystal. Table 3-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is derived from the internal oscillator. As with the system LP oscillator, the user must provide a software time delay to ensure proper oscillator start-up.

TRISA5 and TRISA4 bits are set when the Timer1 oscillator is enabled. RA5 and RA4 read as '0' and TRISA5 and TRISA4 bits read as '1'.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

6.7 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- Timer1 must be on (T1CON<0>)
- TMR1IE bit (PIE1<0>) must be set
- PEIE bit (INTCON<6>) must be set

The device will wake-up on an overflow. If the GIE bit (INTCON<7>) is set, the device will wake-up and jump to the Interrupt Service Routine (0004h) on an overflow. If the GIE bit is clear, execution will continue with the next instruction.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Valu POR,		all c	e on other sets
0Bh/ 8Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	TOIF	INTF	RAIF	0000	0000	0000	0000
0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000	0000	0000	0000
0Eh	TMR1L	Holding r	egister for	the Least S	ignificant B	yte of the 16	-bit TMR1	register		xxxx	xxxx	uuuu	uuuu
0Fh	TMR1H	Holding r	egister for	the Most Si	gnificant By	te of the 16	-bit TMR1	register		xxxx	xxxx	uuuu	uuuu
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000	0000	uuuu	uuuu
1Ah	CMCON1	—	_	_	_	_	_	T1GSS	C2SYNC		10		10
8Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE	0000	0000	0000	0000

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER1

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

DS41203B-page 52

Preliminary

7.0 COMPARATOR MODULE

The comparator module contains two analog comparators. The inputs to the comparators are multiplexed with I/O port pins RA0, RA1, RC0 and RC1, while the outputs are multiplexed to pins RA2 and RC4. An on-chip Comparator Voltage Reference (CVREF) can also be applied to the inputs of the comparators.

The CMCON0 register (Register 7-1) controls the comparator input and output multiplexers. A block diagram of the various comparator configurations is shown in Figure 7-3.

REGISTER 7-1:	CMCON0 -	- COMPAF	ATOR CO	NFIGURA	FION REG	ISTER (AD	DRESS: 1	9h)
	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	C2OUT	C10UT	C2INV	C1INV	CIS	CM2	CM1	CM0
	bit 7							bit 0
bit 7	C2OUT: Co When C2IN 1 = C2 VIN- 0 = C2 VIN- When C2IN 1 = C2 VIN- 0 = C2 VIN-	+ > C2 VIN- + < C2 VIN- IV = 1: + < C2 VIN-	Output bit					
bit 6		$\frac{VV = 0}{VV}$ + > C1 VIN- + < C1 VIN- <u>IV = 1</u> : + < C1 VIN-	Output bit					
bit 5	1 = C2 outp	mparator 2 (out inverted out not inver	а	rsion bit				
bit 4	C1INV: Cor	mparator 1 (Dutput Inver	rsion bit				
Ele bit 3	0 = C1 Out CIS: Comp	put inverted put not inve arator Input	rted Switch bit	S.A	1. (le	<i>C</i> .	V_{\bullet}
	1 = C1 VIN- C2 VIN 0 = C1 VIN- C2 VIN When CM< 1 = C1 VIN-	$\frac{2:0> = 010:}{\text{connects to}}$ - connects to - connects to - connects to $\frac{2:0> = 001:}{\text{connects to}}$	o RA0/AN0 o RC0/AN4 o RA1/AN1 o RC1/AN5 o RA0/AN0					
bit 2		Comparator shows the C		modes and (CM<2:0> bit	settings		
	Legend: R = Readal	ble bit	W = W	/ritable bit	U = Unin	nplemented	bit, read as	ʻ0'

© 2004 Microchip Technology Inc.

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

7.1 Comparator Operation

A single comparator is shown in Figure 7-1 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 7-1 represent the uncertainty due to input offsets and response time.

Note: To use CIN+ and CIN- pins as analog inputs, the appropriate bits must be programmed in the CMCON0 (19h) register.

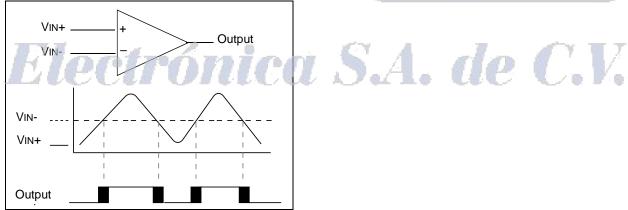
The polarity of the comparator output can be inverted by setting the CxINV bits (CMCON0<5:4>). Clearing CxINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 7-1.

TABLE 7-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	CINV	CxOUT
VIN- > VIN+	0	0
VIN- < VIN+	0	1
VIN- > VIN+	1	1
VIN- < VIN+	1	0

FIGURE 7-1:

SINGLE COMPARATOR

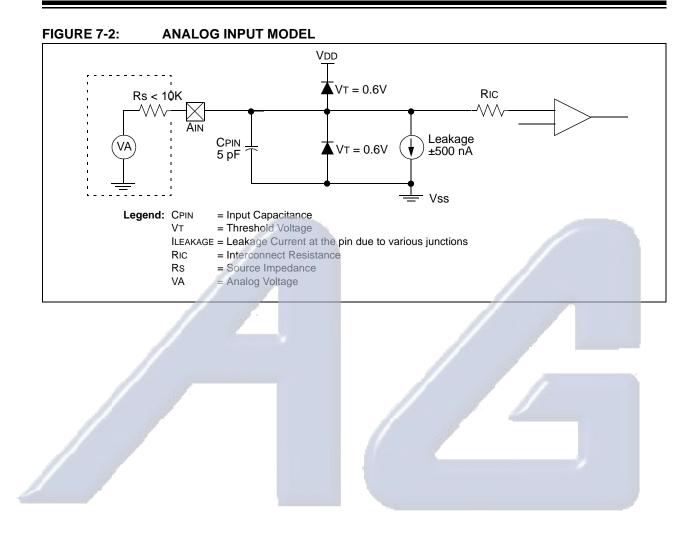


7.2 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 7-2. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and Vss. The analog input, therefore, must be between Vss and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 k Ω is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

- Note 1: When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as analog inputs according to the input specification.
 - 2: Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified.

www.agelectronica.com PIC16F688



Electrónica S.A. de C.V.

$\ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

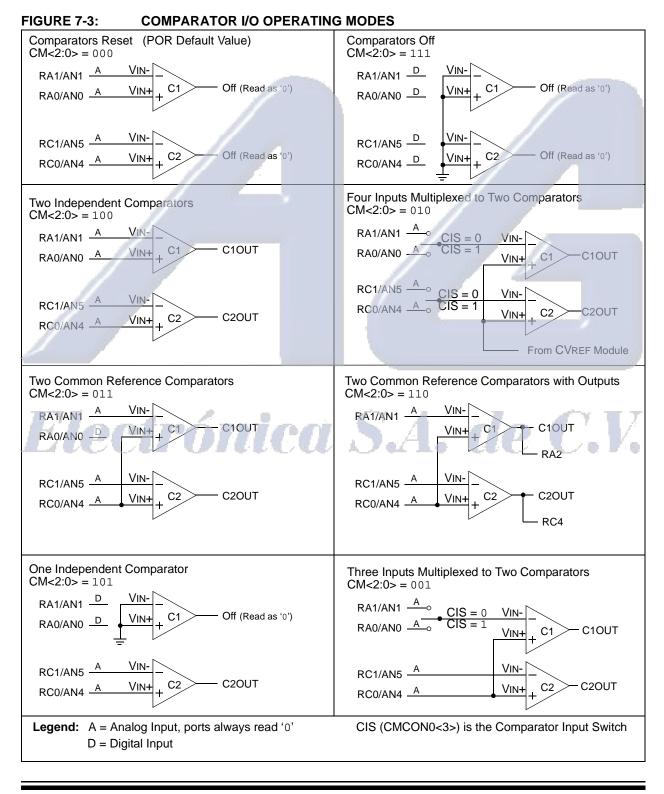
DS41203B-page 55

PIC16F688

7.3 Comparator Configuration

There are eight modes of operation for the comparators. The CMCON0 register is used to select these modes. Figure 7-3 shows the eight possible modes. If the Comparator mode is changed, the comparator output level may not be valid for the specified mode change delay shown in **Section 14.0 "Electrical Specifications**".

Note: Comparator interrupts should be disabled during a Comparator mode change. Otherwise, a false interrupt may occur.

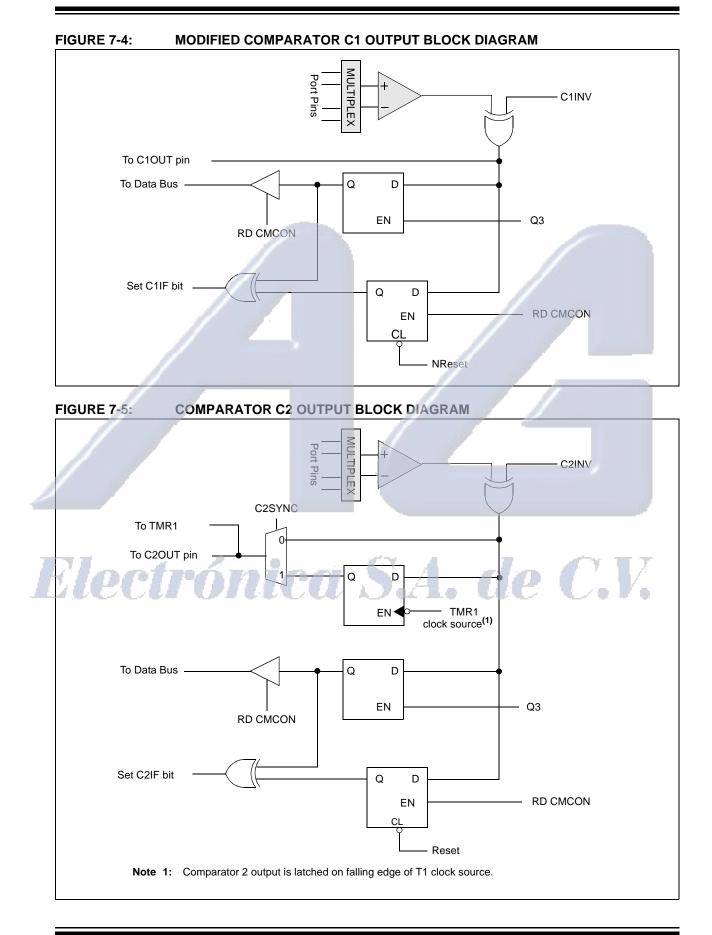


DS41203B-page 56

© 2004 Microchip Technology Inc.

www.agelectronica.com

PIC16F688



© 2004 Microchip Technology Inc.

Preliminary

DS41203B-page 57

www.agelectronica.com

PIC16F688

REGISTER 7-2:	CMCON1 – COMPARATOR CONFIGURATION REGISTER (ADDRESS: 1Ah)											
	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0				
	_				_		T1GSS	C2SYNC				
	bit 7							bit 0				
bit 7-2:	Unimplemented: Read as '0'											
bit 1	T1GSS: Tim	T1GSS: Timer1 Gate Source Select bit										
	1 = Timer1	gate sourc	e is T1G pir	n (RA4 must	t be configur	ed as digita	l input)					
	0 = Timer1	gate sourc	e is Compa	rator 2 Outp	out							
bit 0	C2SYNC: C	omparator	2 Synchroni	ze bit								
	1 = C2 out			•••		ock						
	0 = C2 out	put not syn	chronized w	ith Timer1 c	lock							
	Legend:											
	R = Readab	le bit	VV = VV	ritable bit	U = Unim	plemented	bit, read as	·O'				
	- n = Value a	at POR	'1' = Bi	t is set	'0' = Bit is	s cleared	x = Bit is u	Inknown				

7.4 Comparator Outputs

The comparator outputs are read through the CMCON0 register. These bits are read-only. The comparator outputs may also be directly output to the RA2 and RC4 I/O pins. When enabled, multiplexors in the output path of the RA2 and RC4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 7-4 and Figure 7-5 show the output block diagram for Comparator 1 and 2.

The TRIS bits will still function as an output enable/ disable for the RA2 and RC4 pins while in this mode.

The polarity of the comparator outputs can be changed using the C1INV and C2INV bits (CMCON0<5:4>).

Timer1 gate source can be configured to use the T1G pin or Comparator 2 output as selected by the T1GSS bit (CMCON1<1>). This feature can be used to time the duration or interval of analog events. The output of Comparator 2 can also be synchronized with Timer1 by setting the C2SYNC bit (CMCON1<0>). When enabled, the output of Comparator 2 is latched on the falling edge of Timer1 clock source. If a prescaler is used with Timer1, Comparator 2 is latched after the prescaler. To prevent a race condition, the Comparator 2 output is latched on the falling edge of the Timer1 increments on the rising edge of its clock source. See (Figure 7-5), Comparator 2 Block Diagram and (Figure 6-1), Timer1 Block Diagram for more information.

It is recommended to synchronize Comparator 2 with Timer1 by setting the C2SYNC bit when Comparator 2 is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if Comparator 2 changes during an increment.

7.5 Comparator Interrupts

The comparator interrupt flags are set whenever there is a change in the output value of its respective comparator. Software will need to maintain information about the status of the output bits, as read from CMCON0<7:6>, to determine the actual change that has occurred. The CxIF bits, PIR1<4:3>, are the Comparator Interrupt flags. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CxIE bits (PIE1<4:3>) and the PEIE bit (INTCON<6>) must be set to enable the interrupts. In addition, the GIE bit must also be set. If any of these bits are cleared, the interrupt is not enabled, though the CxIF bits will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of CMCON0. This will end the mismatch condition.
- b) Clear flag bit CxIF

A mismatch condition will continue to set flag bit CxIF. Reading CMCON0 will end the mismatch condition and allow flag bits CxIF to be cleared.

Note: If a change in the CMCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF (PIR1<3>) interrupt flag may not get set.

7.6 Comparator Reference

The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The VRCON register, Register 7-3, controls the voltage reference module shown in Figure 7-6.

7.6.1 CONFIGURING THE VOLTAGE REFERENCE

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range.

The following equation determines the output voltages:

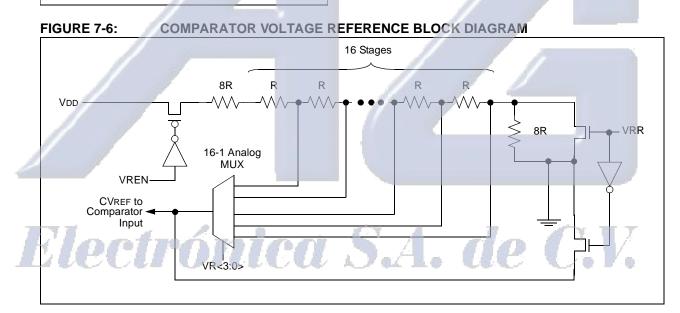
EQUATION 7-1:

VRR = 1 (low range): CVREF = (VR3:VR0/24) x VDD VRR = 0 (high range): CVREF = (VDD/4) + (VR3:VR0 x VDD/32)

7.6.2 VOLTAGE REFERENCE ACCURACY/ERROR

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 7-6) keep CVREF from approaching VSS or VDD. The exception is when the module is disabled by clearing the VREN bit (VRCON<7>). When disabled, the reference voltage is VSS when VR<3:0> = 0000. This allows the comparators to detect a zero-crossing and not consume CVREF module current.

The voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the comparator voltage reference can be found in **Section 14.0** "**Electrical Specifications**".



^{© 2004} Microchip Technology Inc.

7.7 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output is ensured to have a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (Table 14-9).

7.8 Operation During Sleep

The comparators and voltage reference, if enabled before entering Sleep mode, remain active during Sleep. This results in higher Sleep currents than shown in the power-down specifications. The additional current consumed by the comparator and the voltage reference is shown separately in the specifications. To minimize power consumption while in Sleep mode, turn off the comparator, CM<2:0> = 111, and voltage reference, VRCON<7> = 0.

While the comparator is enabled during Sleep, an interrupt will wake-up the device. If the GIE bit (INTCON<7>) is set, the device will jump to the interrupt vector (0004h), and if clear, continues execution with the next instruction. If the device wakes up from Sleep, the contents of the CMCON0, CMCON1 and VRCON registers are not affected.

7.9 Effects of a Reset

A device Reset forces the CMCON0, CMCON1 and VRCON registers to their Reset states. This forces the comparator module to be in the Comparator Reset mode, CM<2:0> = 000 and the voltage reference to its off state. Thus, all potential inputs are analog inputs with the comparator and voltage reference disabled to consume the smallest current possible.



Electrónica S.A. de C.V.

REGISTER 7-3:	VRCON-	VOLTAGE	REFEREN	ICE CONT	ROL REGI	STER (AD	DRESS: 99	9h)				
	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
	VREN		VRR	_	VR3	VR2	VR1	VR0				
	bit 7							bit 0				
bit 7		circuit powe	ered on	no IDD drain	and CVREF	= Vss.						
bit 6	Unimplem	Unimplemented: Read as '0'										
bit 5	VRR: CVRE	VRR: CVREF Range Selection bit										
	1 = Low rar											
	0 = High ra											
bit 4	Unimplem	ented: Rea	d as '0'									
bit 3-0	VR<3:0>: (VREF value	e selection 0	≤ VR<3:0>	•≤ 15							
			= (VR<3:0	,	-							
	When VRR	<u>= 0</u> : CVREF	= VDD/4 +	(VR<3:0>/32	2) * Vdd							
	Legend:	1				1	1					
	R = Reada	ble bit	VV = V	/ritable bit	U = Unin	nplemented	bit, read as	'O'				
	- n = Value at POR $(1)^2$ = Bit is set $(0)^2$ = Bit is cleared x = Bit is unknow											
TABLE 7-2: RE	GISTERS A	SSOCIAT	ED WITH	COMPAR	TOR MOD	ULE						
				/			Value on	Value on				

A	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
OE	3h/8Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	TOIF	INTF	RAIF	0000 0000	0000 0000
00	Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000 0000	0000 0000
19	9h	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
14	۹h	CMCON1	_	-	-	—	-	—	T1GSS	C2SYNC	10	10
85	5h/185h	TRISA	_		TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	11 1111	11 1111
87	7h/187h	TRISC	_	-	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	11 1111	11 1111
80	Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR11E	0000 0000	0000 0000
99	9h	VRCON	VREN		VRR	H.	VR3	VR2	VR1	VR0	0-0- 0000	0-0-0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the comparator or Comparator Voltage Reference module.

 $[\]circledast$ 2004 Microchip Technology Inc.

www.agelectronica.com

PIC16F688

NOTES:



Electrónica S.A. de C.V.

DS41203B-page 62

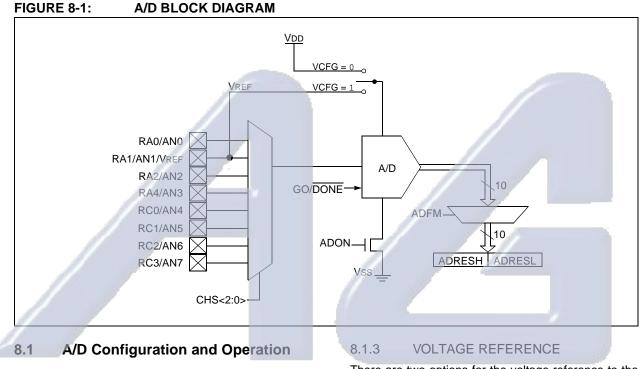
Preliminary

© 2004 Microchip Technology Inc.

www.agelectronica.com

8.0 ANALOG-TO-DIGITAL **CONVERTER (A/D) MODULE**

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a 10-bit binary representation of that signal. The PIC16F688 has eight analog inputs, multiplexed into one sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a binary result via successive approximation and stores the result in a 10-bit register. The voltage reference used in the conversion is software selectable to either VDD or a voltage applied by the VREF pin. Figure 8-1 shows the block diagram of the A/D on the PIC16F688.



There are three registers available to control the functionality of the A/D module:

```
1. ANSEL (Register 8-1)
```

ADCON0 (Register 8-2) 2. ADCON1 (Register 8-3) 3.

8.1.1 ANALOG PORT PINS

The ANS<7:0> bits (ANSEL<7:0>) and the TRIS bits control the operation of the A/D port pins. Set the corresponding TRIS bits to set the pin output driver to its high-impedance state. Likewise, set the corresponding ANSEL bit to disable the digital input buffer.

Note:	Analog voltages on any pin that is defined										
	as a digital input may cause the input										
	buffer to conduct excess current.										

8.1.2 CHANNEL SELECTION

There are eight analog channels on the PIC16F688. AN0 through AN7. The CHS<2:0> bits (ADCON0<4:2>) control which channel is connected to the sample and hold circuit.

There are two options for the voltage reference to the A/D converter: either VDD is used, or an analog voltage applied to VREF is used. The VCFG bit (ADCON0<6>) controls the voltage reference selection. If VCFG is set, then the voltage on the VREF pin is the reference; otherwise, VDD is the reference. 8.7

^{© 2004} Microchip Technology Inc.

For correct conversion, the A/D conversion clock (1/TAD) must be selected to ensure a minimum TAD of

1.6 μ s. Table 8-1 shows a few TAD calculations for

selected frequencies.

8.1.4 CONVERSION CLOCK

The A/D conversion cycle requires 11 TAD. The source of the conversion clock is software selectable via the ADCS bits (ADCON1<6:4>). There are seven possible clock options:

- Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- FRC (dedicated internal oscillator)

A/D Clock	Source (TAD)		Device F	Device Frequency							
Operation	ADCS<2:0>	20 MHz	5 MHz	4 MHz	1.25 MHz						
2 Tosc	000	100 ns ⁽²⁾	400 ns ⁽²⁾	500 ns ⁽²⁾	1.6 μs						
4 Tosc	100	200 ns ⁽²⁾	800 ns ⁽²⁾	1.0 μs ⁽²⁾	3.2 μs						
8 Tosc	001	400 ns ⁽²⁾	1.6 μs	2.0 μs	6.4 μs						
16 Tosc	101	800 ns ⁽²⁾	3.2 μs	4.0 μs	12.8 μs ⁽³⁾						
32 Tosc	010	1.6 μs	6.4 μs	8.0 μs ⁽³⁾	25.6 μs ⁽³⁾						
64 Tosc	110	3.2 μs	12.8 μs ⁽³⁾	16.0 μs <mark>(3)</mark>	51.2 μs ⁽³⁾						
A/D RC	x11	2-6 μs ^(1,4)	2-6 μs ^(1,4)	2-6 μs ^(1,4)	2-6 μs ^(1,4)						

TABLE 8-1: TAD VS. DEVICE OPERATING FREQUENCIES

Legend: Shaded cells are outside of recommended range.

Note 1: The A/D RC source has a typical TAD time of 4 μ s for VDD > 3.0V.

- 2: These values violate the minimum required TAD time.
- 3: For faster conversion times, the selection of another clock source is recommended.
- 4: When the device frequency is greater than 1 MHz, the A/D RC clock source is only recommended if the conversion will be performed during Sleep.

8.1.5 STARTING A CONVERSION

The <u>A/D</u> conversion is initiated by setting the GO/DONE bit (ADCON0<1>). When the conversion is complete, the A/D module:

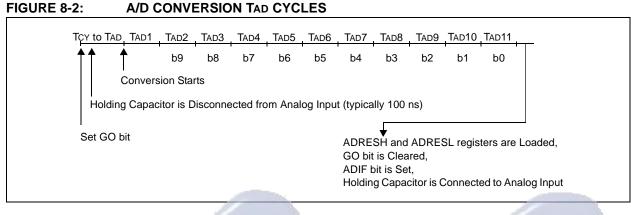
- Clears the GO/DONE bit
- Sets the ADIF flag (PIR1<6>)
- Generates an interrupt (if enabled)

If the conversion must be aborted, the GO/DONE bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete A/D conversion sample. Instead, the ADRESH:ADRESL registers will retain the value of the previous conversion. After an aborted conversion, a 2 TAD delay is required before another acquisition can be initiated. Following the delay, an input acquisition is automatically started on the selected channel.

Note: The GO/DONE bit should not be set in the same instruction that turns on the A/D.

DS41203B-page	64	
JOH IZUJD page	0-	

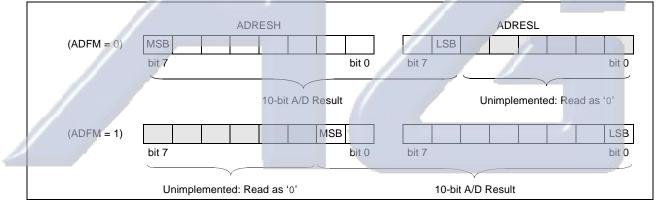
PIC16F688



8.1.6 CONVERSION OUTPUT

The A/D conversion can be supplied in two formats: left or right shifted. The ADFM bit (ADCON0<7>) controls the output format. Figure 8-3 shows the output formats.





REGISTER 8-1: ANSEL – ANALOG SELECT REGISTER (ADDRESS: 91h)									
T.IPTII	R/W-1	R/W-1	R/W-1	R/W-1 /-	R/W-1	RAW-1	R/W-1	R/W-1	
	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	
	bit 7							bit 0	

bit 7-0:

ANS<7:0>: Analog Select bits

Analog select between analog or digital function on pins AN<7:0>, respectively.

- 1 = Analog input. Pin is assigned as analog input.⁽¹⁾
- 0 = Digital I/O. Pin is assigned to port or special function.
 - **Note 1:** Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

```
© 2004 Microchip Technology Inc.
```

REGISTER 8-2:	ADCON0 -	A/D CON	FROL RE	GISTER (A	DDRESS:	: 1Fh)					
	R/W-0	R/W-0	U-0	R/W-0	R/W-0	, R/W-0	R/W-0	R/W-0			
	ADFM	VCFG	_	CHS2	CHS1	CHS0	GO/DONE	ADON			
	bit 7							bit 0			
bit 7	1 = Right ju		ned Select	bit							
hit G	0 = Left just		aa hit								
bit 6	1 = VREF pi 0 = VDD	age Referen n	ce dit								
bit 5	Unimpleme	ented: Read	as '0'								
bit 4-2	000 = Cha 001 = Cha 010 = Cha 011 = Cha 100 = Cha 101 = Cha 110 = Cha	Analog Cha nnel 00 (AN nnel 01 (AN nnel 02 (AN nnel 03 (AN nnel 04 (AN nnel 05 (AN nnel 06 (AN nnel 07 (AN	0) 1) 2) 3) 4) 5) 6)	t bits							
bit 1	1 = A/D cor This bit		e in progre ally cleare	ess. Setting t d by hardwa	re when the		nversion cycle ersion has com				
bit 0	1 = A/D cor	Conversion overter modu	le is opera		o operating c	current					
	Legend:										
	R = Readat	ole bit	VV = V	Vritable bit	U = Unir	nplemente	d bit, read as '0)'			
manufacture and	- n = Value	at POR	'1' = E	Bit is set	'0' = Bit	is cleared	x = Bit is un	known			
REGISTER 8-3:	ADCON1 - U-0 	A/D CONT R/W-0 ADCS2	R/W-0 ADCS1	GISTER 1 R/W-0 ADCS0	(ADDRES U-0 —	S: 9Fh) U-0 —	B <u>C</u> -	U-0 — bit 0			
bit 7	Unimpleme	ented: Read	as '0'								
bit 6-4	ADCS<2:0: 000 = Fos 001 = Fos 010 = Fos	A/D Conversion C/2 C/8 C/32 (clock deriversion C/4 C/16	ersion Cloo			ator = 500 l	(Hz max)				
bit 3-0	Unimpleme	ented: Read	as '0'								
	Legend:										
	R = Readat	ole bit	W = V	Vritable bit	U = Unir	nplemente	d bit, read as '0)'			
	- n = Value	at POR	'1' = E	Bit is set	'0' = Bit	is cleared	x = Bit is un	iknown			

DS41203B-page 66

© 2004 Microchip Technology Inc.

8.1.7 CONFIGURING THE A/D

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To determine sample time, see **Section 14.0 "Electrical Specifications"**. After this sample time has elapsed, the A/D conversion can be started.

These steps should be followed for an A/D conversion:

- 1. Configure the A/D module:
 - Configure analog/digital I/O (ANSEL)
 - Configure voltage reference (ADCON0)
 - Select A/D input channel (ADCON0)
 - Select A/D conversion clock (ADCON1)
 - Turn on A/D module (ADCON0)
- 2. Configure A/D interrupt (if desired):
 - Clear ADIF bit (PIR1<6>)
 - Set ADIE bit (PIE1<6>)
 - Set PEIE and GIE bits (INTCON<7:6>)
- 3. Wait the required acquisition time.
- 4. Start conversion:
 - Set GO/DONE bit (ADCON0<0>)
- 5. Wait for A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared (with interrupts disabled); OR
 Waiting for the A/D interrupt Read A/D Result register pair

(ADRESH:ADRESL), clear bit ADIF if required.

7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

EXAMPLE 8-1: A/D CONVERSION

;This c	ode block conf	igures the A/D								
;for polling, Vdd reference, R/C clock										
;and RA0 input.										
;										
;Conversion start & wait for complete										
;pollin	ng code include	ed.								
;										
BSF	STATUS, RPO	;Bank 1								
MOVLW	B'01110000'	;A/D RC clock								
MOVWF	ADCON1									
BSF	TRISA,0	;Set RAO to input								
BSF	ANSEL,0	;Set RA0 to analog								
BCF	STATUS, RPO	;Bank 0								
MOVLW	B'10000001'	;Right, Vdd Vref, AN0								
MOVWF	ADCON0									
CALL	SampleTime	;Wait min sample time								
BSF	ADCON0,GO	Start conversion								
BTFSC	ADCON0,GO 🧹	;Is conversion done?								
GOTO	\$-1	;No, test again								
MOVF	ADRESH,W	;Read upper 2 bits								
MOVWF	RESULTHI									
BSF	STATUS, RPO	;Bank 1								
MOVF	ADRESL,W	;Read lower 8 bits								
MOVWF	RESULTLO									

© 2004 Microchip Technology Inc.

8.2 A/D Acquisition Requirements

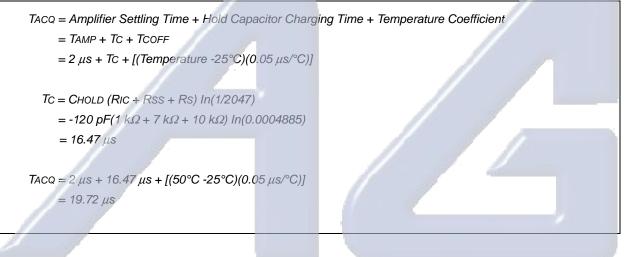
For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 8-4. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), see Figure 8-4. The maximum recommended impedance for analog sources is 10 k Ω .

As the impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 8-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, TACQ, see the "*PICmicro[®] Mid-Range MCU Family Reference Manual*" (DS33023).

EQUATION 8-1: ACQUISITION TIME

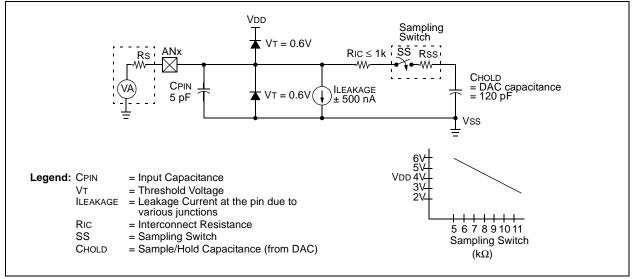


Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

FIGURE 8-4: ANALOG INPUT MODEL



DS41203B-page 68

© 2004 Microchip Technology Inc.

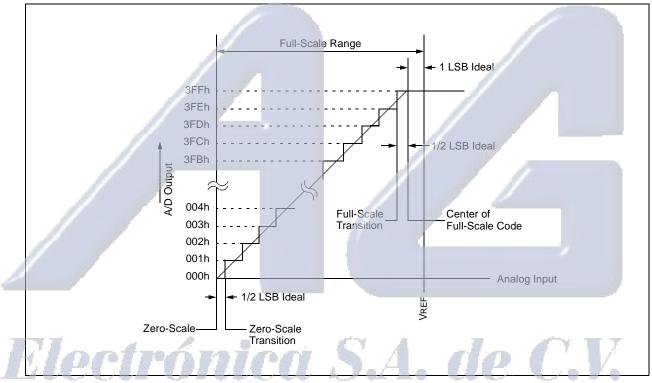
8.3 A/D Operation During Sleep

The A/D converter module can operate during Sleep. This requires the A/D clock source to be set to the internal oscillator. When the RC clock source is selected, the A/D waits one instruction before starting the conversion. This allows the SLEEP instruction to be executed, thus eliminating much of the switching noise from the conversion. When the conversion is complete, the GO/DONE bit is cleared and the result is loaded into the ADRESH:ADRESL registers. If the A/D

FIGURE 8-5: A/D TRANSFER FUNCTION

interrupt is enabled, the device awakens from Sleep. If the GIE bit (INTCON<7>) is set, the program counter is set to the interrupt vector (0004h), if GIE is clear, the next instruction is executed. If the A/D interrupt is not enabled, the A/D module is turned off, although the ADON bit remains set.

When the A/D clock source is something other than RC, a SLEEP instruction causes the present conversion to be aborted, and the A/D module is turned off. The ADON bit remains set.



^{© 2004} Microchip Technology Inc.

PIC16F688

8.4 **Effects of Reset**

A device Reset forces all registers to their Reset state. Thus, the A/D module is turned off and any pending conversion is aborted. The ADRESH:ADRESL registers are unchanged.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD	Value on all other Resets
05h/ 105h	PORTA	—	-	RA5	RA4	RA3	RA2	RA1	RA0	xx xxxx	uu uuuu
07h/ 107h	PORTC	—	-	RC5	RC4	RC3	RC2	RC1	RC0	xx xxxx	uu uuuu
0Bh/ 8Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000 0000	0000 0000
1Eh	ADRESH	Most Signifi	cant 8 bits of	the left shifte	ed A/D result	or 2 bits <mark>of th</mark>	e right shifted	l result		XXXX XXXX	uuuu uuuu
1Fh	ADCON0	ADFM	VCFG		CHS2	CHS1	CHS0	GO/DONE	ADON	00-0 0000	00-0 0000
85h/ 185h	TRISA	—	1	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	11 1111	11 1111
87h/ 187h	TRISC	-/		TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	11 1111	11 1111
8Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE	0000 0000	0000 0000
91h	ANSEL	ANS7	ANS6	ANS5	ANS4	ANS <mark>3</mark>	ANS2	ANS1	ANS0	1111 1111	1111 1111
9Eh	ADRESL	SL Least Significant 2 bits of the left shifted A/D result or 8 bits of the right shifted result									uuuu uuuu
9Fh	ADCON1	- /	ADCS2	ADCS1	ADCS0	—		- 34	_	-000	-000
Legend: $x = unknown u = unknowed - = unimplemented read as '0'. Shaded cells are not used for A/D module$											

TABLE 8-2: SUMMARY OF A/D REGISTERS

Legend: = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D module.

Electrónica S.A. de C.V.

9.0 DATA EEPROM AND FLASH PROGRAM MEMORY CONTROL

Data EEPROM memory is readable and writable and the Flash program memory is readable during normal operation (full VDD range). These memories are not directly mapped in the register file space. Instead, they are indirectly addressed through the Special Function Registers. There are six SFRs used to access these memories:

- EECON1
- EECON2
- EEDAT
- EEDATH
- EEADR
- EEADRH

When interfacing the data memory block, EEDAT holds the 8-bit data for read/write, and EEADR holds the address of the EE data location being accessed. This device has 256 bytes of data EEPROM with an address range from 0h to 0FFh.

When interfacing the program memory block, the EEDAT and EEDATH registers form a 2-byte word that holds the 14-bit data for read/write, and the EEADR and EEADRH registers form a 2-byte word that holds the 12-bit address of the EEPROM location being accessed. This device has 4K words of program EEPROM with an address range from 0h to 0FFFh. The program memory allows one word reads.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

When the device is code-protected, the CPU may continue to read and write the data EEPROM memory and read the program memory. When code-protected, the device programmer can no longer access data or program memory.

Additional information on the data EEPROM is available in the "*PICmicro[®] Mid-Range MCU Family Reference Manual*" (DS33023).

9.1 EEADR and EEADRH Registers

The EEADR and EEADRH registers can address up to a maximum of 256 bytes of data EEPROM or up to a maximum of 4K words of program EEPROM.

When selecting a program address value, the MSB of the address is written to the EEADRH register and the LSB is written to the EEADR register. When selecting a data address value, only the LSB of the address is written to the EEADR register.

9.1.1 EECON1 AND EECON2 REGISTERS

EECON1 is the control register for EE memory accesses.

Control bit EEPGD determines if the access will be a program or data memory access. When clear, as it is when reset, any subsequent operations will operate on the data memory. When set, any subsequent operations will operate on the program memory. Program memory can only be read.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation to data EEPROM. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and rewrite the location. The data and address will be unchanged in the EEDAT and EEADR registers.

Interrupt flag bit EEIF (PIR1<7>), is set when write is complete. It must be cleared in the software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence.

www.agelectronica.com PIC16F688

REGISTER 9-1:	EEDAT – EEPROM D					D AA4 o
	R/W-0 R/W-0	R/W-0 R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEDAT7 EEDAT6 bit 7	EEDAT5 EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0 bit 0
bit 7-0	EEDATn: Byte Value to W	rite to or Read From Data	EEPROM bits			
	Legend:]
	R = Readable bit	W = Writable bit	II – Unimpl	emented bit,	read as 'O'	
	n = Value at POR	'1' = Bit is set	0' = Bit is c		x = Bit is un	known
REGISTER 9-2:	EEADR – EEPRON R/W-0 R/W-0	ADDRESS REGIST	FER (ADDRI	E SS: 9Bh) _{R/W-0}	R/W-0	R/W-0
	EEADR7 EEADR6	EEADR5 EEADR4	EEADR3	EEADR2	EEADR1	EEADR0
	bit 7	EEADR3 EEADR4	EEADRS		EEADRI	bit 0
bit 7-0	EEADR: Specifies One of	256 Locations for EEPRC	M Read/Write	Operation bits	,	
	Legend:					
	R = Readable bit	W = Writable bit	U = Unimpl	emented bit, I	read as '0'	
	- n = Value at POR	'1' = Bit is set	'0' = Bit is c		x = Bit is un	known
REGISTER 9-3:	EECON1 - EEPROM	CONTROL REGIST	ER 1 (ADDF	RESS: 9Ch	1)	
	R/W-0 U-0	U-0 U-0	R/W-x	R/W-0	R/S-0	R/S-0
	EEPGD — bit 7		WRERR	WREN	WR	RD bit 0
bit 7	EEPGD: Program/Data EB 1 = Accesses program m 0 = Accesses data memo	emory				
bit 6-4	Unimplemented: Read as	s '0'		100	_	
bit 3	WRERR: EEPROM Error 1 = A write operation is p normal operation or E 0 = The write operation or	rematurely terminated (an 3OD detect)	y MCLR Reset,	any WDT Re	eset during	· V.
bit 2	WREN: EEPROM Write E 1 = Allows write cycles 0 = Inhibits write to the dat					
bit 1	<pre>WR: Write Control bit <u>EEPGD = 1</u>: This bit is ignored <u>EEPGD = 0</u>: 1 = Initiates a write cycle set, not cleared, in so 0 = Write cycle to the dat</pre>	oftware.)	dware once writ	e is complete	. The WR bit	can only be
bit 0	 RD: Read Control bit 1 = Initiates an memory r set, not cleared, in so 0 = Does not initiate an n 	ead (Read takes one cycl ftware.)	le. RD is cleare	d in hardware	e. The RD bit	can only be
	Legend: S = Bit can only be set					
	R = Readable bit	W = Writable bit	U = Unimpl	emented bit,	read as '0'	
	- n = Value at POR	'1' = Bit is set	'0' = Bit is c		x = Bit is un	known
]

DS41203B-page 72

Preliminary

© 2004 Microchip Technology Inc.

EVANDLE O

9.1.2 READING THE DATA EEPROM MEMORY

To read a data memory location, the user must write the address to the EEADR register, clear the EEPGD control bit (EECON1<7>), and then set control bit RD (EECON1<0>). The data is available in the very next cycle, in the EEDAT register; therefore, it can be read in the next instruction. EEDAT will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 9-1:	DATA EEPROM READ

BSF	STATUS, RPO	;
BCF	STATUS, RP1	; Bank 1
MOVLW	DATA_EE_ADDR	;
MOVWF	EEADR	; Data Memory
		; Address to read
BCF	EECON1, EEPGD	; Point to DATA
		; memory
BSF	EECON1, RD	; EE Read
MOVF	EEDAT, W ;	; W = EEDAT

9.1.3 WRITING TO THE DATA EEPROM MEMORY

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDAT register. Then the user must follow a specific sequence to initiate the write for each byte.

The write will not initiate if the above sequence is not followed exactly (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. Interrupts should be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

	BSF	STATUS, RPO	,
	BCF	STATUS, RP1	; Bank 1
	MOVLW	DATA_EE_ADDR	;
	MOVWF	EEADR	; Data Memory Address to write
	MOVLW	DATA_EE_DATA	;
	MOVWF	EEDAT	; Data Memory Value to write
-	BCF	EECON1, EEPG	D ; Point to DATA memory
17	BSF	EECON1, WREN	; Enable writes
	BCF	INTCON, GIE	; Disable INTs. LJQL LO USU VOJO
τe	MOVLW	55h	;
Required Sequence	MOVWF	EECON2	; Write 55h
edr	MOVLW	AAh	;
чv	MOVWF	EECON2	; Write AAh
	BSF	EECON1, WR	; Set WR bit to begin write
	BSF	INTCON, GIE	; Enable INTs.
	SLEEP		; Wait for interrupt to signal write complete
	BCF	EECON1, WREN	; Disable writes

9.1.4 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must write two bytes of the address to the EEADR and EEADRH registers, set the EEPGD control bit (EECON1<7>), and then set control bit RD (EECON1<0>). Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the "BSF EECON1, RD" instruction to be ignored. The data is available in the very next cycle, in the EEDAT and EEDATH registers; therefore, it can be read as two bytes in the following instructions.

EXAMPLE 9-3: FLASH PROGRAM READ

EEDAT and EEDATH registers will hold this value until another read or until it is written to by the user (during a write operation).

- Note 1: The two instructions following a program memory read are required to be NOP's. This prevents the user from executing a two-cycle instruction on the next instruction after the RD bit is set.
 - If the WR bit is set when EEPGD = 1, it will be immediately reset to '0' and no operation will take place.

	BSF	STATUS, RPO	;	
	BCF	STATUS, RP1	;	Bank 1
	MOVLW	MS_PROG_EE_ADDR	;	
	MOVWF	EEADRH	;	MS Byte of Program Address to read
	MOVLW	LS_PROG_EE_ADDR	;	
	MOVWF	EEADR	;	LS Byte of Program Address to read
	BSF	EECON1, EEPGD	;	Point to PROGRAM memory
	BSF	EECON1, RD	;	EE Read
;				
			;	First instruction after BSF EECON1, RD executes normally
	NOP			
	NOP		;	Any instructions here are ignored as program
			;	memory is read in second cycle after BSF EECON1,RD
;				
	MOVF	EEDAT, W	;	W = LS Byte of Program EEDAT
	MOVF	EEDATH, W	;	W = MS Byte of Program EEDAT
	1			

Electrónica S.A. de C.V.

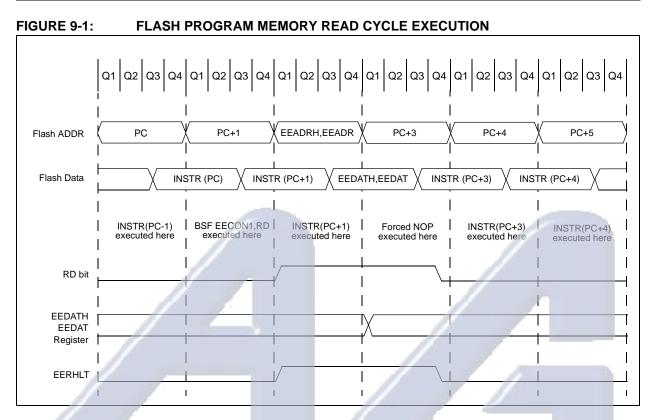


TABLE 9-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

	Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
	0Bh/8Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	TOIF	INTF	RAIF	0000 0000	0000 0000
	0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000 0000	0000 0000
	8Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE	0000 0000	0000 0000
	97h	EEDATH	EEPROM Data register, high byte									
	98h	EEADRH	EEPROM	Address r	egister, hi	gh byte		A	6	D.	0000	0000 0000
	9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
	9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
	9Ch	EECON1	EEPGD		_	_	WRERR	WREN	WR	RD	x000	d000
	9Dh	EECON2 ⁽¹⁾	_	_		_	_	_	_	_		—

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by data EEPROM module.

Note 1: EECON2 is not a physical register.

www.agelectronica.com

PIC16F688

NOTES:



Electrónica S.A. de C.V.

DS41203B-page 76

Preliminary

© 2004 Microchip Technology Inc.

www.agelectronica.com

10.0 ENHANCED UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is the serial I/O module available for PIC16F688 . (EUSART is also known as a Serial Communications Interface or SCI). The EUSART can be configured as a full-duplex asynchronous system that can communicate with peripheral devices, such as CRT terminals and personal computers. It can also be configured as a half-duplex synchronous system that can communicate with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs, etc.

The EUSART module implements additional features, including automatic baud rate detection and calibration, automatic wake-up on Break reception and 13-bit Break character transmit. These make it ideally suited for use in Local Interconnect Network (LIN) bus systems.

The USART can be configured in the following modes:

- Asynchronous (full-duplex) with:
 - Auto-wake-up on Break
 - Auto baud calibration
 - 13-bit Break character transmission
- Synchronous Master (half-duplex) with selectable clock polarity
- Synchronous Slave (half-duplex) with selectable clock polarity

In order to configure pins RC4/C2OUT/TX/CK and RC5/RX/DT as the Universal Synchronous Asynchronous Receiver Transmitter:

- SPEN (RCSTA<7>) bit must be set (= 1),
- TRISC<5> bit must be set (= 1), and
- TRISC<4> bit must be set (= 1).

Note: The USART control will automatically reconfigure the pin from input to output as needed.

The operation of the EUSART module is controlled through three registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)
- Baud Rate Control (BAUDCTL)

These are detailed in on the following pages in Register 10-1, Register 10-2 and Register 10-3, respectively.

10.1 Clock Accuracy With Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC) for 8 MHz. However, this frequency may drift as VDD or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output back to 8 MHz. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source (see **Section 3.4** "Internal Clock Modes" for more information).

The other method adjusts the value in the baud rate generator. There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.



S.A. de C.V.

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0			
	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D			
	bit 7							bit 0			
h.:4	7	a alv Cauraa C	Valaat hit								
bit		ock Source S	Select Dit								
		Asynchronous mode:									
	Don't care Synchrone										
		r mode (cloci	c apparatad	internally fre	m BRG)						
		mode (clock			Jin Bree)						
bit	6 TX9: 9-bit	Transmit En	able bit								
	1 = Select	s 9-bit transn	nission								
	0 = Select	s 8-bit transn	nission								
bit	5 TXEN: Tra	ansmit Enable	e bit								
		mit enabled	1								
	0 = Transı	nit disabled									
	Note:	SREN/CRE	N overrides	STXEN in Sy	/nc mode.						
bit	4 SYNC: US	SART Mode S	Select bit				1				
		ronous mode									
	0 = Async	hronous mod	le					,			
bit	3 SENDB: S	Send Break C	Character bit								
	1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1	nous mode:				1 4					
		Sync Break c			ared by har	dware upon	completion)				
	-	Break transm	ission comp	oleted							
	Synchrone Don't care										
hit			• Coloct bit								
bit		gh Baud Rate	e Select bit					34			
	1 = High s	nous mode:									
	0 = Low s										
11 Y 1		ous mode:		101			1	Y TT			
	Unused in	this mode	ഹ		- 4	684	<u> </u>	· / /			
bit	1 TRMT: Tra	ansmit Shift F	Register Stat	tus bit	K Lø		2. 0	(.			
	1 = TSR e										
	0 = TSR f										
bit	0 TX9D: 9th	bit of Transr	nit Data								
	Can be ac	ldress/data b	it or a parity	bit.							
	Legend:										
	R = Read	able bit		/ritable bit	U = Unim	plemented	bit, read as	ʻ0'			

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

 $\ensuremath{\textcircled{}^{\circ}}$ 2004 Microchip Technology Inc.

x = Bit is unknown

		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x		
		SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D		
		bit 7							bit 0		
	bit 7	SPEN: Ser	ial Port Enal	ble bit							
			oort enabled			TX/CK pins a	as serial po	ort pins)			
	bit 6	-	Receive Ena	-							
		1 = Selects 9-bit reception 0 = Selects 8-bit reception									
	bit 5	SREN: Sin	gle Receive	Enable bit							
		Asynchrone	-								
		Don't care									
		Synchrono	us mode - N	laster:							
		1 = Enable	s single rece	eive							
			es single rec								
			leared after		complete.			1			
		Don't care	us mode - S	lave:			1		1.11		
	1. 1. A			anian English	- 1-14		1				
	bit 4		ntinuous Re	ceive Enable	e dit				1		
		Asynchron									
		1 = Enable 0 = Disable									
		Synchrono									
				s receive un	til enable bit	CREN is cle	ared (CRE	N overrides	SREN)		
	1		es continuou						OREN		
	bit 3	ADDEN: A	ddress Dete	ct Enable b	it						
		Asynchronous mode 9-bit (RX9 = 1):									
		1 = Enables address detection, enable interrupt and load the receive buffer when RSR<8 set									
						eceived and r	hinth bit car	he used as	parity bit		
	PT.		o <u>us mode 8-</u>	<u>bit (RX9 = (</u>	<u>)</u> :						
uvc		Don't care			∪ «Ľ	lo U			N . 👷 👘		
	bit 2	FERR: Fra	ming Error b	oit							
		1 = Framing error (can be updated by reading RCREG register and receive next valid byte)									
		0 = No fran	-								
	bit 1		errun Error b								
		1 = Overrun error (can be cleared by clearing bit CREN)									
		0 = No overrun error									
	bit 0		bit of Receiv								
		This can be	e address/da	ata bit or a p	arity bit and	must be calc	ulated by u	iser firmware	Э.		
		Legend:									
		R = Reada	ble bit	W = W	/ritable bit	U = Unim	plemented	bit, read as	'0'		

 $\ensuremath{\textcircled{}^{\circ}}$ 2004 Microchip Technology Inc.

REGISTER 10-3:	BAUDCTL	– BAUD F		ITROL REG	GISTER (A	DDRESS	: 11h)	
	R-0	R-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN
	bit 7							bit 0
bit 7	ABDOVF: /	Auto Baud D	Detect Over	flow bit				
		aud timer ov aud timer dic		w				
bit 6	RCIDL: Red	ceive IDLE	Flag bit					
	Asynchrono 1 = Receive 0 = Start bit <u>Synchrono</u> Don't care	er is IDLE t has been r	eceived and	the receive	r is receiving	3		
bit 5	Unimpleme	ented: Read	d as '0'					
bit 4	SCKP: Syn	chronous C	lock Polarity	/ Select bit				
		iit pin TX iit pin TX <u>us mode</u> : clocked on		of the clock				
bit 3	BRG16: 16	bit Baud R	ate Generat	or bit				
		aud rate ge uud rate gen						
bit 2	Unimpleme	ented: Read	d as '0'					1
bit 1	WUE: Wake	e-up Enable	e bit					
B bit 0	after fa 0 = RX/DT ABDEN: Au Asynchrono	lling edge) edges do no uto Baud De <u>ous mode</u> :	ot generate etect Enable	bit 💭 💧	Å.	de	B	rising edge
				lears when a	uto baud is	complete)		
	0 = Auto Ba Synchronou	aud mode is us mode:	disabled					
	Don't care	<u>us mous</u> .						
	Legend:							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

DS41203B-page 80

10.2 USART Baud Rate Generator (BRG)

The BRG is a dedicated 8-bit or 16-bit generator, that supports both the Asynchronous and Synchronous modes of the USART. By default, the BRG operates in 8-bit mode; setting the BRG16 bit (BAUDCTL<3>) selects 16-bit mode.

The SPBRGH:SPBRG register pair controls the period of a free running timer. In Asynchronous mode, bits BRGH (TXSTA<2>) and BRG16 also control the baud rate. In Synchronous mode, bit BRGH is ignored. Table 10-1 shows the formula for computation of the baud rate for different USART modes, which only apply in Master mode (internally generated clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRGH:SPBRG registers can be calculated using the formulas in Table 10-1. From this, the error in baud rate can be determined. An example calculation is shown in Example 10-1. Typical baud rates and error values for the various asynchronous modes are shown in Table 10-2. It may be advantageous to use the high baud rate (BRGH = 1), or the 16-bit BRG to reduce the baud rate error, or achieve a slow baud rate for a fast oscillator frequency.

Writing a new value to the SPBRGH:SPBRG registers causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

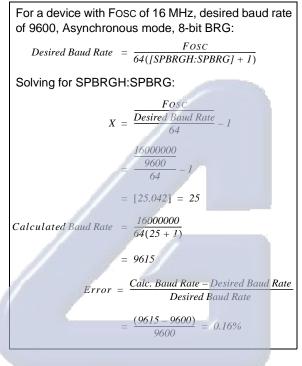
If the system clock is changed during an active receive operation, a receive error or data loss may result. To avoid this problem, check the status of the RCIDL bit and make sure that the receive operation is IDLE before changing the system clock.

TABLE 10-1: BAUD RATE FORMULAS

10.2.1 SAMPLING

The data on the RC5/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin.

EXAMPLE 10-1: CALCULATING BAUD RATE ERROR



Note: When BRGH = 1 and BRG16 = 1 then SPBRGH:SPBRG values ≤ 4 are invalid.

	Configuration Bi	ts		Baud Rate Formula		
SYNC	BRG16	BRGH	BRG/USART Mode			
0	0	0	8-bit/Asynchronous	Fosc/[64 (n+1)]		
0	0	1	8-bit/Asynchronous			
0	1	0	16-bit/Asynchronous	Fosc/[16 (n+1)]		
0	1	1	16-bit/Asynchronous			
1	0	x	8-bit/Synchronous	Fosc/[4 (n+1)]		
1	1	х	16-bit/Synchronous			

Legend:

www.agelectronica.com

x = Don't care, n = value of SPBRGH:SPBRG register pair

TABLE 10-2:	REGISTER	S ASSO	DCIATE	D WITH	BAUD	RATE G	ENERA	TOR	

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD	Value on all other Resets
11h	BAUDCTL	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	-1-1 0-00	-1-1 0-00
12h	SPBRGH		E	Baud Rate	Generato	r register,	high byte			0000 0000	0000 0000
13h	SPBRG		E	Baud Rate	Generato	or register,	low byte			0000 0000	0000 0000
16h	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 -010	0000 -010
17h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

TABLE 10-3:	BAUD RATES FOR	ASYNCHRONOUS MODES	;

			S	YNC = 0, E	BRGH = 0	, BRG1 <mark>6 =</mark>	0		
BAUD RATE	Fosc = 20.000 MHz) MHz	Fosc	= 10.000	MHz	Fosc = 8.000 MHz		
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	- /	2-		_	_		—	1/-
1.2	1.221	1.73	255	1.202	0.16	129	1201	-0.16	103
2.4	2.404	0.16	129	2.404	0.16	64	2403	-0.16	51
9.6	9.766	1.73	31	9.766	1.73	15	9615	-0.16	12
19.2	19.531	1.73	15	19.531	1.73	7	_//	<u> </u>	1-
57.6	62.500	8.51	4	52.083	- 9.58	2	H		/ _
115.2	104.167	-9.58	2	78.125	-3 2.18	1	14	_/	—

1	1		S	YNC = 0, I	BRGH = (), BRG1 <mark>6 =</mark>	0				
BAUD	Fos	c = 4.000	MHz	Fosc = 2.000 MHz			Fos	Fosc = 1.000 MHz			
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)		~ = -
0.3	0.300	0.16	207	300	-0.16	103	300	-0.16	51		
1.2	1.202	0.16	51	1201	-0.16	25	1201	-0.16	12	E.	Ny a Ma
2.4	2.404	0.16	25	2403	-0.16	12	—	_	_		
9.6	8.929	-6.99	6	—	—	—	—	—	—		
19.2	20.833	8.51	2	—	—	—	—	—	—		
57.6	62.500	8.51	0	—	—	—	—	—	_		
115.2	62.500	-45.75	0	_	—	—	—	—	—		

	SYNC = 0, BRGH = 1, BRG16 = 0									
BAUD RATE	Fosc = 20.000 MHz			Fosc	= 10.000	0 MHz	Fosc = 8.000 MHz			
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	
2.4	—			2.441	1.73	255	2403	-0.16	207	
9.6	9.615	0.16	129	9.615	0.16	64	9615	-0.16	51	
19.2	19.231	0.16	64	19.531	1.73	31	19230	-0.16	25	
57.6	56.818	-1.36	21	56.818	-1.36	10	55555	3.55	8	
115.2	113.636	-1.36	10	125.000	8.51	4	_	—	—	

DS41203B-page 82

			S	YNC = 0, E	BRGH = 1	, BRG16 =	0			
BAUD RATE	Foso	c = 4.000	MHz	Fos	c = 2.000	MHz	Fosc = 1.000 MHz			
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	
0.3				_	_		300	-0.16	207	
1.2	1.202	0.16	207	1201	-0.16	103	1201	-0.16	51	
2.4	2.404	0.16	103	2403	-0.16	51	2403	-0.16	25	
9.6	9.615	0.16	25	9615	-0.16	12	_	—	_	
19.2	19.231	0.16	12	—	_	_	_	—	_	
57.6	62.500	8.51	3	_	-	_	_	_	_	
115.2	125.000	8.51	1	H	_		_	—	—	

TABLE 10-3: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

		SYNC = 0, BRGH = 0, BRG16 = 1												
BAUD	Fosc = 20.000 MHz			Fos	c = 10.000	MHz	Fosc = 8.000 MHz							
RATE (K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)					
0.3	0.300	0.02	4165	0.300	0.02	2082	300	-0.04	1665					
1.2	1.200	-0.03	1041	1.200	-0.03	520	1201	-0.16	415					
2.4	2.399	-0.03	520	2.404	0.16	259	2403	-0.16	207					
9.6	9.615	0.16	129	9.615	0.16	64	9615	-0.16	51					
19.2	19.231	0.16	64	19.531	1.73	31	19230	-0.16	25					
57.6	56.818	-1.36	21	56.818	-1.36	10	55555	3.55	8					
115.2	113.636	-1.36	10	125.000	8.51	4	_	200-	_					

	and a second		S	YNC = 0,	BRGH = 0	, BRG16 =	1		
BAUD RATE	Fos	c = 4.000	MHz	Fo	sc = 2.000	MHz	Fos	c = 1.000) MHz
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3 1.2	0.300	0.04 0.16	832 207	300 1201	-0.16 -0.16	415 103	300 1201	-0.16 -0.16	207 51
2.4	2.404	0.16	103	2403	-0.16	51	2403	-0.16	25
9.6 19.2	9.615 19.231	0.16 0.16	25 12	9615	-0.16	12	—	—	_
19.2 57.6	62.500	0.16 8.51	3	_	_	_	_	_	_
115.2	125.000	8.51	1	—	_	_	—	—	_

		SYN	NC = 0, BR	GH = 1, BF	RG16 = 1	or SYNC =	= 1, BRG16	δ = 1		
BAUD RATE	Fosc	= 20.000) MHz	Fosc	= 10.000) MHz	Fosc = 8.000 MHz			
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	
0.3	0.300	0.00	16665	0.300	0.00	8332	300	-0.01	6665	
1.2	1.200	0.02	4165	1.200	0.02	2082	1200	-0.04	1665	
2.4	2.400	0.02	2082	2.402	0.06	1040	2400	-0.04	832	
9.6	9.596	-0.03	520	9.615	0.16	259	9615	-0.16	207	
19.2	19.231	0.16	259	19.231	0.16	129	19230	-0.16	103	
57.6	57.471	-0.22	86	58.140	0.94	42	57142	0.79	34	
115.2	116.279	0.94	42	113.636	-1.36	21	117647	-2.12	16	

© 2004 Microchip Technology Inc.

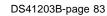


TABLE 10-3: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

		SYN	NC = 0, BR	GH = 1, BI	RG16 = 1	or SYNC =	1, BRG1	6 = 1		
BAUD	Fos	c = 4.000	MHz	Fos	c = 2.000	MHz	Fosc = 1.000 MHz			
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	
0.3	0.300	0.01	3332	300	-0.04	1665	300	-0.04	832	
1.2	1.200	0.04	832	1201	-0.16	415	1201	-0.16	207	
2.4	2.404	0.16	415	2403	-0.16	207	2403	-0.16	103	
9.6	9.615	0.16	103	9615	-0.16	51	9615	-0.16	25	
19.2	19.231	0.16	51	19230	-0.16	25	19230	-0.16	12	
57.6	58.824	2.12	16	55555	3.55	8	—	_	_	
115.2	111.111	-3.55	8			-	_	—	—	

10.2.2 AUTO BAUD RATE DETECT

The EUSART module supports the automatic detection and calibration of baud rate. This feature is active only in Asynchronous mode and while the WUE bit is clear.

The automatic baud rate measurement sequence (Figure 10-1) begins whenever a Start bit is received and the ABDEN bit is set. The calculation is selfaveraging.

In the Auto Baud Rate Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. In ABD mode, the internal baud rate generator is used as a counter to time the bit period of the incoming serial byte stream.

Once the ABDEN bit is set, the state machine will clear the BRG and look for a Start bit. The Auto Baud Detect must receive a byte with the value 55h (ASCII "U", which is also the LIN bus sync character), in order to calculate the proper bit rate. The measurement takes over both a low and a high bit time in order to minimize any effects caused by asymmetry of the incoming signal. After a Start bit, the SPBRG begins counting up using the preselected clock source on the first rising edge of RX. After eight bits on the RX pin, or the fifth rising edge, an accumulated value totalling the proper BRG period is left in the SPBRGH:SPBRG registers. Once the 5th edge is seen (should correspond to the Stop bit), the ABDEN bit is automatically cleared.

While calibrating the baud rate period, the BRG registers are clocked at 1/8th the pre-configured clock rate. Note that the BRG clock will be configured by the BRG16 and BRGH bits. Independent of the BRG16 bit setting, both the SPBRG and SPBRGH will be used as a 16-bit counter. This allows the user to verify that no carry occurred for 8-bit modes, by checking for 00h in the SPBRGH register. Refer to Table 10-4 for counter clock rates to the BRG.

While the ABD sequence takes place, the USART state machine is held in IDLE. The RCIF interrupt is set once the fifth rising edge on RX is detected. The value in the RCREG needs to be read to clear the RCIF interrupt. RCREG content should be discarded.

Note 1:	If the WUE bit is set with the ABDEN bit, auto baud rate detection will occur on the
1	
	byte following the Break character (see
100	Section 10.3.4 "Auto-Wake-up on
	SYNC Break Character").
2:	It is up to the user to determine that the
	incoming character baud rate is within the
	range of the selected BRG clock source.
	Some combinations of oscillator
	frequency and USART baud rates are not
	possible due to bit error rates. Overall
	•
	system timing and communication baud
17 Y	rates must be taken into consideration
	when using the Auto Baud Rate Detection
The second se	feature.

TABLE 10-4: BRG COUNTER CLOCK RATES

BRG16	BRGH	BRG Counter Clock
0	0	Fosc/512
0	1	Fosc/128
1	0	Fosc/128
1	1	Fosc/32

Note: During the ABD sequence, SPBRG and SPBRGH are both used as a 16-bit counter, independent of BRG16 setting.

	-I. AU		KAIL C	ALCOLA				
BRG Value	XXXXh	0000h						001Ch
RX pin		Start	Bit 0 Bit	Edge #	Edge Bit 3 Bit 4		7 1	Edge #5 op Bit
BRG Clock		İmmunun	, MUUUU	www	സസസ	տուրու	านที่เหตุ่	
	Set by User —	1	1					- Auto Cleared
ABDEN bit			I					
RCIDL		1	1					
		:	• •				i	
RCIF bit (Interrupt)								
								(
Read RCREG			1					
SPBRG		- //	XXXXh					1Ch
SPBRG								топ
SPBRGH			XXXXh					00h
Note 1	I: The ABD sequ	ience requires the USAF	T module to	be configured	in Asynchron	ous mode and W	/UE = 0.	
						1	1	

FIGURE 10-1: AUTOMATIC BAUD RATE CALCULATION

Electrónica S.A. de C.V.

10.3 USART Asynchronous Mode

The Asynchronous mode of operation is selected by clearing the SYNC bit (TXSTA<4>). In this mode, the USART uses standard non-return-to-zero (NRZ) format (one Start bit, eight or nine data bits and one Stop bit). The most common data format is 8 bits. An on-chip dedicated 8-bit/16-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator.

The USART transmits and receives the LSb first. The USART's transmitter and receiver are functionally independent, but use the same data format and baud rate. The baud rate generator produces a clock, either x16 or x64 of the bit shift rate, depending on the BRGH and BRG16 bits (TXSTA<2> and BAUDCTL<3>). Parity is not supported by the hardware, but can be implemented in software and stored as the 9th data bit.

Asynchronous mode is available in all times. It is available in Sleep mode only when auto-wake-up on Sync Break is enabled. The baud rate generator values may need to be adjusted if the clocks are changed.

When operating in Asynchronous mode, the USART module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver
- · Auto-wake-up on Sync Break Character
- 13-bit Break Character Transmit
- Auto Baud Rate Detection

Electrónica

10.3.1 USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 10-2. The heart of the transmitter is the Transmit (serial) Shift Register (TSR). The shift register obtains its data from the read/write transmit buffer, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the Stop bit has been transmitted from the previous load. As soon as the Stop bit is transmitted, the TSR is loaded with new data from the TXREG register (if available).

Once the TXREG register transfers the data to the TSR register (occurs in one Tcr), the TXREG register is empty and flag bit TXIF (PIR1<4>) is set. This interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set, regardless of the state of enable bit TXIE and cannot be cleared in software. Flag bit TXIF is not cleared immediately upon loading the transmit buffer register TXREG. TXIF becomes valid in the second instruction cycle following the load instruction. Polling TXIF immediately following a load of TXREG will return invalid results.

While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. Status bit TRMT is a read only bit, which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

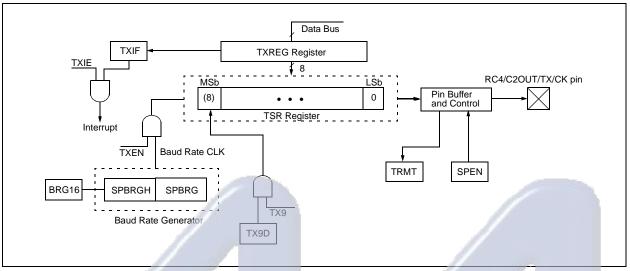
- Note 1: The TSR register is not mapped in data memory, so it is not available to the user.
 - 2: Flag bit TXIF is set when enable bit TXEN is set.

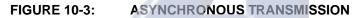
To set up an Asynchronous Transmission:

- Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- 3. If interrupts are desired, set enable bit TXIE.
- 4. If 9-bit transmission is desired, set transmit bit TX9. Can be used as address/data bit.
- 5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Load data to the TXREG register (starts transmission).

If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 10-2: USART TRANSMIT BLOCK DIAGRAM





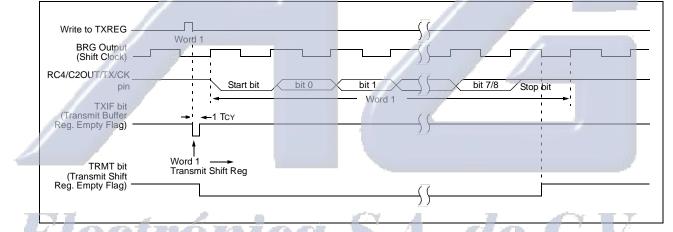
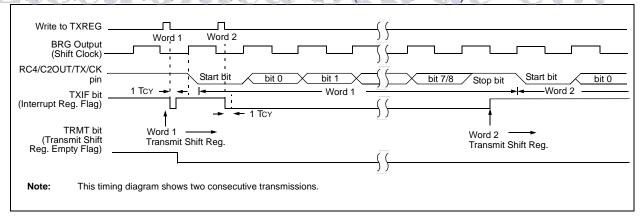


FIGURE 10-4: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)



DS41203B-page 87

 $[\]ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

IADL	BLE 10-5. REGISTERS ASSOCIATED WITH ASTICHRONOUS TRANSMISSIO									133101	N		
Addr	Name	Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0									Value on POR, BOD		e on ther sets
0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000	0000	0000	0000
11h	BAUDCTL	ABDOVF	RCIDL		SCKP	BRG16	_	WUE	ABDEN	00-0	0-00	00-0	0-00
12h	SPBRGH	USART B	aud Rate H	ligh Gener	ator					0000	0000	0000	0000
13h	SPBRG	USART Ba	aud Rate G	Generator						0000	0000	0000	0000
14h	RCREG	USART R	eceive Reg	gister						0000	0000	0000	0000
15h	TXREG	USART Tr	ansmit Re	gister						0000	0000	0000	0000
16h	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000	0010	0000	0010
17h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000	000X	0000	000X
8Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE	0000	0000	0000	0000

TABLE 10-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Transmission.

Electrónica S.A. de C.V.

10.3.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 10-5. The data is received on the RC5/RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at Fosc. This mode would typically be used in RS-232 systems.

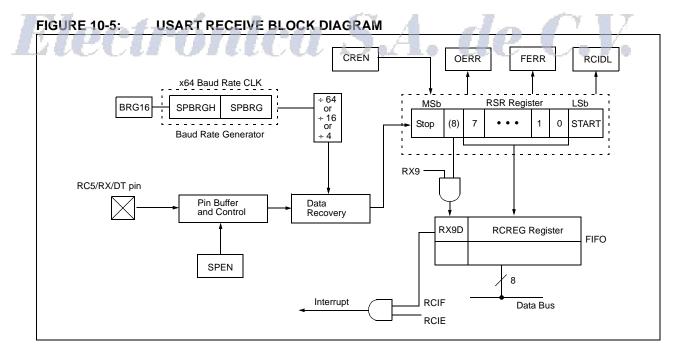
To set up an Asynchronous Reception:

- 1. Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- 3. If interrupts are desired, set enable bit RCIE.
- 4. If 9-bit reception is desired, set bit RX9.
- 5. Enable the reception by setting bit CREN.
- 6. Flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE was set.
- Read the RCSTA register to get the 9th bit (if enabled) and determine if any error occurred during reception.
- 8. Read the 8-bit received data by reading the RCREG register.
- 9. If any error occurred, clear the error by clearing enable bit CREN.
- 10. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

10.3.3 SETTING UP 9-BIT MODE WITH ADDRESS DETECT

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

- 1. Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
- If interrupts are required, set the RCEN bit and select the desired priority level with the RCIP bit.
- 4. Set the RX9 bit to enable 9-bit reception.
- 5. Set the ADDEN bit to enable address detect.
- 6. Enable reception by setting the CREN bit.
- 7. The RCIF bit will be set when reception is complete. The interrupt will be acknowledged if the RCIE and GIE bits are set.
- 8. Read the RCSTA register to determine if any error occurred during reception, as well as read bit 9 of data (if applicable).
- 9. Read RCREG to determine if the device is being addressed.
- 10. If any error occurred, clear the CREN bit.
- 11. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and interrupt the CPU.



© 2004 Microchip Technology Inc.

DS41203B-page 89

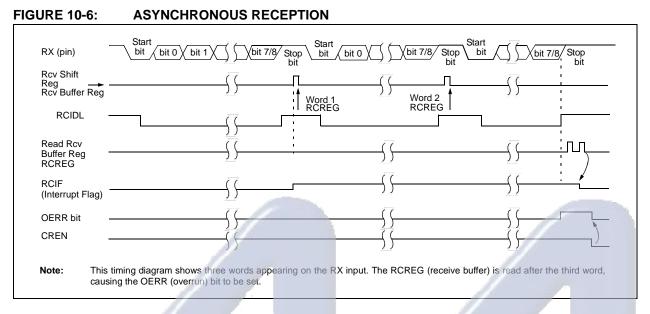


TABLE 10-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0 000 0000	0000 0000
11h	BAUDCTL	ABDOVF	RCIDL	—	SCKP	BRG16	-	WUE	ABDEN	00-0 0-00	00-0 0-00
12h	SPBRGH	USART Ba	ud Rate H	igh Gene	rator					0000 0000	0000 0000
13h	SPBRG	USART Ba	ud Rate G	enerator						0000 0000	0000 0000
14h	RCREG	USART Re	ceive Reg	ister						0000 0000	0000 0000
15h	TXREG	USART Tra	ansmit Reg	jister						0000 0000	0000 0000
16h	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
17h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000X
8Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE	0000 0000	0000 0000
Legend	d: $x = unk$	nown, - = u	inimplemer	nted locat	ions read	as '0'. Sha	aded cells	are not u	sed for Asy	nchronous Rec	eption.

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Reception.

10.3.4 AUTO-WAKE-UP ON SYNC BREAK CHARACTER

The auto-wake-up feature allows the controller to wake-up due to activity on the RX/DT line, despite the baud clock being turned off. This allows communications systems to save power by only responding to direct requests.

Setting the WUE bit (BAUDCTL<1>) enables the auto-wake-up feature. When the auto-wake-up feature is enabled, the next falling edge on the RX/DT line will trigger an RCIF interrupt. The WUE bit will automatically clear after the rising RX/DT edge after triggering a falling edge. Receiving a RCIF interrupt after setting the WUE bit signals to the user that the wake-up event has occurred. See Figure 10-7 and Figure 10-8 for timing details of the auto-wake-up process.

10.3.4.1 Special Considerations Using Auto- Wake-up

The auto-wake-up function is edge sensitive. To prevent data errors or framing errors, the data following the Break should be all '0's until the baud clock is stable. If the LP, XT or HS oscillators are used, the oscillator start-up time will affect the amount of time the application must wait before receiving valid data. Special care should be taken when using the two-speed start-up or the fail-safe clock monitor because the application will start running from the internal oscillator before the primary oscillator is ready.

Because the auto-wake-up feature uses the RCIF flag to signify the wake-up event, the application should discard the data read from RCREG when servicing the RCIF flag after setting the WUE bit.

When entering Sleep with auto-wake-up enabled, the following procedure should be used.

- 1. Clear all interrupt flags including RCIF.
- 2. Check RCIDL to ensure no receive is currently in progress.
- 3. No characters are being received so the WUE bit can be set.
- 4. Sleep.

FIGURE 10-7:	AUTO-WAKE-UP BI	T (WUE) TIMINO	GS DURING NORMAL OPERATION
OSC1 TVV			
WUE bit	y user		Auto Cleared
RCIF			Cleared due to User Read of RCREG
Note: The USAR	remains in IDLE while the WUE I	bit is set.	
FIGURE 10-8:	AUTO-WAKE-UP BI	T (WUE) TIMINO	SS DURING SLEEP
Q1 Q2 Q3	24,01,02,03,04,01,02,03,04,	Q1	02/03/04,01/02/03/04,01/02/03/04,01/02/03/04,01/02/03/04,
Bit Set b WUE bit	y User —		Auto Cleared
RX/DT Line	I I I I I I	b	
RCIF		<u>,</u>	
Ś	leep Command Executed	Sleep Ends	Cleared due to User Read of RCREG

© 2004 Microchip Technology Inc.

www.agelectronica.com

10.3.5 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. The Break character transmit consists of a Start bit, followed by 12 '0' bits and a Stop bit. The frame Break character is sent whenever the SENDB and TXEN bits (TXSTA<3> and TXSTA<5>) are set, while the Transmit Shift register is loaded with data. Note that the value of data written to TXREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

Note that the data value written to the TXREG for the Break character is ignored. The write simply serves the purpose of initiating the proper sequence.

The TRMT bit indicates when the transmit operation is active or IDLE, just as it does during normal transmission. See Figure 10-9 for the timing of the Break character sequence.



10.3.5.1 Break and Sync Transmit Sequence

The following sequence will send a message frame header made up of a Break, followed by an auto baud Sync byte. This sequence is typical of a LIN bus master.

- 1. Configure the USART for the desired mode.
- 2. Set the TXEN and SENDB bits to setup the Break character.
- 3. Load the TXREG with a dummy character to initiate transmission (the value is ignored).
- 4. Write '55h' to TXREG to load the Sync character into the transmit FIFO buffer.
- 5. After the Break has been sent, the SENDB bit is reset by hardware. The Sync character now transmits in the Pre-Configured mode.

When the TXREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXREG.

10.3.6 RECEIVING A BREAK CHARACTER

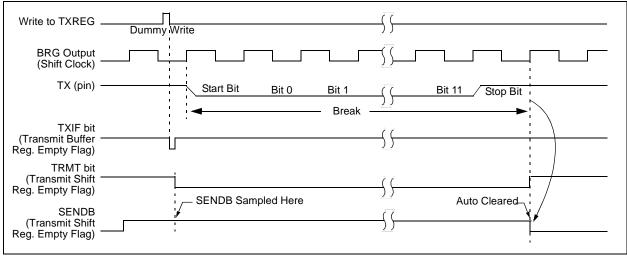
The Enhanced USART module can receive a Break character in two ways.

The first method forces to configure the baud rate at a frequency of 9/13 the typical speed. This allows for the Stop bit transition to be at the correct sampling location (13 bits for Break versus Start bit and 8 data bits for typical data).

The second method uses the auto-wake-up feature described in Section 10.3.4 "Auto-Wake-up on SYNC Break Character". By enabling this feature, the USART will sample the next two transitions on RX/DT, cause an RCIF interrupt, and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto Baud Rate Detect feature. For both methods, the user can set the ABD bit before placing the USART in its Sleep mode.

FIGURE 10-9: SEND BREAK CHARACTER SEQUENCE



DS41203B-page 92

© 2004 Microchip Technology Inc.

10.4 USART Synchronous Master Mode

The Synchronous Master mode is entered by setting the CSRC bit (TXSTA<7>). In this mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition, enable bit SPEN (RCSTA<7>) is set in order to configure the RC4/C2OUT/TX/CK and RC5/RX/DT I/O pins to CK (clock) and DT (data) lines, respectively.

The Master mode indicates that the processor transmits the master clock on the CK line. Clock polarity is selected with the SCKP bit (BAUDCTL<5>); setting SCKP sets the IDLE state on CK as high, while clearing the bit, sets the IDLE state low. This option is provided to support Microwire[®] devices with this module.

10.4.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 10-2. The heart of the transmitter is the Transmit (serial) Shift Register (TSR). The shift register obtains its data from the read/write transmit buffer register TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available).

Once the TXREG register transfers the data to the TSR register (occurs in one TCYCLE), the TXREG is empty and interrupt bit TXIF (PIR1<4>) is set. The interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set, regardless of the state of enable bit TXIE, and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register.

While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. TRMT is a read-only bit, which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory, so it is not available to the user.

To set up a Synchronous Master Transmission:

- Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 3. If interrupts are desired, set enable bit TXIE.
- 4. If 9-bit transmission is desired, set bit TX9.
- 5. Enable the transmission by setting bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREG register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 10	-10. 3	YNCHRONO	US INANG	511133101	4		9.54			/
Q1Q2	03040102030	24010203040102	20304010203	Q4 Q3Q4	10102030	401020304	101020304	010203040	21020304	Q1Q2Q3Q4
RC5/RX/ DT pin	×	bit 0 bit			bit 7	bit 0 X	bit 1			bit 7
RC4/C2OUT/ TX/CK pin (SCKP = 0)			ord 1 <u></u>				ord 2		<u></u>	_►
RC4/C2OUT/ TX/CK pin (SCKP = 1)				∟∫∫─∟					<u>, </u>	
Write to TXREG Reg	Write Word 1	Write Wo	rd 2		- - - -	- - - -	1 1	1 1 1	<u></u>	
TXIF bit (Interrupt Flag)					1 1 1	- 			<u>}</u>	
TRMT bit			י י		1 1 +	1 1 1	1 1 1	I I I	<u> </u>	
TXEN bit <u>'1'</u>			1 1 1		1 1 1	1 1 1	1 1 1	1 1 1	<u> </u>	'1'
	nc Master mode	, SPBRG = 0, cont	inuous transmi	ssion of two 8	bit words.				<u>}</u>	

© 2004 Microchip Technology Inc.

DS41203B-page 93

T



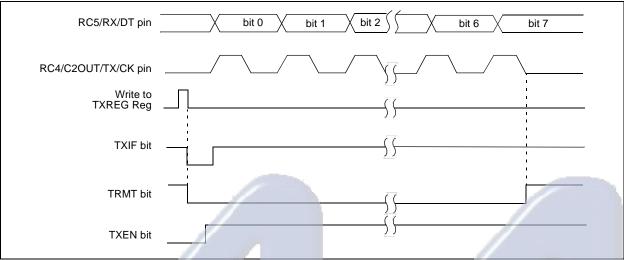


TABLE 10-7: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000 0000	0000 0000
11h	BAUDCTL	ABDOVF	RCIDL	_	SCKP	BRG16	—	WUE	ABDEN	00-00-00	00-0 0-00
12h	SPBRGH	USART Ba	ud Rate H	igh Gene	rator				1	0000 0000	0000 0000
13h	SPBRG	USART Ba	ud Rate G	enerator				1		0000 0000	0000 0000
14h	RCREG	USART Re	ceive Reg	ister						0000 0000	0000 0000
15h	TXREG	USART Tra	ansmit Reg	jister						0000 0000	0000 0000
16h	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
17h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000X
8Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE	0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Reception.

1

10.4.2 USART SYNCHRONOUS MASTER RECEPTION

Once Synchronous mode is selected, reception is enabled by setting either the Single Receive Enable bit SREN (RCSTA<5>), or the Continuous Receive Enable bit, CREN (RCSTA<4>). Data is sampled on the RC5/RX/DT pin on the falling edge of the clock.

If enable bit SREN is set, only a single word is received. If enable bit CREN is set, the reception is continuous until CREN is cleared. If both bits are set, then CREN takes precedence.



To set up a Synchronous Master Reception:

- Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 3. Ensure bits CREN and SREN are clear.
- 4. If interrupts are desired, set enable bit RCIE.
- 5. If 9-bit reception is desired, set bit RX9.
- 6. If a single reception is required, set bit SREN. For continuous reception, set bit CREN.
- Interrupt flag bit RCIF will be set when reception is complete and an interrupt will be generated if the enable bit RCIE was set.
- 8. Read the RCSTA register to get the 9th bit (if enabled) and determine if any error occurred during reception.
- 9. Read the 8-bit received data by reading the RCREG register.
- 10. If any error occurred, clear the error by clearing bit CREN.
- 11. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 10-12: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)

Q2Q	30401020	3Q4Q1Q2Q	3Q4Q1Q2C	3 <mark>Q4Q1Q2Q3</mark>	Q4 <mark>Q1</mark> Q2Q3	240102030	4 Q1 Q2 Q3	24010203	Q4Q1Q2Q3	Q4Q1Q2Q3
RC5/RX/ DT pin		bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	
RC4/C2OUT/ TX/CK pin (SCKP = 0)	1 1 1 1	ſ <u></u>				<u>+</u>	<u>-</u>	<u>+</u>		
RC4/C2OUT/ TX/CK pin- (SCKP = 1)	e i	Ś	ha i	e d	5			le.	Ċ	V
Write to bit SREN	ų —									
SREN bit	<u>ان</u>									
CREN bit	, , , , , , , , , , , , , , , , , , , ,	1 1	1 1 1	1 1 1	1 1	1 1 1	1 1 1	1 1	1 1 1	"(
RCIF bit (Interrupt) —	1 1 	1 1 1	1 1 1	1 1 1 1	1 1 1 1	1 1 1	1 1 1	1 1 1		
Read RXREG	, ,				ı ı		•	• •	• •	

TABLE 10-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION	N
--	---

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000 0000	0000 0000
11h	BAUDCTL	ABDOVF	RCIDL		SCKP	BRG16	_	WUE	ABDEN	00-0 0-00	00-0 0-00
12h	SPBRGH	USART Ba	ud Rate H	igh Gene	rator					0000 0000	0000 0000
13h	SPBRG	USART Ba	ud Rate G	enerator						0000 0000	0000 0000
14h	RCREG	USART Re	eceive Reg	ister						0000 0000	0000 0000
15h	TXREG	USART Tra	ansmit Reg	gister						0000 0000	0000 0000
16h	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
17h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	X000 000X
8Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE	0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Reception.

Electrónica S.A. de C.V.

10.5 USART Synchronous Slave Mode

Synchronous Slave mode is entered by clearing bit CSRC (TXSTA<7>). This mode differs from the Synchronous Master mode in that the shift clock is supplied externally at the RC4/C2OUT/TX/CK pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in any Low-power mode.

10.5.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the Synchronous Master and Slave modes are identical, except in the case of the Sleep mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- a) The first word will immediately transfer to the TSR register and transmit.
- b) The second word will remain in TXREG register.
- c) Flag bit TXIF will not be set.
- When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.
- e) If enable bit TXIE is set, the interrupt will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Transmission:

- Enable the synchronous slave serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- 2. Clear bits CREN and SREN.
- 3. If interrupts are desired, set enable bit TXIE.
- 4. If 9-bit transmission is desired, set bit TX9.
- 5. Enable the transmission by setting enable bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREG register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000 0000	0000 0000
11h	BAUDCTL	ABDOVF	RCIDL		SCKP	BRG16	Q4]	WUE	ABDEN	00-0 0-00	00-0 0-00
12h	SPBRGH	USART Ba	ud Rate H	igh Gene	rator					0000 0000	0000 0000
13h	SPBRG	USART Ba	ud Rate G	enerator						0000 0000	0000 0000
14h	RCREG	USART Re	eceive Reg	ister						0000 0000	0000 0000
15h	TXREG	USART Tra	ansmit Reg	jister						0000 0000	0000 0000
16h	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
17h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000X	x000 0000
8Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE	0000 0000	0000 0000

TABLE 10-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Reception.

10.5.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical, except in the case of Sleep, or any IDLE mode and bit SREN, which is a "don't care" in Slave mode.

If receive is enabled by setting the CREN bit prior to entering Sleep, then a word may be received. Once the word is received, the RSR register will transfer the data to the RCREG register; if the RCIE enable bit is set, the interrupt generated will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector. To set up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- 2. If interrupts are desired, set enable bit RCIE.
- 3. If 9-bit reception is desired, set bit RX9.
- 4. To enable reception, set enable bit CREN.
- Flag bit RCIF will be set when reception is complete. An interrupt will be generated if enable bit RCIE was set.
- Read the RCSTA register to get the 9th bit (if enabled) and determine if any error occurred during reception.
- 7. Read the 8-bit received data by reading the RCREG register.
- 8. If any error occurred, clear the error by clearing bit CREN.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 10-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000 0000	0000 0000
11h	BAUDCTL	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	00-0 0-00	00-0 0-00
12h	SPBRGH	USART Ba	ud Rate H	igh Gene	rato ^r					0000 0000	0000 0000
13h	SPBRG	USART Ba	ud Rate G	enerator			1			0000 0000	0000 0000
14h	RCREG	USART Re	eceive Reg	ister			100			0000 0000	0000 0000
15h	TXREG	USART Tra	ansmit Reg	gister						0000 0000	0000 0000
16h	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
17h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
8Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE-	TMR1IE	0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Reception.

11.0 SPECIAL FEATURES OF THE CPU

The PIC16F688 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Detect (BOD)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator Selection
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming

The PIC16F688 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brownout occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions-on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low -current Power-down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer Wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options (see Register 11-1).

Electrónica S.A. de C.V.

 $[\]ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

www.agelectronica.com

www.agelectronica.com

11.1 Configuration Bits

PIC16F688

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 11-1. These bits are mapped in program memory location 2007h.

Note: Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204) for more information.

REGISTER 11-1: CONFIG – CONFIGURATION WORD (ADDRESS: 2007h)

	- FCMEN IESO E	BODEN1 BODEN0 CPD	CP	MCLRE	PWRTE	WDTE	FOSC2 FOSC1 FOSC0
bit 13							bit 0
bit 13-12	Unimplemented: Read	las '1'					
bit 11	FCMEN: Fail-Safe Cloc						
		k Monitor is enabled					
	0 = Fail-Safe Cloc	k Monitor is disabled					
bit 10	IESO: Internal External	Switchover bit					
	1 = Internal Extern	al Switchover mode is enable	ed				
		al Switchover mode is disable	ed				
bit 9-8		out Detect Selection bits ⁽¹⁾					
	11 = BOD enabled						
		d during operation and disable		ер			1
	00 = BOD disable	ed by SBODEN bit (PCON<4>	>)			1	
bit 7	CPD: Data Code Prote						
bit i		code protection is disabled					
		code protection is enabled					
bit 6	CP: Code Protection bi	(3)					
	1 = Program mem	ory code protection is disable	d				
	0 = Program mem	ory code protection is enabled	d 🦷				
bit 5	MCLRE: RA3/MCLR pi						19
		n function is MCLR	<u>-</u>				
		n function is digital input, MCL	.R intern	ally tied to	VDD		
bit 4	PWRTE: Power-up Tim	er Enable bit	100	in J		37	1 N T T
- 8 C 8	1 = PWRT disable 0 = PWRT enable	hte in at		 A 		# 8 h	n // \/
hit 2	WDTE: Watchdog Time	r Epoblo bit	- A 3	l al 1	0		e C.V.
bit 5	1 = WDT enabled						
		and can be enabled by SWD	TEN bit	(WDTCON	√ <0>)		
bit 2-0	FOSC<2:0>: Oscillator			,	,		
	111 = RC oscillator: CL	KOUT function on RA4/OSC2	2/CLKOU	JT pin, RC	on RA5/0	DSC1/CL	KIN
	110 = RCIO oscillator:	I/O function on RA4/OSC2/CL	_KOUT p	oin, RC on	RA5/OSC	1/CLKIN	
		r: CLKOUT function on RA4/OS					
		ator: I/O function on RA4/OSC					OSC1/CLKIN
		on RA4/OSC2/CLKOUT pin, (gh-speed crystal/resonator on					
		/stal/resonator on RA4/OSC2/					
	-	v-power crystal on RA4/OSC2					
	Note 1: Enabling E	Brown-out Detect does not aut	tomatica	ally enable	Power-up	Timer.	
	2: The entire	data EEPROM will be erased	d when tl	he code pr	otection is	s turned c	off.
	3: The entire	program memory will be eras	sed wher	n the code	protection	n is turne	d off.
		LR is asserted in INTOSC or I					
				-,			
	Legend:						
	R = Readable bit	W = Writable bit			nplemente	d hit rea	d as '0'
	-n = Value at POR	'1' = Bit is set		v = Bit I	s cleared		x = Bit is unknown

DS41203B-page 100

© 2004 Microchip Technology Inc.

11.2 Calibration Bits

The Brown-out Detect (BOD), Power-on Reset (POR) and 8 MHz internal oscillator (HFINTOSC) are factory calibrated. These calibration values are stored in the Calibration Word, as shown in Register 11-2 and are mapped in program memory location 2008h.

The Calibration Word is not erased when the device is erased when using the procedure described in the "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204). Therefore, it is not necessary to store and reprogram these values when the device is erased.

Note: Address 2008h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "PIC12F6XX/16F6XX Memory Programming Specification" (DS41204) for more information.

REGISTER 11-2: CALIB – CALIBRATION WORD (ADDRESS: 2008h)



- Note 1: This location does not participate in bulk erase operations if the "PIC12F6XX/16F6XX Memory Programming Specification" (DS41204) procedure is used.
 - **2:** Calibration bits are reserved for factory calibration. These values can and will change across the entire range; therefore, specific values and available adjustment range can not be specified.

Legend:					
R = Readable bit	W = Writable bit	V = Writable bit U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

11.3 Reset

The PIC16F688 differentiates between various kinds of Reset:

- a) Power-on Reset (POR)
- b) WDT Reset during normal operation
- c) WDT Reset during Sleep
- d) MCLR Reset during normal operation
- e) MCLR Reset during Sleep
- f) Brown-out Detect (BOD)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

- Power-on Reset
- MCLR Reset
- MCLR Reset during Sleep
- WDT Reset

FIGURE 11-1:

Brown-out Detect (BOD)

They are not affected by a WDT wake-up since this is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different Reset situations, as indicated in Table 11-2. These bits are used in software to determine the nature of the Reset. See Table 11-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 11-1.

The MCLR Reset path has a noise filter to detect and ignore small pulses. See **Section 14.0** "**Electrical Specifications**" for pulse width specifications.

External Reset MCLR/VPP pin SLEEF WDT WDT Module Time-out Reset VDD Rise Detect Power-on Reset Brown-out(1) Detect BODEN SBODEN OST/PWRT OST Chip_Reset 10-bit Ripple Counter R Q OSC1/ CLKI pin **PWRT** 11-bit Ripple Counter LFINTOSC Enable PWRT Enable OST Note 1: Refer to the Configuration Word register (Register 11-1).

SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

DS41203B-page 102

© 2004 Microchip Technology Inc.

11.4 Power-On Reset

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the POR, simply connect the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Section 14.0 "Electrical Specifications" for details. If the BOD is enabled, the maximum rise time specification does not apply. The BOD circuitry will keep the device in Reset until VDD reaches VBOD (see Section 11.4.4 "Brown-Out Detect (BOD)").

Note: The POR circuit does not produce an internal Reset when VDD declines. To re-enable the POR, VDD must reach Vss for a minimum of 100 μs.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00607).

11.4.1 MCLR

PIC16F688 has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

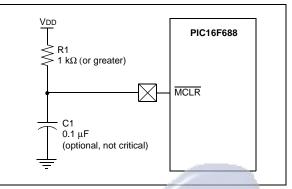
It should be noted that a WDT Reset does not drive MCLR pin low.

The behavior of the ESD protection on the MCLR pin has been altered from early devices of this family. Voltages applied to the pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 11-2, is suggested.

An internal MCLR option is enabled by clearing the MCLRE bit in the Configuration Word register. When cleared, MCLR is internally tied to VDD and an internal weak pull-up is enabled for the MCLR pin. In-Circuit Serial Programming is not affected by selecting the internal MCLR option.

FIGURE 11-2:

RECOMMENDED MCLR CIRCUIT



11.4.2 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the POR, simply connect the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Section 14.0 "Electrical Specifications" for details. If the BOD is enabled, the maximum rise time specification does not apply. The BOD circuitry will keep the device in Reset until VDD reaches VBOD (see Section 11.4.4 "Brown-Out Detect (BOD)").

Note: The POR circuit does not produce an internal Reset when VDD declines. To re-enable the POR, VDD must reach Vss for a minimum of 100 μs.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00607).

11.4.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Detect. The Power-up Timer operates from the 31 kHz LFINTOSC oscillator. For more information, see **Section 3.4 "Internal Clock Modes"**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration bit, PWRTE, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Detect is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip and vary due to:

- VDD variation
- Temperature variation
- Process variation

See DC parameters for details (Section 14.0 "Electrical Specifications").

11.4.4 BROWN-OUT DETECT (BOD)

The BODEN0 and BODEN1 bits in the Configuration Word register selects one of four BOD modes. Two modes have been added to allow software or hardware control of the BOD enable. When BODEN<1:0> = 01, the SBODEN bit (PCON<4>) enables/disables the BOD allowing it to be controlled in software. By selecting BODEN<1:0>, the BOD is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBODEN bit is disabled. See Register 11-1 for the configuration word definition. If VDD falls below VBOD for greater than parameter (TBOD) (see **Section 14.0** "**Electrical Specifica-tions**"), the Brown-out situation will reset the device. This will occur regardless of VDD slew rate. A Reset is not insured to occur if VDD falls below VBOD for less than parameter (TBOD).

On any Reset (Power-on, Brown-out Detect, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOD (see Figure 11-3). The Power-up Timer will now be invoked, if enabled and will keep the chip in Reset an additional 64 ms.

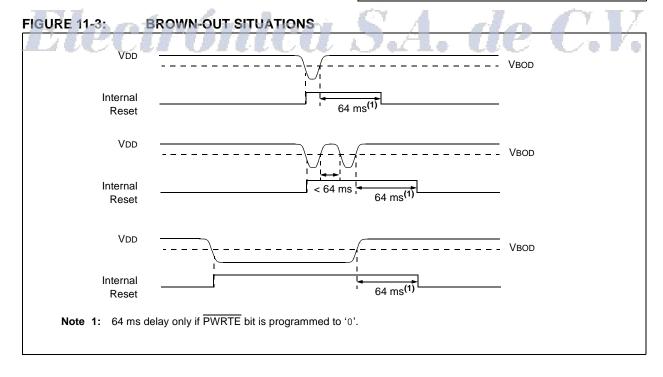
Note: <u>The Power-up Timer is enabled by the</u> <u>PWRTE bit in the Configuration Word.</u>

If VDD drops below VBOD while the Power-up Timer is running, the chip will go back into a Brown-out Detect and the Power-up Timer will be re-initialized. Once VDD rises above VBOD, the Power-up Timer will execute a 64 ms Reset.

11.4.5 BOD CALIBRATION

The PIC16F688 stores the BOD calibration values in fuses located in the Calibration Word (2008h). The Calibration Word is not erased when using the specified bulk erase sequence in the *PIC12F6XX/16F6XX Memory Programming Specification* (DS41204) and thus, does not require reprogramming.

Note: Address 2008h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See *PIC12F6XX/16F6XX Memory Programming Specification* (DS41204) for more information.



DS41203B-page 104

Preliminary

© 2004 Microchip Technology Inc.

www.agelectronica.com

11.4.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: first, PWRT time-out is invoked after POR has expired, then OST is activated after the PWRT time-out has expired. The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in EC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 11.4, Figure 11-5 and Figure 11-6 depict time-out sequences. The device can execute code from the INTOSC while OST is active by enabling Two-Speed Start-up or Fail-Safe Monitor (see Section 3.6.2 "Two-Speed Start-up Sequence" and Section 3.7 "Fail-Safe Clock Monitor").

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then, bringing MCLR high will begin execution immediately (see Figure 11-5). This is useful for testing purposes or to synchronize more than one PIC16F688 device operating in parallel.

Table 11-5 shows the Reset conditions for some special registers, while Table 11-4 shows the Reset conditions for all the registers.

11.4.7 POWER CONTROL (PCON) REGISTER

The Power Control (PCON) register (address 8Eh) has two status bits to indicate what type of Reset that last occurred.

Bit 0 is \overline{BOD} (Brown-out). \overline{BOD} is unknown on Poweron Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{BOD} = 0$, indicating that a Brown-out has occurred. The \overline{BOD} status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BODEN<1:0> = 00 in the Configuration Word register).

Bit 1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if POR is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see Section 4.2.3 "Ultra Low-Power Wake-up" and Section 11.4.4 "Brown-Out Detect (BOD)".

Oscillator Configuration	Powe	er-up	Brown-o	Wake-up		
Oscillator Configuration	PWRTE = 0	PWRTE = 1	PWRTE = 0	PWRTE = 1	from Sleep	
XT, HS, LP	TPWRT + 1024 • Tosc	1024 • To sc	Tpwrt + 1024 • Tosc	1024 • Tosc	1024 • Tosc	
RC, EC, INTOSC	TPWRT		TPWRT			

TABLE 11-1: TIME-OUT IN VARIOUS SITUATIONS

TABLE 11-2: PCON BITS AND THEIR SIGNIFICANCE

R	POR	BOD	то	PD	Condition
	0	u	1	111	Power-on Reset
	1	0	1	1	Brown-out Detect
	u	u	0	u	WDT Reset
	u	u	0	0	WDT Wake-up
	u	u	u	u	MCLR Reset during normal operation
	u	u	1	0	MCLR Reset during Sleep

Legend: u = unchanged, x = unknown

TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets ⁽¹⁾
03h	STATUS	IRP	RP1	RPO	TO	PD	Z	DC	С	0001 1xxx	000q quuu
8Eh	PCON	_		ULPWUE	SBODEN	_	_	POR	BOD	01qq	Ouuu

Legend: u = unchanged, x = unknown, — = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOD.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

www.agelectronica.com

PIC16F688

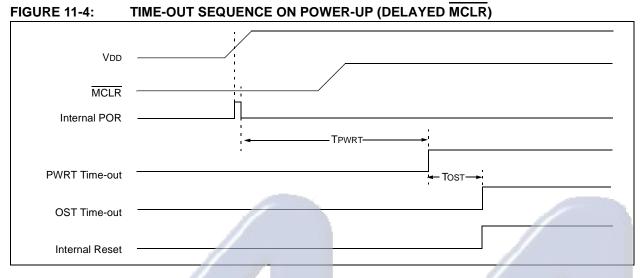


FIGURE 11-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR)

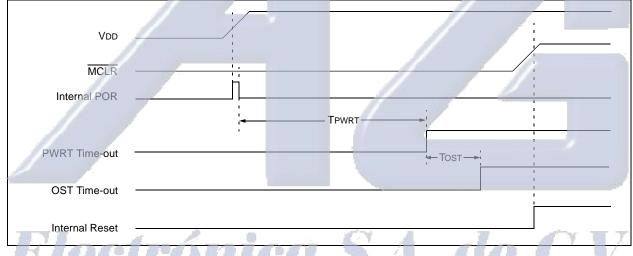
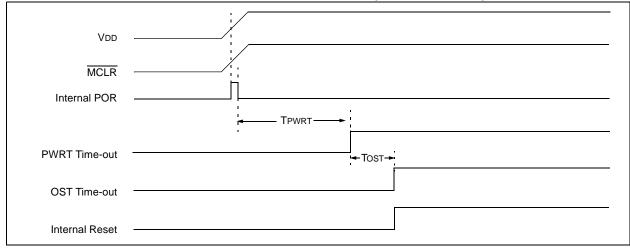


FIGURE 11-6: TIME-OUT SEQUENCE ON POWER-UP (MCLR WITH VDD)



DS41203B-page 106

Register	Address	Power-on Reset	MCLR Reset WDT Reset Brown-out Detect ⁽¹⁾	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	_	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h/100h/180h	xxxx xxxx	xxxx xxxx	սսսս սսսս
TMR0	01h/101h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h/102h/182h	0000 0000	0000 0000	PC + 1 ⁽³⁾
STATUS	03h/83h/103h/183h	0001 1xxx	000q quuu ⁽⁴⁾	uuuq quuu ⁽⁴⁾
FSR	04h/84h/104h/184h	XXXX XXXX	uuuu uuuu	uuuu uuuu
PORTA	05h/105h	xx xx00	00 0000	uu uuuu
PORTC	07h/107h	xx xx00	00 0000	uu uuuu
PCLATH	0Ah/8Ah/10Ah/18Ah	0 0000	0 0000	u uuuu
INTCON	0Bh/8Bh/10Bh/18Bh	0000 0000	0000 0000	uuu uuuu(2)
PIR1	0Ch	0000 0000	0000 0000	uuu uuuu ⁽²⁾
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	-uuu uuuu
BAUDCTL	11h	01-0 0-00	01-0 0-00	uu-u u-uu
SPBRGH	12h	-000 0000	-000 0000	-uuu uuuu
SPBRG	13h	0000 0000	0000 0000	uuuu uuuu
RCREG	14h	0000 0000	0000 0000	uuuu uuuu
TXREG	15h	0000 0000	0000 0000	uuuu uuuu
TXSTA	16h	0000 0010	0000 0010	uuuu uuuu
RCSTA	17h	000x 000x	000x 000x	uuuu uuuu
WDTCON	18h	0 1000	0 1000	u uuuu
CMCON0	19h	0000 0000	0000 0000	uuuu uuuu
CMCON1	1Ah	10	10	uu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	1Fh	00-0 0000	00-0 0000	uu-u uuuu
OPTION_REG	81h/181h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h/185h	11 1111	11 1111	uu uuuu
TRISC	87h/187h	11 1111	11 1111	uu uuuu
PIE1	8Ch	0000 0000	0000 0000	นนนน นนนน
PCON	8Eh	010x	0uuu (1,5)	uuuu

TABLE 11-4: INITIALIZATION CONDITION FOR REGISTERS

Legend: u = unchanged, x = unknown, — = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 11-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

TABLE 11-4.			UN FOR REGISTERS (CONTI	
Register	Address	Power-on Reset	 MCLR Reset WDT Reset Brown-out Detect⁽¹⁾ 	 Wake-up from Sleep through interrupt Wake-up from Sleep through WDT time-out
OSCCON	8Fh	-110 x000	-110 x000	-uuu uuuu
OSCTUNE	90h	0 0000	u uuuu	u uuuu
ANSEL	91h	1111 1111	1111 1111	uuuu uuuu
WPUA	95h	11 -111	11 -111	սսսս սսսս
IOCA	96h	00 0000	00 0000	uu uuuu
EEDATH	97h	00 0000	0000 0000	uuuu uuuu
EEADRH	98h	0000	0000 0000	uuuu uuuu
VRCON	99h	0-0- 0000	0-0- 0000	u-u- uuuu
EEDAT	9Ah	0000 0000	0000 0000	uuuu uuuu
EEADR	9Bh	0000 0000	0000 0000	uuuu u <mark>uu</mark> u
EECON1	9Ch	x x000	u q000	u uuuu
EECON2	9Dh		//	
ADRESL	9Eh	XXXX XXXX	uuuu uuuu	uuuu uuuu
ADCON1	9Fh	-000	-000	-uuu

TABLE 11-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Legend: u = unchanged, x = unknown, ---= unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

- 3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
- 4: See Table 11-5 for Reset value for specific condition.
- 5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

TABLE 11-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	A Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	010x
MCLR Reset during normal operation	000h	000u uuuu	Ouuu
MCLR Reset during Sleep	000h	0001 Ouuu	0uuu
WDT Reset	000h	0000 uuuu	0uuu
WDT Wake-up	PC + 1	սսս0 Օսսս	uuuu
Brown-out Detect	000h	0001 luuu	0110
Interrupt Wake-up from Sleep	PC + 1 ⁽¹⁾	uuul Ouuu	uuuu

Legend: u = unchanged, x = unknown, — = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

T

www.agelectronica.com PIC16F688

11.5 Interrupts

The PIC16F688 has 11 sources of interrupt:

- External Interrupt RA2/INT
- TMR0 Overflow Interrupt
- PORTA Change Interrupts
- 2 Comparator Interrupts
- A/D Interrupt
- Timer1 Overflow Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt

The Interrupt Control (INTCON) register and Peripheral Interrupt Request 1 (PIR1) register record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

A Global Interrupt Enable bit, GIE (INTCON<7>), enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIE1 register. GIE is cleared on Reset.

The Return from Interrupt instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- PORTA Change Interrupt
- TMR0 Overflow Interrupt

The peripheral interrupt flags are contained in the special register, PIR1. The corresponding interrupt enable bit is contained in special register, PIE1.

The following interrupt flags are contained in the PIR1 register:

- EEPROM Data Write Interrupt
- A/D Interrupt
- 2 Comparator Interrupts
- Timer1 Overflow Interrupt
- Fail-Safe Clock Monitor Interrupt

When an interrupt is serviced:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

For external interrupt events, such as the INT pin or PORTA change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 11-8). The latency is the same for one or twocycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

- Note 1: Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.
 - 2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, A/D or data EEPROM modules, refer to the respective peripheral section.

inthe PIRI S.A. de C.V.

www.agelectronica.com **PIC16F688**

11.5.1 **RA2/INT INTERRUPT**

External interrupt on RA2/INT pin is edge-triggered; either rising if the INTEDG bit (OPTION<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RA2/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The RA2/INT interrupt can wake-up the processor from Sleep if the INTE bit was set prior to going into Sleep. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up (0004h). See Section 11.8 "Power-Down Mode (Sleep)" for details on Sleep and Figure 11-10 for timing of wake-up from Sleep through RA2/INT interrupt.

Note: The ANSEL (91h) and CMCONO (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

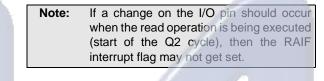
FIGURE 11-7: INTERRUPT LOGIC

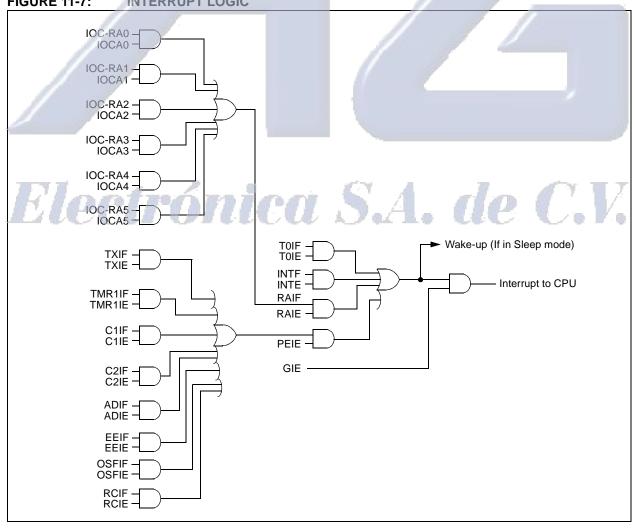
11.5.2 TMR0 INTERRUPT

An overflow (FFh \rightarrow 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing TOIE (INTCON<5>) bit. See Section 5.0 "Timer0 Module" for operation of the Timer0 module.

11.5.3 PORTA INTERRUPT

An input change on PORTA change sets the RAIF (INTCON<0>) bit. The interrupt can be enabled/ disabled by setting/clearing the RAIE (INTCON<3>) bit. Plus, individual pins can be configured through the IOCA register.





DS41203B-page 110

© 2004 Microchip Technology Inc.

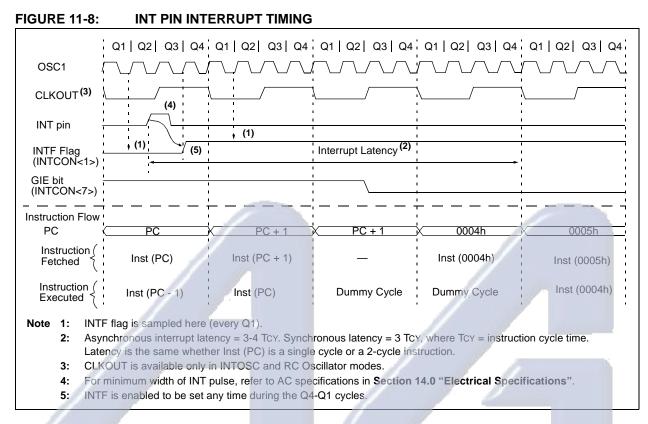


TABLE 11-6: SUMMARY OF INTERRUPT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
0Bh, 8Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	TOIF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	ADIF	RCIF	C2IF	C1IF	OSFIF	TXIF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	EEIE	ADIE	RCIE	C2IE	C1IE	OSFIE	TXIE	TMR1IE	0000 0000	0000 0000
Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by the interrupt module.											

© 2004 Microchip Technology Inc.

11.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and Status registers). This must be implemented in software.

Since the lower 16 bytes of all banks are common in the PIC16F688 (see Figure 2-2), temporary holding registers, W_TEMP and STATUS_TEMP, should be placed in here. These 16 locations do not require banking and therefore, make it easier to context save and restore. The same code shown in Example 11-1 can be used to:

- Store the W register
- Store the Status register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

Note: The PIC16F688 normally does not require saving the PCLATH. However, if computed GOTO's are used in the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 11-1: SAVING STATUS AND W REGISTERS IN RAM

MOVWF SWAPF CLRF MOVWF	W_TEMP STATUS,W STATUS STATUS_TEMP	<pre>;Copy W to TEMP register ;Swap status to be saved into W ;bank 0, regardless of current bank, Clears IRP,RP1,RP0 ;Save status to bank zero STATUS_TEMP register</pre>
: :(ISR) :		;Insert user code here
SWAPF MOVWF SWAPF SWAPF	STATUS_TEMP,W STATUS W_TEMP,F W_TEMP,W	<pre>;Swap STATUS_TEMP register into W ;(sets bank to original state) ;Move W into Status register ;Swap W_TEMP ;Swap W_TEMP into W</pre>

11.7 Watchdog Timer (WDT)

For PIC16F688, the WDT has been modified from previous 16F devices. The new WDT is code and functionally compatible with previous 16F WDT modules and adds a 16-bit prescaler to the WDT. This allows the user to have a scaler value for the WDT and TMR0 at the same time. In addition, the WDT time-out value can be extended to 268 seconds. WDT is cleared under certain conditions described in Table 11-7.

11.7.1 WDT OSCILLATOR

The WDT derives its time base from the 31 kHz LFINTOSC. The LTS bit does not reflect that the LFINTOSC is enabled.

The value of WDTCON is `---0 1000' on all Resets. This gives a nominal time base of 16 ms, which is compatible with the time base generated with previous 16F microcontroller versions.

Note:	When the Oscillator Start-up Timer (OST)								
	is invoked, the WDT is held in Reset,								
	because the WDT Ripple Counter is used								
	by the OST to perform the oscillator delay								
	count. When the OST count has expired,								
	the WDT will begin counting (if enabled).								

A new prescaler has been added to the path between the INTRC and the multiplexers used to select the path for the WDT. This prescaler is 16 bits and can be programmed to divide the INTRC by 32 to 65536, giving the WDT a nominal range of 1 ms to 268s.

11.7.2 WDT CONTROL

The WDTE bit is located in the Configuration Word register. When set, the WDT runs continuously.

When the WDTE bit in the Configuration Word register is set, the SWDTEN bit (WDTCON<0>) has no effect. If WDTE is clear, then the SWDTEN bit can be used to enable and disable the WDT. Setting the bit will enable it and clearing the bit will disable it.

The PSA and PS<2:0> bits (OPTION_REG) have the same function as in previous versions of the 16F family of microcontrollers. See Section 5.0 "Timer0 Module" for more information.

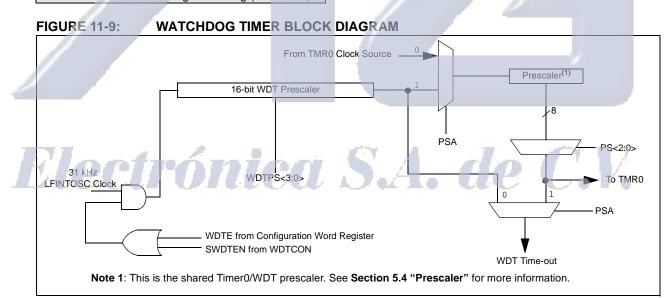


TABLE 11-7: WDT STATUS

Conditions	WDT
WDTE = 0	
CLRWDT Command	Cleared
Oscillator Fail Detected	Cleared
Exit Sleep + System Clock = T1OSC, EXTRC, INTRC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

^{© 2004} Microchip Technology Inc.

www.agelectronica.com

PIC16F688

REGISTER 11-3:	WDTCON	– WATCH	DOG TIME		OL REGIS	TER (ADD	RESS: 18h	ı)
	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
	_	—	_	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN
	bit 7							bit 0
bit 7-5	Unimplem	ented: Rea	d as '0'					
bit 4-1	WDTPS<3	:0>: Watchc	log Timer P	eriod Select	bits			
	Bit Value =	= Prescale F	Rate					
	0000 = 1:	32						
	0001 = 1:	-						
	0010 = 1:	-						
	0011 = 1:		(and)					
	0100 = 1: 0101 = 1:	512 (Reset	value)					
	0101 = 1. 0110 = 1:							
	0110 = 1:							
	1000 = 1		/ L					
	1001 = 1:	1.1 C						
	1010 = 1:	32768						
	1011 = 1:	65536					1	10
	1100 = re							
	1101 = re					1		
	1110 = re					1		
	1111 = re	served				1. 1		
bit 0		Software E	hable or Dis	ahle the Wa	tchdog Time	r(1)		
DIT U	1 = WDT is				tondog mine	1		
		s turned off (Reset value					
		s turrieu on (Neset value	·)				
11	Note 1		onfiguration	hit - 1 the	n WDT is a	lways enab	led irresper	tive of this
	1010 1.				it = 0, then i			
		this control		3	,			

Rioe	Legend:	nn S	1 614	
	R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
	- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 11-8:	SUMMARY OF WATCHDOG TIMER REGISTERS
-------------	-------------------------------------

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WSTPS1	WDTPS0	SWDTEN
81h	OPTION_REG	RAPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0
2007h ⁽¹⁾	CONFIG	CPD	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Register 11-1 for operation of all Configuration Word register bits.

DS41203B-page 114

11.8 Power-Down Mode (Sleep)

The Power-down mode is entered by executing a SLEEP instruction.

If the Watchdog Timer is enabled:

- WDT will be cleared but keeps running.
- PD bit in the Status register is cleared.
- TO bit is set.
- · Oscillator driver is turned off.
- I/O ports maintain the status they had before SLEEP was executed (driving high, low or highimpedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSs, with no external circuitry drawing current from the I/O pin, and the comparators and CVREF should be disabled. I/O pins that are high-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or Vss for lowest current consumption. The contribution from on-chip pull-ups on PORTA should be considered.

The MCLR pin must be at a logic high level.

Note: It should be noted that a Reset generated by a WDT time-out does not drive MCLR pin low.

11.8.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

- 1. External Reset input on MCLR pin.
- 2. Watchdog Timer wake-up (if WDT was enabled).
- Interrupt from RA2/INT pin, PORTA change or a peripheral interrupt.

The first event will cause a device Reset. The two latter events are considered a continuation of program execution. The $\overline{\text{TO}}$ and PD bits in the Status register can be used to determine the cause of device Reset. The PD bit, which is set on power-up, is cleared when Sleep is invoked. $\overline{\text{TO}}$ bit is cleared if WDT wake-up occurred.

The following peripheral interrupts can wake the device from Sleep:

- 1. TMR1 Interrupt. Timer1 must be operating as an asynchronous counter.
- 2. EUSART Receive Interrupt.
- 3. ULPWU Interrupt.
- 4. A/D conversion (when A/D clock source is RC).
- 5. EEPROM write operation completion.
- 6. Comparator output changes state.
- 7. Interrupt-on-change.
- 8. External Interrupt from INT pin.

Other peripherals cannot generate interrupts since during Sleep, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

Note: If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from Sleep. The SLEEP instruction is completely executed.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

11.8.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will not be cleared, the TO bit will not be set and the PD bit will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake-up from Sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will be cleared, the TO bit will be set and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

© 2004 Microchip Technology Inc.

WAKE-UP FROM SLEEP THROUGH INTERRUPT **FIGURE 11-10:**

OSC1 / CLKOUT ⁽⁴⁾ \ INT pin _	Q1 Q2 Q3 Q4; 	Q1 Q2 Q3 Q4 _/_/_/ 	· · · · · · · · · · · · · · · · · · ·		Q1 Q2 Q3 Q4 √√√√√√ 	01 02 03 04 	Q1 Q2 Q3 Q4; ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	Q1 Q2 Q3 Q4;
INTF flag			: s	· · ·	Interrupt Laten			
(INTCON<1>) -			· · · · · · · · · · · · · · · · · · ·		Interrupt Laten			1
GIE bit (INTCON<7>)			Processor	in			, , ,	
;-	į		Sleep	`'-				
Instruction Flow	i		1 1	: i		1 1		
РС Х	PC X	PC+1	X PC	+2 X	PC+2	X PC+2	(<u>0004h</u>)	0005h ·
Instruction { Fetched	Inst(PC) = Sleep	Inst(PC + 1)			Inst(PC + 2)	 	Inst(0004h)	Inst(0005h)
Instruction { Executed {	Inst(PC - 1)	Sleep		1	Inst(PC + 1)	Dummy Cycle	Dummy Cycle	Inst(0004h)
Note 1: X	T. HS or LP Oscilla	ator mode assum	ed.					

- TOST = 1024 TOSC (drawing not to scale). This delay does not apply to EC and RC Oscillator modes. 2:
- 3: GIE = 1 assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = 0, execution will continue in-line.
- CLKOUT is not available in XT, HS, LP or EC Oscillator modes, but shown here for timing reference. 4:



Electrónica S.A. de C.V.

11.9 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP for verification purposes.

Note: The entire data EEPROM and Flash program memory will be erased when the code protection is turned off. See the "PIC12F6XX/16F6XX Memory Programming Specification" (DS41204) for more information.

11.10 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.

11.11 In-Circuit Serial Programming

The PIC16F688 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for:

- power
- ground
- programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

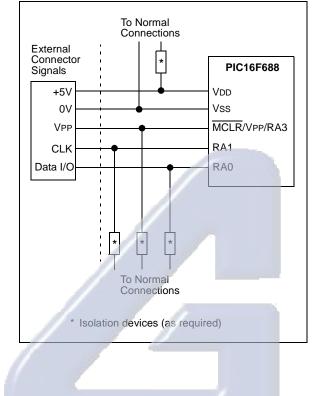
The device is placed into a Program/Verify mode by nolding the RA0 and RA1 pins low, while raising the MCLR (VPP) pin from VIL to VIHH. See the "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204) for more information. RA0 becomes the programming data and RA1 becomes the programming clock. Both RA0 and RA1 are Schmitt Trigger inputs in this mode.

After Reset, to place the device into Program/Verify mode, the Program Counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204).

A typical In-Circuit Serial Programming connection is shown in Figure 11-11.

FIGURE 11-11:

TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



S.A. de C.V.

^{© 2004} Microchip Technology Inc.

11.12 In-Circuit Debugger

Since in-circuit debugging requires access to the data and MCLR pins, MPLAB[®] ICD 2 development with an 14-pin device is not practical. A special 20-pin PIC16F688 ICD device is used with MPLAB ICD 2 to provide separate clock, data and MCLR pins and frees all normally available pins to the user.

A special debugging adapter allows the ICD device to be used in place of a PIC16F688 device. The debugging adapter is the only source of the ICD device.

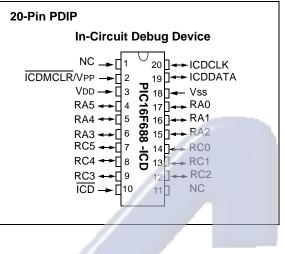
When the $\overline{\text{ICD}}$ pin on the PIC16F688 ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 11-9 shows which features are consumed by the background debugger:

TABLE 11-9: DEBUGGER RESOURCES

Resource	Description	
I/O pins	ICDCLK, ICDDATA	
Stack	1 level	
Program Memory	Address 0h must be NOP 700h-7FFh	

For more information, see "*MPLAB ICD 2 In-Circuit Debugger User's Guide*" (DS51292), available on Microchip's web site (www.microchip.com).

FIGURE 11-12: 20-PIN ICD PINOUT



Electrónica S.A. de C.V.

12.0 INSTRUCTION SET SUMMARY

The PIC16F688 instruction set is highly orthogonal and is comprised of three basic categories:

- Byte-oriented operations
- Bit-oriented operations
- Literal and control operations

Each PIC16 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 12-1, while the various opcode fields are summarized in Table 12-1.

Table 12-2 lists the instructions recognized by the MPASM[™] assembler. A complete description of each instruction is also available in the "*PICmicro*[®] *Mid-Range MCU Family Reference Manual*" (DS33023).

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μ s. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

Note:	To maintain upward compatibility with
	future products, do not use the OPTION
	and TRIS instructions.

All instruction examples use the format '0 xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

12.1 READ-MODIFY-WRITE OPERATIONS

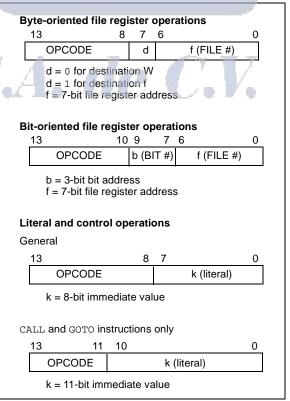
Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a CLRF GPIO instruction will read GPIO, clear all the data bits, then write the result back to GPIO. This example would have the unintended result of clearing the condition that set the GPIF flag.

TABLE 12-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with $x = 0$. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; $d = 0$: store result in W, d = 1: store result in file register f. Default is $d = 1$.
PC	Program Counter
ТО	Time-out bit
PD	Power-down bit

FIGURE 12-1: GENERAL FORMAT FOR INSTRUCTIONS



© 2004 Microchip Technology Inc.

Mnemonic, Description		Deceription	Cueles		14-Bit C	Opcode	Status Affected	Neter	
		Cycles	MSb			LSb		Notes	
		BYTE-ORIENTED FILE RE	GISTER OPE	RATIC	NS				
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	. 1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	fff	Z	1,2
		BIT-ORIENTED FILE REC		ATIO	NS		1		
BCF	f, b 🥖	Bit Clear f	1	01	00bb	bfff	ffff	2	1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
	/	LITERAL AND CONTR	ROL OPERAT	IONS	/				
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	199
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	I	Return from interrupt	2	00	0000	0000	1001	100	T
RETLW	k	Return with literal in W	2	/ 11	01xx	kkkk	kkkk		
RETURN		Return from Subroutine	2	00	0000	0000	1000	1 / m	V
SLEEP		Go into Standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11			kkkk	Z	
Note 1: When an I/O register is modified as a function of itself (e.g., MOVF GPIO, 1), the value used will be that value present									
on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external									
	on the pir	ns themselves. For example, if the data latch is	s '1' for a pin co	onfigur	ed as inp	out and	is drive	n low by an	exte

TABLE 12-2: PIC16F688 INSTRUCTION SET

device, the data will be written back with a '0'.
2: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

Note: Additional information on the mid-range instruction set is available in the *PICmicro[®] Mid-Range MCU Family Reference Manual*" (DS33023).

ADDLW	Add Literal and W
Syntax:	[label] ADDLW k
Operands:	$0 \le k \le 255$
Operation:	$(W) + k \to (W)$
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

12.2	Instruction Descrip	tions
------	---------------------	-------

BCF	Bit Clear f
Syntax:	[label] BCF f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	$0 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

ADDWF	Add W and f
Syntax:	[label] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) \rightarrow (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW	AND Literal with W
Syntax:	[label] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) \rightarrow (W)
Status Affected:	tránica
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[label] ANDWF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1\right] \end{array}$
Operation:	(W) .AND. (f) \rightarrow (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BSF	Bit Set f
Syntax:	[labe/]BSF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	$1 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.
BTFSS	Bit Test f, Skip if Set
Svntax:	[label] BTFSS f.b
Syntax: Operands:	[<i>label</i>] BTFSS f,b 0 ≤ f ≤ 127 0 ≤ b < 7
•	$0 \le f \le 127$
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7

© 2004 Microchip Technology Inc.

www.agelectronica.com PIC16F688

BTFSC	Bit Test, Skip if Clear
Syntax:	[label]BTFSC f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	skip if (f) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the
	next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

CALL	Call Subroutine
Syntax:	[label] CALL k
Operands:	$0 \le k \le 2047$
Operation:	$\begin{array}{l} (PC) + 1 \rightarrow TOS, \\ \mathbf{k} \rightarrow PC < 10:0 >, \\ (PCLATH < 4:3 >) \rightarrow PC < 12:11 > \end{array}$
Status Affected:	None
Description:	Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

CLRWDT	Clear Watchdog Timer
Syntax:	[label] CLRWDT
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow WDT \\ 0 \rightarrow WDT \text{ prescaler,} \\ 1 \rightarrow \overline{TO} \\ 1 \rightarrow \overline{PD} \end{array}$
Status Affected:	TO, PD
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set.
COMF	Complement f
Syntax:	[label] COMF f,d
Operands:	0 ≤ f ≤ 127
	d ∈ [0,1]
Operation:	$(\overline{f}) \rightarrow (destination)$
Operation: Status Affected:	$(\tilde{f}) \rightarrow (destination)$

CLRF	Clear f
Syntax:	[label] CLRF f
Operands:	$0 \le f \le 127$
Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

CLRW	Clear W
Syntax:	[label] CLRW
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow (W) \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

DECF	Decrement f
Syntax:	[label] DECF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \ [0,1] \end{array}$
Operation:	(f) - 1 \rightarrow (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

DS41203B-page 122

© 2004 Microchip Technology Inc.

www.agelectronica.com

www.agelectronica.com PIC16F688

DECFSZ	Decrement f, Skip if 0	INCFSZ	Increment f, Skip if 0
Syntax:	[label] DECFSZ f,d	Syntax:	[label] INCFSZ f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1\right] \end{array}$	Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 \rightarrow (destination); skip if result = 0	Operation:	(f) + 1 \rightarrow (destination), skip if result = 0
Status Affected:	None	Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.	Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.
бото	Unconditional Branch	MOVF	Move f
Syntax:	[label] GOTO k	Syntax:	[label] MOVF f,d
Operands:	$0 \le k \le 2047$	Operands:	0 ≤ f ≤ 127
Operation:	$k \rightarrow PC < 10:0>$		d ∈ [0,1]
	$PCLATH<4:3> \rightarrow PC<12:11>$	Operation:	(f) \rightarrow (dest)
Status Affected:	None	Status Affected:	Z
Description:	GOTO is an unconditional branch.	Encoding:	00 1000 dfff fff
Blec	The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.	Description:	The contents of register f is moved to a destination dependent upon the status of d. If $d = 0$, destination is W register. If $d = 1$, the destination is file register f itself. $d = 1$ is useful to test a file register since status flag Z is affected.
Syntax:	[label] INCF f,d	Words:	1
Operands:	$0 \le f \le 127$	Cycles:	1
oporarias.	$d \in [0,1]$	<u>Example</u>	MOVF FSR, 0
Operation:	(f) + 1 \rightarrow (destination)		After Instruction
Status Affected:	Z		W = value in FSR
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.		register Z = 1

© 2004 Microchip Technology Inc.

DS41203B-page 123

4

www.agelectronica.com

MOVWF	Move W to f
Syntax:	[label] MOVWF f
Operands:	$0 \le f \le 127$
Operation:	$(WV) \to (f)$
Status Affected:	None
Encoding:	00 0000 1fff ffff
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
<u>Example</u>	MOVWF OPTION
IORLW	$\begin{array}{rcl} & \text{OPTION} = & 0xFF\\ W & = & 0x4F\\ \text{After Instruction} & & \\ & \text{OPTION} = & 0x4F\\ W & = & 0x4F\\ \end{array}$ Inclusive OR Literal with W
Syntax:	[label] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. $k \rightarrow$ (W)
Status Affected:	z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.
IORWF Syntax:	Inclusive OR W with f

MOVLW	Move Literal to W
Syntax:	[<i>label</i>] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	$k \rightarrow (W)$
Status Affected:	None
Encoding:	11 00xx kkkk kkkk
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.
Words:	1
Cycles:	1
Example	MOVLW 0x5A
	After Instruction W = 0x5A
NOP	No Operation
Syntax:	[label] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Encoding:	000 0000 0xx0 0000
Description:	No operation.
Words:	1
Cycles:	1
	ile C.V.

IORWF	Inclusive OR W with f
Syntax:	[label] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .OR. (f) \rightarrow (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

DS41203B-page 124

RETFIE	Return from Interrupt	RETLW	Return with Literal in W
Syntax:	[label] RETFIE	Syntax:	[<i>label</i>] RETLW k
Operands:	None	Operands:	$0 \le k \le 255$
Operation:	$TOS \rightarrow PC,$ 1 $\rightarrow GIE$	Operation:	$\begin{array}{l} k \rightarrow (W);\\ TOS \rightarrow PC \end{array}$
Status Affected:	None	Status Affected:	None
Encoding:	00 0000 0000 1001	Encoding:	11 01xx kkkk kkk
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE	Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top o the stack (the return address). This is a two-cycle instruction.
	(INTCON<7>). This is a two-cycle instruction.	Words:	1
Words:	1	Cycles:	2
Cycles: Example	2 RETFIE	Example	CALL TABLE; W contains table ;offset value • ;W now has table value
	After Interrupt PC = TOS GIE = 1	TABLE	ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; • • • • • • • • • • • • • • • • • • •
e e e e e e e e e e e e e e e e e e e	etrónica –		Return from Subroutine
		Syntax:	[label] RETURN
		Operands:	None
		Operation:	$TOS \to PC$
		Status Affected:	None
		Description:	Return from subroutine. The stact is POPed and the top of the stact (TOS) is loaded into the program counter. This is a two-cycle instruction.

www.agelectronica.com PIC16F688

RLF	Rotate Left f through Carry		
Syntax:	[<i>label</i>] RLF f,d		
Operands:	$0 \le f \le 127$		
	d ∈ [0,1]		
Operation:	See description below		
Status Affected:	С		
Encoding:	00 1101 dfff ffff		
Description:	The contents of register 'f' are		
	rotated one bit to the left through		
	the Carry Flag. If 'd' is '0', the result is placed in the W register.		
	If 'd' is '1', the result is stored		
	back in register 'f'.		
	C Register f		
Words:	1		
Cycles:	1		
Example	RLF REG1,0		
<u> </u>	Before Instruction		
	REG1 = 1110 0110		
	C = 0		
	After Instruction REG1 = 1110 0110		
	W = 1100 1100		
	C = 1		
1			
RRF	Rotate Right f through Carry		
Syntax:	[<i>label</i>] RRF f,d		
Operands:	0≤f≤127 d∈ [0,1]		
Operation:	See description below		
Status Affected:	С		
Description:	The contents of register 'f' are		
	rotated one bit to the right through		
	the Carry Flag. If 'd' is '0', the result is placed in the W register.		
	If 'd' is '1', the result is placed		
	back in register 'f'.		
	C Register f		

SLEEP

Syntax:	[label] SLEEP
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow WDT, \\ 0 \rightarrow WDT \text{ prescaler,} \\ 1 \rightarrow \overline{TO}, \\ 0 \rightarrow \overline{PD} \end{array}$
Status Affected:	TO, PD
Description:	The power-down Status bit, PD is cleared. Time-out Status bit, TO is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.
SUBLW	Subtract W from Literal
Syntax:	[label] SUBLW k
Operands:	$0 \le k \le 255$
Operation:	$k - (W) \rightarrow (W)$
Status Affected:	C, DC, Z
Description:	The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.
and the second se	

SUBWF	Subtract W from f
Syntax:	[label] SUBWF f,d
Operands:	$\begin{array}{c} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) - (W) \rightarrow (destination)
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

SWAPF	Swap Nibbles in f	
Syntax:	[<i>label</i>] SWAPF f,d	
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in \left[0,1\right] \end{array}$	
Operation:	(f<3:0>) \rightarrow (destination<7:4>), (f<7:4>) \rightarrow (destination<3:0>)	
Status Affected:	None	
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.	
XORLW	Exclusive OR Literal with W	
Syntax:	[label] XORLW k	
Operands:	0 ≤ k ≤ 255	
Operation:	(W) .XOR. $k \rightarrow$ (W)	
Status Affected:	Z	
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.	
XORWF	Exclusive OR W with f	
Syntax:	[label] XORWF f,d	
Operands:	$0 \le f \le 127$	
	d ∈ [0,1]	CA J. CV
Operation: Status Affected:-	(W) .XOR. (f) \rightarrow (destination)	S.A. de C.
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.	

www.agelectronica.com

PIC16F688

NOTES:



Electrónica S.A. de C.V.

DS41203B-page 128

Preliminary

© 2004 Microchip Technology Inc.

www.agelectronica.com

13.0 DEVELOPMENT SUPPORT

The PICmicro[®] microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB[®] IDE Software
- Assemblers/Compilers/Linkers
 - MPASM[™] Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB C30 C Compiler
 - MPLAB ASM30 Assembler/Linker/Library
- Simulators
 - MPLAB SIM Software Simulator
 - MPLAB dsPIC30 Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
- MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
- MPLAB ICD 2
- Device Programmers
 - PRO MATE® II Universal Device Programmer
 - PICSTART[®] Plus Development Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration Boards
 - PICDEM[™] 1 Demonstration Board
 - PICDEM.net[™] Demonstration Board
 - PICDEM 2 Plus Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 4 Demonstration Board
 - PICDEM 17 Demonstration Board
 - PICDEM 18R Demonstration Board
 - PICDEM LIN Demonstration Board
 - PICDEM USB Demonstration Board
- Evaluation Kits
 - KEELOQ®
 - PICDEM MSC
 - microID®
 - CAN
 - PowerSmart®
 - Analog

13.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows[®] based application that contains:

- An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- · A full-featured editor with color coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Extensive on-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files (assembly or C)
 - mixed assembly and C
 - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

13.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PICmicro MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- · User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

13.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI C compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

13.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB object librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

13.5 MPLAB C30 C Compiler

The MPLAB C30 C compiler is a full-featured, ANSI compliant, optimizing compiler that translates standard ANSI C programs into dsPIC30F assembly language source. The compiler also supports many command line options and language extensions to take full advantage of the dsPIC30F device hardware capabilities and afford fine control of the compiler code generator.

MPLAB C30 is distributed with a complete ANSI C standard library. All library functions have been validated and conform to the ANSI C library standard. The library includes functions for string manipulation, dynamic memory allocation, data conversion, timekeeping and math functions (trigonometric, exponential and hyperbolic). The compiler provides symbolic information for high-level source debugging with the MPLAB IDE.

13.6 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 compiler uses the assembler to produce it's object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

13.7 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC hosted environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any pin. The execution can be performed in Single-Step, Execute Until Break or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and MPLAB C18 C Compilers, as well as the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent, economical software development tool.

13.8 MPLAB SIM30 Software Simulator

The MPLAB SIM30 software simulator allows code development in a PC hosted environment by simulating the dsPIC30F series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any of the pins.

The MPLAB SIM30 simulator fully supports symbolic debugging using the MPLAB C30 C Compiler and MPLAB ASM30 assembler. The simulator runs in either a Command Line mode for automated tasks, or from MPLAB IDE. This high-speed simulator is designed to debug, analyze and optimize time intensive DSP routines.

13.9 MPLAB ICE 2000 High-Performance Universal In-Circuit Emulator

The MPLAB ICE 2000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 in-circuit emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft[®] Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

13.10 MPLAB ICE 4000 High-Performance Universal In-Circuit Emulator

The MPLAB ICE 4000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for highend PICmicro microcontrollers. Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICD 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high-speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, up to 2 Mb of emulation memory and the ability to view variables in real-time.

The MPLAB ICE 4000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

13.11 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PICmicro MCUs and can be used to develop for these and other PICmicro microcontrollers. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming[™] (ICSP[™]) protocol, offers cost effective in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single-stepping and watching variables, CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real-time, MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

13.12 PRO MATE II Universal Device Programmer

The PRO MATE II is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features an LCD display for instructions and error messages and a modular detachable socket assembly to support various package types. In Stand-Alone mode, the PRO MATE II device programmer can read, verify and program PICmicro devices without a PC connection. It can also set code protection in this mode.

13.13 MPLAB PM3 Device Programmer

The MPLAB PM3 is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 device programmer can read, verify and program PICmicro devices without a PC connection. It can also set code protection in this mode. MPLAB PM3 connects to the host PC via an RS-232 or USB cable. MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

^{© 2004} Microchip Technology Inc.

13.14 PICSTART Plus Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus development programmer supports most PICmicro devices up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

13.15 PICDEM 1 PICmicro Demonstration Board

The PICDEM 1 demonstration board demonstrates the capabilities of the PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The sample microcontrollers provided with the PICDEM 1 demonstration board can be programmed with a PRO MATE II device programmer or a PICSTART Plus development programmer. The PICDEM 1 demonstration board can be connected to the MPLAB ICE in-circuit emulator for testing. A prototype area extends the circuitry for additional application components. Features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs.

13.16 PICDEM.net Internet/Ethernet Demonstration Board

The PICDEM.net demonstration board is an Internet/ Ethernet demonstration board using the PIC18F452 microcontroller and TCP/IP firmware. The board supports any 40-pin DIP device that conforms to the standard pinout used by the PIC16F877 or PIC18C452. This kit features a user friendly TCP/IP stack, web server with HTML, a 24L256 Serial EEPROM for Xmodem download to web pages into Serial EEPROM, ICSP/MPLAB ICD 2 interface connector, an Ethernet interface, RS-232 interface and a 16 x 2 LCD display. Also included is the book and CD-ROM *"TCP/IP Lean, Web Servers for Embedded Systems,"* by Jeremy Bentham

13.17 PICDEM 2 Plus Demonstration Board

The PICDEM 2 Plus demonstration board supports many 18, 28 and 40-pin microcontrollers, including PIC16F87X and PIC18FXX2 devices. All the necessary hardware and software is included to run the demonstration programs. The sample microcontrollers provided with the PICDEM 2 demonstration board can be programmed with a PRO MATE II device programmer, PICSTART Plus development programmer, or MPLAB ICD 2 with a Universal Programmer Adapter. The MPLAB ICD 2 and MPLAB ICE in-circuit emulators may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area extends the circuitry for additional application components. Some of the features include an RS-232 interface, a 2 x 16 LCD display, a piezo speaker, an on-board temperature sensor, four LEDs and sample PIC18F452 and PIC16F877 Flash microcontrollers.

13.18 PICDEM 3 PIC16C92X Demonstration Board

The PICDEM 3 demonstration board supports the PIC16C923 and PIC16C924 in the PLCC package. All the necessary hardware and software is included to run the demonstration programs.

13.19 PICDEM 4 8/14/18-Pin Demonstration Board

The PICDEM 4 can be used to demonstrate the capabilities of the 8, 14 and 18-pin PIC16XXXX and PIC18XXXX MCUs, including the PIC16F818/819, PIC16F87/88, PIC16F62XA and the PIC18F1320 family of microcontrollers. PICDEM 4 is intended to showcase the many features of these low pin count parts, including LIN and Motor Control using ECCP. Special provisions are made for low-power operation with the supercapacitor circuit and jumpers allow onboard hardware to be disabled to eliminate current draw in this mode. Included on the demo board are provisions for Crystal, RC or Canned Oscillator modes, a five volt regulator for use with a nine volt wall adapter or battery, DB-9 RS-232 interface, ICD connector for programming via ICSP and development with MPLAB ICD 2, 2 x 16 liquid crystal display, PCB footprints for H-Bridge motor driver, LIN transceiver and EEPROM. Also included are: header for expansion, eight LEDs, four potentiometers, three push buttons and a prototyping area. Included with the kit is a PIC16F627A and a PIC18F1320. Tutorial firmware is included along with the User's Guide.

13.20 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. A programmed sample is included. The PRO MATE II device programmer, or the PICSTART Plus development programmer, can be used to reprogram the device for user tailored application development. The PICDEM 17 demonstration board supports program download and execution from external on-board Flash memory. A generous prototype area is available for user hardware expansion.

13.21 PICDEM 18R PIC18C601/801 Demonstration Board

The PICDEM 18R demonstration board serves to assist development of the PIC18C601/801 family of Microchip microcontrollers. It provides hardware implementation of both 8-bit Multiplexed/Demultiplexed and 16-bit Memory modes. The board includes 2 Mb external Flash memory and 128 Kb SRAM memory, as well as serial EEPROM, allowing access to the wide range of memory types supported by the PIC18C601/801.

13.22 PICDEM LIN PIC16C43X Demonstration Board

The powerful LIN hardware and software kit includes a series of boards and three PICmicro microcontrollers. The small footprint PIC16C432 and PIC16C433 are used as slaves in the LIN communication and feature on-board LIN transceivers. A PIC16F874 Flash microcontroller serves as the master. All three micro-controllers are programmed with firmware to provide LIN bus communication.

13.23 PICkit[™]1 Flash Starter Kit

A complete "development system in a box", the PICkit Flash Starter Kit includes a convenient multi-section board for programming, evaluation and development of 8/14-pin Flash PIC[®] microcontrollers. Powered via USB, the board operates under a simple Windows GUI. The PICkit 1 Starter Kit includes the User's Guide (on CD ROM), PICkit 1 tutorial software and code for various applications. Also included are MPLAB[®] IDE (Integrated Development Environment) software, software and hardware "Tips 'n Tricks for 8-pin Flash PIC[®] Microcontrollers" Handbook and a USB interface cable. Supports all current 8/14-pin Flash PIC microcontrollers, as well as many future planned devices.

13.24 PICDEM USB PIC16C7X5 Demonstration Board

The PICDEM USB Demonstration Board shows off the capabilities of the PIC16C745 and PIC16C765 USB microcontrollers. This board provides the basis for future USB products.

13.25 Evaluation and Programming Tools

In addition to the PICDEM series of circuits, Microchip has a line of evaluation kits and demonstration software for these products.

- KEELOQ evaluation and programming tools for Microchip's HCS Secure Data Products
- CAN developers kit for automotive network applications
- Analog design boards and filter design software
- PowerSmart battery charging evaluation/ calibration kits
- IrDA[®] development kit
- microID development and rfLab[™] development software
- SEEVAL[®] designer kit for memory evaluation and endurance calculations
- PICDEM MSC demo boards for Switching mode power supply, high-power IR driver, delta sigma ADC and flow rate sensor

Check the Microchip web page and the latest Product Selector Guide for the complete list of demonstration and evaluation kits.

S.A. de C.V.

^{© 2004} Microchip Technology Inc.

www.agelectronica.com

PIC16F688

NOTES:



Electrónica S.A. de C.V.

DS41203B-page 134

Preliminary

© 2004 Microchip Technology Inc.

www.agelectronica.com

14.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings^(†)

Ambient termenerature under bies	0 to 1000
Ambient temperature under bias40	1250
-65°C	C to +150°C
Voltage on VDD with respect to Vss	3V to +6.5V
Voltage on MCLR with respect to Vss0.3	V to +13.5V
Voltage on all other pins with respect to Vss0.3V to (Vdd + 0.3V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, Iiк (Vi < 0 or Vi > VDD)	± 20 m <mark>A</mark>
Output clamp current, loк (Vo < 0 or Vo >VDD)	± 20 m <mark>A</mark>
Maximum output current sunk by any I/O pin	25 m <mark>A</mark>
Maximum output current sourced by any I/O pin	25 m <mark>A</mark>
Maximum current sunk by PORTA and PORTC (combined)	200 m <mark>A</mark>
Maximum current sourced PORTA and PORTC (combined)	200 mA

Note 1: Power dissipation is calculated as follows: $PDIS = VDD \times \{IDD - \sum IOH\} + \sum \{(VDD - VOH) \times IOH\} + \sum (VOL \times IOL).$

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

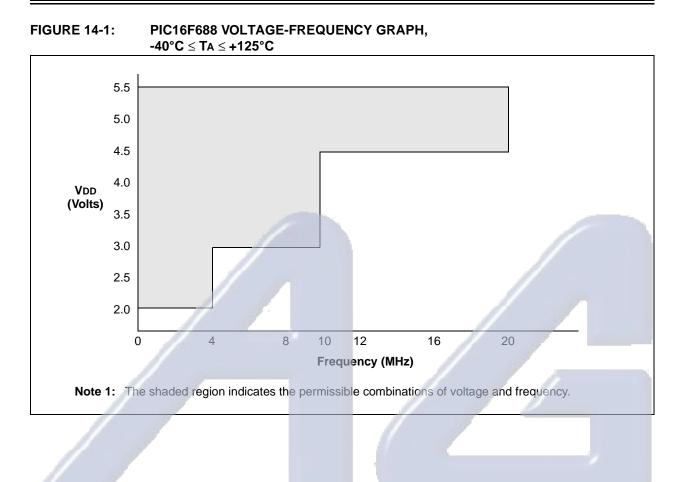
Note: Voltage spikes below Vss at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the $\overline{\text{MCLR}}$ pin, rather than pulling this pin directly to Vss.

"ALA

CU D

www.agelectronica.com

PIC16F688



Electrónica S.A. de C.V.

Preliminary

14.1 DC Characteristics: PIC16F688 -I (Industrial) PIC16F688 -E (Extended)

			Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended						
Param No.	Min	Тур†	Max	Units	Conditions				
	Vdd	Supply Voltage							
D001			2.0		5.5	V	Fosc < = 4 MHz:		
D001C			3.0	—	5.5	V	Fosc < = 10 MHz		
D001D			4.5	—	5.5	V	Fosc < = 20 MHz		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	1.5*		_	V	Device in Sleep mode		
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	-	Vss	_	V	See Section 11.4.2 "Power-On Reset (POR)" for details.		
D004	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05*	-	_	V/ms	See Section 11.4.2 "Power-On Reset (POR)" for details.		
D005	VBOD	Brown-out Detect		2.1	—	V			

These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

Electrónica S.A. de C.V.

^{© 2004} Microchip Technology Inc.

14.2 DC Characteristics: PIC16F688-I (Industrial)

DC Cha	racteristics	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial								
Param Device Characteristic		Min	Tunt	Mox	Units	Conditions				
No.	Device Characteristics	IVIIII	Тур†	Max	Units	Vdd	Note			
D010	Supply Current (IDD) ^(1, 2)	-	9	TBD	μA	2.0	Fosc = 32 kHz			
		—	18	TBD	μA	3.0	LP Oscillator mode			
		—	35	TBD	μA	5.0				
D011			110	TBD	μA	2.0	Fosc = 1 MHz			
		-	190	TBD	μA	3.0	XT Oscillator mode			
		/	330	TBD	μA	5.0				
D012		Ŧ	220	TBD	μA	2.0	Fosc = 4 MHz			
		/-	370	TBD	μA	3.0	XT Oscillator mode			
			0.6	TBD	mA	5.0				
D013			70	TBD	μA	2.0	Fosc = 1 MHz			
			140	TBD	μA	3.0	EC Oscillator mode			
		—	260	TBD	μA	5.0				
D014			180	TBD	μA	2.0	Fosc = 4 MHz			
		_	320	TBD	μΑ	3.0	EC Oscillator mode			
		—	580	TBD	μA	5.0				
D015		—	TBD	TBD	μA	2.0	Fosc = 31 kHz			
		—	TBD	TBD	μA	3.0	INTRC mode			
		—	TBD	TBD	mA	5.0				
D016		—	340	TBD	μA	2.0	Fosc = 4 MHz			
		_	500	TBD	μA	3.0	INTOSC mode			
		-	0.8	TBD	mA	5.0				
D017			180	TBD	μΑ	2.0	Fosc = 4 MHz			
$T \geq 1$	Inatuch		320	TBD	μA	3.0	EXTRC mode			
IT.I	<u> RELEA</u>	14	580	TBD	μA	5.0				
D018			2.1	TBD	mA	4.5	Fosc = 20 MHz			
		—	2.4	TBD	mA	5.0	HS Oscillator mode			

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

DC Cha	racteristics	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial									
Param						Conditions					
No.	Device Characteristics	Min	Тур†	Max	Units	Vdd	Note				
D020	Power-down Base	—	0.99	TBD	nA	2.0	WDT, BOD, Comparators, VREF and				
	Current (IPD) ⁽⁴⁾		1.2	TBD	nA	3.0	T1OSC disabled				
			2.9	TBD	nA	5.0					
D021		—	0.3	TBD	μA	2.0	WDT Current				
		-	1.8	TBD	μΑ	3.0					
		14	8.4	TBD	μA	5.0					
D022			58	TBD	μΑ	3.0	BOD Current				
		_	109	TBD	μΑ	5.0					
D023		F	3.3	TBD	μΑ	2.0	Comparator Current ⁽³⁾				
		<u> </u>	6.1	TBD	μΑ	3.0					
		_	11.5	TBD	μΑ	5.0					
D024			58	TBD	μΑ	2.0	CVREF Current				
		_	85	TBD	μA	3.0					
			138	TBD	μA	5.0					
D025			4.0	TBD	μΑ	2.0	T1OSC Current				
			4.6	TBD	μΑ	3.0					
J			6.0	TBD	μΑ	5.0					
D026			1.2	TBD	nA	3.0	A/D Current				
	1	_	0.0022	TBD	μΑ	5.0					

14.3 DC Characteristics: PIC16F688-I (Industrial)

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- **Note 3:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.
 - 4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in hi-impedance state and tied to VDD.

 $[\]ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

14.4 DC Characteristics: PIC16F688-E (Extended)

DC Cha	racteristics	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended								
Param	Device Characteristics	Min	Trust	May	Units	Conditions				
No.	Device Characteristics	WIIN	Тур†	Max		Vdd	Note			
D010E	Supply Current (IDD)		9	TBD	μA	2.0	Fosc = 32 kHz			
		_	18	TBD	μA	3.0	LP Oscillator mode			
		_	35	TBD	μA	5.0				
D011E			110	TBD	μA	2.0	Fosc = 1 MHz			
		_	190	TBD	μA	3.0	XT Oscillator mode			
			330	TBD	μΑ	5.0				
D012E		H	220	TBD	μΑ	2.0	Fosc = 4 MHz			
		—	370	TBD	μA	3.0	XT Oscillator mode			
		_	0.6	TBD	mA	5.0				
D013E			70	TBD	μA	2.0	Fosc = 1 MHz			
			140	TBD	μA	3.0	EC Oscillator mode			
			260	TBD	μA	5.0				
D014E			180	TBD	μA	2.0	Fosc = 4 MHz			
			320	TBD	μA	3.0	EC Oscillator mode			
		—	580	TBD	μA	5.0	1. 1			
D015E			TBD	TBD	μA	2.0	Fosc = 31 kHz			
		—	TBD	TBD	μA	3.0	INTRC mode			
		—	TBD	TBD	mA	5.0				
D016E			340	TBD	μA	2.0	Fosc = 4 MHz			
			500	TBD	μA	3.0	INTOSC mode			
		—	0.8	TBD	mA	5.0				
D017E	-		180	TBD	μA	2.0	FOSC = 4 MHz			
12	Lootno		320	TBD	μA	3.0	EXTRC mode			
<u></u>	i e canti da		580	TBD	μA	5.0				
D018E		_	2.1	TBD	mA	4.5	Fosc = 20 MHz			
		—	2.4	TBD	mA	5.0	HS Oscillator mode			

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

DC Cha	racteristics	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended								
Param Device Characteristics		Min	Тур†	Max	Units	Conditions				
No.					•	VDD	Note			
D020E	Power-down Base	—	0.00099	TBD	μA	2.0	WDT, BOD, Comparators, VREF			
	Current (IPD) ⁽⁴⁾	—	0.0012	TBD	μΑ	3.0	and T1OSC disabled			
		—	0.0029	TBD	μA	5.0				
D021E		—	0.3	TBD	μΑ	2.0	WDT Current			
		_	1.8	TBD	μA	3.0				
		14	8.4	TBD	μA	5.0				
D022E		<i>6</i>) —	58	TBD	μA	3.0	BOD Current			
			109	TBD	μA	5.0				
D023E		-	3.3	TBD	μA	2.0	Comparator Current ⁽³⁾			
		· —	6.1	TBD	μA	3.0				
			11.5	TBD	μA	5.0				
D024E			58	TBD	μA	2.0	CVREF Current			
		—	85	TBD	μA	3.0				
		_	138	TBD	μA	5.0				
D025E			4.0	TBD	μA	2.0	T1OSC Current			
			4.6	TBD	μA	3.0				
1		—	6.0	TBD	μΑ	5.0				
D026E			0.0012	TBD	μΑ	3.0	A/D Current ⁽³⁾			
		—	0.0022	TBD	μΑ	5.0				

14.5 DC Characteristics: PIC16F688-E (Extended)

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- **Note 3:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral \triangle current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.
 - 4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

 $[\]ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

14.6 DC Characteristics: PIC16F688 -I (Industrial) PIC16F688 -E (Extended)

DC CHA	RACT	ERISTICS	Standard Opera Operating tempe	Conditions (unless otherwise stated) e $-40^{\circ}C \le Ta \le +85^{\circ}C$ for industrial $-40^{\circ}C \le Ta \le +125^{\circ}C$ for extended			
Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
	Vil	Input Low Voltage					
		I/O port:					
D030		with TTL buffer	Vss	—	0.8	V	$4.5V \le VDD \le 5.5V$
D030A			Vss	—	0.15 Vdd	V	Otherwise
D031		with Schmitt Trigger buffer	Vss	—	0.2 Vdd	V	Entire range
D032		MCLR, OSC1 (RC mode)	Vss	—	0.2 Vdd	V	
D033		OSC1 (XT and LP modes) ⁽¹⁾	Vss	—	0.3	V	
D033A		OSC1 (HS mode) ⁽¹⁾	Vss	—	0.3 Vdd	V	
	Vih	Input High Voltage	1				
		I/O port:		—			
D040		with TTL buffer	2.0	—	Vdd	V	$4.5V \leq VDD \leq 5.5V$
D040A			(0.25 VDD + 0.8)	—	Vdd	V	Otherwise
D041		with Schmitt Trigger buffer	0.8 Vdd	—	Vdd	V	Entire range
D042		MCLR	0.8 VDD	—	VDD	V	
D043		OSC1 (XT and LP modes)	1.6	—	Vdd	V	(Note 1)
D043A		OSC1 (HS mode)	0.7 VDD	—	VDD	V	(Note 1)
D043B		OSC1 (RC mode)	0.9 VDD	-//	Vdd	V	
D070	IPUR	PORTA Weak Pull-up	50*	250	400*	μA	VDD = 5.0V, VPIN = VSS
	0	Current					
	li∟	Input Leakage Current ⁽²⁾					
D060	1	I/O port	_	± 0.1	± 1	μΑ	$VSS \leq VPIN \leq VDD$,
		(2)		_			Pin at high-impedance
D061		MCLR ⁽³⁾	—	± 0.1	±5	μA	$VSS \leq VPIN \leq VDD$
D063	-	OSC1	_	± 0.1	± 5	μA	VSS \leq VPIN \leq VDD, XT, HS and
	Ver		100 M			_	LP osc configuration
	VOL	Output Low Voltage	1878 <i>8.</i>		A.		and the second sec
D080		1/O port		ا عبي ا	0.6		10L = 8.5 mA, VDD = 4.5 V (Ind.)
D083		OSC2/CLKOUT (RC mode)	_		0.6	V	IOL = 1.6 mA, VDD = 4.5V (Ind.) IOL = 1.2 mA, VDD = 4.5V (Ext.)
	Vон	Output High Voltage					
D090		I/O port	Vdd - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V (Ind.)
D092		OSC2/CLKOUT (RC mode)	VDD - 0.7	-	—	V	IOH = -1.3 mA, VDD = 4.5V (Ind.) IOH = -1.0 mA, VDD = 4.5V (Ext.)

These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

14.7 DC Characteristics: PIC16F688 -I (Industrial), PIC16F688 -E (Extended)

DC CHAI	RACTERI	ISTICS	Operating temperature -4				tons (unless otherwise stated) $40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $40^{\circ}C \le TA \le +125^{\circ}C$ for extended		
Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions		
D100	IULP	Ultra Low-Power Wake-up Current	—	200		nA			
		Capacitive Loading Specs on Output Pins							
D100	COSC2	OSC2 pin		_	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1		
D101	Сю	All I/O pins	_	—	50*	pF			
		Data EEPROM Memory							
D120	ED	Byte Endurance	100K	1M	—	E/W	$-40^{\circ}C \le TA \le +85^{\circ}C$		
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA <mark>≤ +</mark> 125°C		
D121	Vdrw	VDD for Read/Write	VMIN	_	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage		
D122	TDEW	Erase/Write Cycle Time	_	5	6	ms			
D123	TRETD	Characteristic Retention	40	-	-	Year	Provided no other specification are violated		
D124	TREF	Number of Total Erase/Write Cycles before Refresh ⁽⁴⁾	1M	10M	-/	E/W	-40°C ≤ TA ≤ +85°C		
11	1	Program Flash Memory			20				
D130	EP	Cell Endurance	10K	100K	—	E/W	$-40^{\circ}C \le TA \le +85^{\circ}C$		
D130A	ED	Cell Endurance	1K	10K	—	E/W	$+85^{\circ}C \le TA \le +125^{\circ}C$		
D131	Vpr	VDD for Read	VMIN		5.5	V	Vмin = Minimum operating voltage		
D132	VPEW	VDD for Erase/Write	4.5		5.5	V			
D133	TPEW	Erase/Write cycle time	ni -	2	2.5	ms			
D134	TRETD	Characteristic Retention	40	Jak	1.	Year	Provided no other specification are violated		

These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 4: See Section 9.0 "Data EEPROM And Flash Program Memory Control" for additional information.

 $\ensuremath{\textcircled{}^{\circ}}$ 2004 Microchip Technology Inc.

PIC16F688

14.8 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

15 pF

for OSC2 output

1. TppS2ppS	3
-------------	---

2. TppS т F Т Frequency Time Lowercase letters (pp) and their meanings: рр RC OSC1 СС osc CLKOUT rd RD ck RD or WR CS CS rw SCK di SDI sc SS SDO do SS dt Data in t0 **T0CKI** T1CKI I/O port io t1 MCLR WR mc wr Uppercase letters and their meanings: S F Fall Ρ Period Rise Н High R Invalid (High-impedance) V Valid T Low Ζ **High-impedance** Т **FIGURE 14-2:** LOAD CONDITIONS Load Condition 1 Load Condition 2 VDD/2 RL CL CL Pin Vss Vss $RL = 464\Omega$ CL = 50 pF for all pins

DS41203B-page 144

14.9 AC Characteristics: PIC16F688 (Industrial, Extended)

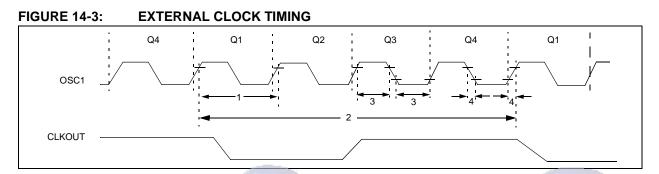


TABLE 14-1: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
	Fosc	External CLKIN Frequency ⁽¹⁾	DC	—	37	kHz	LP Oscillator mode
		1	DC	—	4	MHz	XT Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	—	20	MHz	EC Oscillator mode
		Oscillator Frequency ⁽¹⁾	5	_	37	kHz	LP Oscillator mode
				4	_	MHz	INTOSC mode
			DC		4	MHz	RC Oscillator mode
			0.1	-	4	MHz	XT Oscillator mode
	1		1	-	20	MHz	HS Oscillator mode
1	Tosc	External CLKIN Period ⁽¹⁾	27	-	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	μs	LP Oscillator mode
			50	_	~~~~	ns	HS Oscillator mode
			50	_	~	ns	EC Oscillator mode
		_	250	-	~	ns	XT Oscillator mode
7 8	. and i	Oscillator Period ⁽¹⁾	_ 27	1	200	μs	LP Oscillator mode
, # @ 4	19 - 1	#-4 b ########	-	250	A .	ns	INTOSC mode
			250	<u>~</u> =		ns	RC Oscillator mode
			250	_	10,000	ns	XT Oscillator mode
			50	_	1,000	ns	HS Oscillator mode
2	Тсү	Instruction Cycle Time ⁽¹⁾	200	Тсү	DC	ns	Tcy = 4/Fosc
3	TosL,	External CLKIN (OSC1) High	2*	_	—	μs	LP oscillator, Tosc L/H duty cyc
	TosH	External CLKIN Low	20*	_	—	ns	HS oscillator, Tosc L/H duty cyc
			100 *	_	—	ns	XT oscillator, Tosc L/H duty cyc
4	TosR,	External CLKIN Rise	—	_	50*	ns	LP oscillator
	TosF	External CLKIN Fall	_	_	25*	ns	XT oscillator
					15*	ns	HS oscillator

These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at 'min' values with an external clock applied to OSC1 pin. When an external clock input is used, the 'max' cycle time limit is 'DC' (no clock) for all devices.

© 2004 Microchip Technology Inc.

PIC16F688

TABLE 14-2: PRECISION INTERNAL OSCILLATOR PARAMETERS

Standard	d Operating	Conditions	(unless	otherwise stated)

Operating Temperature-40°C \leq TA \leq +125°C	
--	--

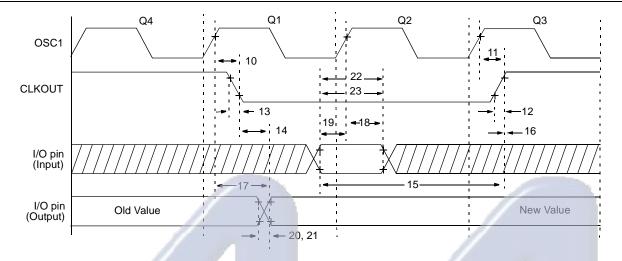
operating	Tempe	Talule-40 C \leq TA \leq +125 C						
Param No.	Sym	Characteristic	Freq Tolerance	Min	Тур†	Max	Units	Conditions
F10	Fosc	Internal Calibrated	±1%	_	8.00	TBD	MHz	VDD and Temperature TBD
		INTOSC Frequency ⁽¹⁾	±2%	—	8.00	TBD	MHz	$2.5V \le VDD \le 5.5V$ $0^{\circ}C \le TA \le +85^{\circ}C$
			±5%	_	8.00	TBD	MHz	$2.0V \le VDD \le 5.5V$ -40°C ≤ TA ≤ +85°C (Ind.) -40°C ≤ TA ≤ +125°C (Ext.)
F14	Tiosc	Oscillator Wake-up from	-	1	TBD	TBD	μs	$VDD = 2.0V, -40^{\circ}C \text{ to } +85^{\circ}C$
	ST	Sleep Start-up Time*	/-		TBD	TBD	μs	VDD = 3.0V, -40°C to +85°C
			_		TBD	TBD	μs	VDD = 5.0V, -40°C to +85°C

Legend: TBD = To Be Determined

- * These parameters are characterized but not tested.
- † Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- **Note 1:** To ensure these oscillator frequency tolerances, VDD and Vss must be capacitively decoupled as close to the device as possible. 0.1 uF and 0.01 uF values in parallel are recommended.

Electrónica S.A. de C.V.





CLKOUT AND I/O TIMING REQUIREMENTS TABLE 14-3:

operating i		$10^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$				1	
Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
10	TosH2ckL	OSC1 [↑] to CLOUT		75	200	ns	(Note 1)
11	TosH2ckH	OSC1↑ to CLOUT↑	/ - /	75	200	ns	(Note 1)
12	TckR	CLKOUT Rise Time		35	100	ns	(Note 1)
13	TckF	CLKOUT Fall Time		35	100	ns	(Note 1)
14	TckL2ioV	CLKOUT↓ to Port Out Valid	_		20	ns	(Note 1)
15	TioV2ckH	Port In Valid before CLKOUT↑	Tosc + 200 ns	—	_	ns	(Note 1)
16	TckH2iol	Port In Hold after CLKOUT1	0	—	_	ns	(Note 1)
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port Out Valid	A I	50	150*	ns	
\overline{u}		\boldsymbol{v}	a - 1.0		300	ns	e
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port Input Invalid (I/O in hold time)	100		—	ns	
19	TioV2osH	Port Input Valid to OSC1↑ (I/O in setup time)	0	—	_	ns	
20	TioR	Port Output Rise Time	_	10	40	ns	
21	TioF	Port Output Fall Time	_	10	40	ns	
22	Tinp	INT Pin High or Low Time	25	—	_	ns	
23	Trbp	PORTA change INT high or low time	Тсү	—	—	ns	

* These parameters are characterized but not tested.

- † Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated.
- Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x Tosc.

PIC16F688

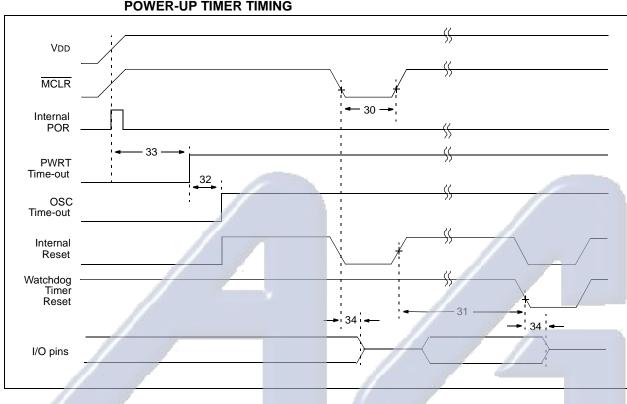
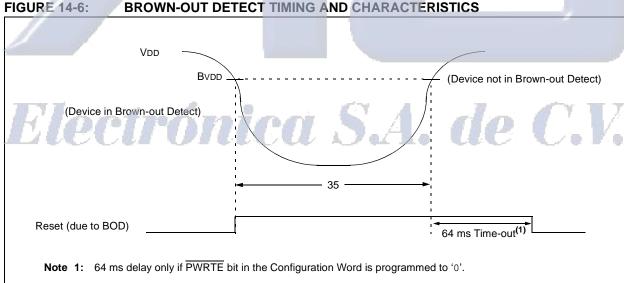


FIGURE 14-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



DS41203B-page 148

© 2004 Microchip Technology Inc.

TABLE 14-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT DETECT REQUIREMENTS

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2 11		 24	μs ms	VDD = 5V, -40°C to +85°C Extended temperature
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	10 10	17 17	25 30	ms ms	VDD = 5V, -40°C to +85°C Extended temperature
32	Tost	Oscillation Start-up Timer Period	_	1024Tosc	_	—	Tosc = OSC1 period
33*	TPWRT	Power-up Timer Period	28* TBD	64 TBD	132* TBD	ms ms	VDD = 5V, -40°C to +85°C Extended Temperature
34	Tioz	I/O High-impedance from MCLR Low or Watchdog Timer Reset	_	_	2.0	μs	
	Bvdd	Brown-out Detect Voltage	2.025	_	2.175	V	
35	TBOD	Brown-out Detect Pulse Width	100*	_ //	_	μs	$VDD \leq BVDD (D005)$

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Electrónica S.A. de C.V.

 $[\]ensuremath{\textcircled{}^{\circ}}$ 2004 Microchip Technology Inc.

PIC16F688

TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS **FIGURE 14-7:**

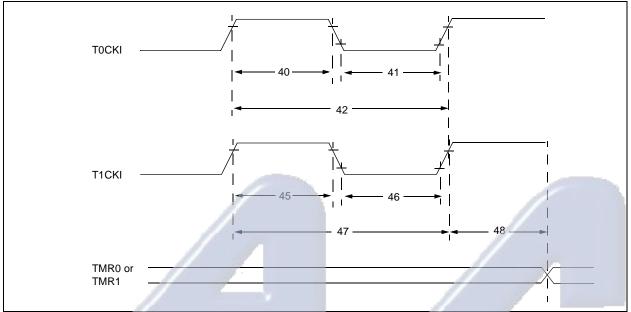


TABLE 14-5:	TIMERO AND TIMER	1 EXTERNAL CLOCK REQUIREMENT	S
-------------	------------------	-------------------------------------	---

41* Tti 42* Tti	it1H	TOCKI High Pu TOCKI Low Pul TOCKI Period T1CKI High	se Width	No Prescaler With Prescaler No Prescaler With Prescaler	0.5 TCY + 20 10 0.5 TCY + 20 10 Greater of: 20 or <u>TCY + 40</u> N			ns ns ns ns	N = prescale
42* Tt	t0P	T0CKI Period		No Prescaler With Prescaler	0.5 TCY + 20 10 Greater of: 20 or <u>TCY + 40</u>			ns ns	
42* Tt	t0P	T0CKI Period		With Prescaler	10 Greater of: 20 or <u>Tcy + 40</u>			ns	
	it1H	T1CKI High	Synchropou		Greater of: 20 or <u>Tcy + 40</u>				
	it1H	T1CKI High	Synchronou		20 or <u>TCY + 40</u>			ns	
45* Tt			Synchronou						
.45* Tt			Synchronou						value (2, 4, , 256)
141	100.00		Logine in on lou	is, No Prescaler	0.5 TCY + 20	-		ns	, 200)
			Synchronou with Prescal		15	Th.	0	ns	
			Asynchronous		30	_	-	ns	
46* Tt	ˈt1L	T1CKI Low	Synchronou	is, No Prescaler	0.5 TCY + 20			ns	
		Time	Synchronou with Prescal		15	_	—	ns	
			Asynchronous		30	_	—	ns	
47* Tt		T1CKI Input Period	Synchronou	IS	Greater of: 30 or <u>Tcy + 40</u> N	_		ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		60		_	ns	
Ft	ït1	Timer1 oscillato (oscillator enab		ency range g bit T1OSCEN)	DC	—	200*	kHz	
48 TC		Delay from externation increment	ernal clock eo	dge to timer	2 Tosc*	—	7 Tosc*	—	

These parameters are characterized but not tested.

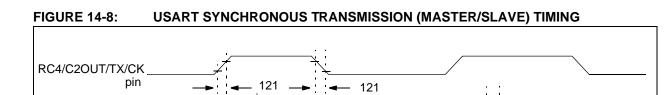
Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only t and are not tested.

DS41203B-page 150

© 2004 Microchip Technology Inc.

RC5/RX/DT pin

Note:



122

TABLE 14-6: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

120

Refer to Figure 14-2 for load conditions.

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (Master & Slave) Clock high to data-out valid	PIC16F688		40	ns	
		Clock high to data-out valu	PIC16LF688	7	100	ns	
121	Tckrf 🥢	Clock out rise time and fall time	PIC16F688	/_	20	ns	_0
		(Master mode)	PIC16LF688	_	50	ns	
122	Tdtrf	Data-out rise time and fall time	PIC16F688	- 7	20	ns	
		7	PIC16LF688	-	50	ns	

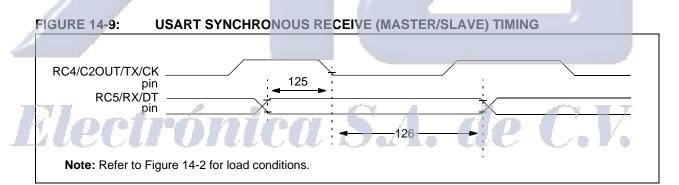


TABLE 14-7: USART SYNCHRONOUS RECEIVE REQUIREMENTS

	Standard Operating Conditions (unless otherwise stated) Operating Temperature-40°C \leq TA \leq +125°C								
Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions			
125	TdtV2ckl	<u>SYNC RCV (Master & Slave)</u> Data-hold before CK ↓ (DT hold time)	10		ns				
126	TckL2dtl	Data-hold after CK \downarrow (DT hold time)	15	_	ns				

DS41203B-page 151

 $[\]ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

PIC16F688

TABLE 14-8: COMPARATOR SPECIFICATIONS

Comparate	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$						
Sym	Characteristics	Min	Тур	Max	Units	Comments	
Vos	Input Offset Voltage	—	± 5.0	± 10	mV		
Vсм	Input Common Mode Voltage	0		Vdd - 1.5	V		
CMRR	Common Mode Rejection Ratio	+55*		_	db		
Trt	Response Time ⁽¹⁾	—	150	400*	ns		
Тмс2coV	Comparator Mode Change to Output Valid	-		10*	μs		

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD - 1.5)/2 while the other input transitions from Vss to VDD - 1.5V.

TABLE 14-9: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

Voltage Reference Specifications		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$						
Sym.	Characteristics	Min Typ Ma		Max	Units	Comments		
	Resolution	_	VDD/24* VDD/32	1	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)		
	Absolute Accuracy	_	=	± 1/4* ± 1/2*	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)		
	Unit Resistor Value (R)	_	2K*	- (Ω			
	Settling Time ⁽¹⁾	_	—	10*	μs			
*	* These parameters are characterized but not tested.							

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.



TABLE 14-10: PIC16F688 A/D CONVERTER CHARACTERISTICS:

Standard Operating Conditions	(unless otherwise stated)
-------------------------------	---------------------------

Temperature-40°C < Ta < +125°C

Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
A01	Nr	Resolution	_	-	10 bits	bit	
A02	Eabs	Total Absolute Error* ⁽¹⁾	—	_	±1	LSb	VREF = 5.0V
A03	EIL	Integral Error	_	_	±1	LSb	VREF = 5.0V
A04	Edl	Differential Error	_		±1	LSb	No missing codes to 10 bits VREF = 5.0V
A05	Efs	Full-scale Range	2.2*	-	5.5*	V	
A06	EOFF	Offset Error	/_		±1	LSb	VREF = 5.0V
A07	Egn	Gain Error			±1	LSb	VREF = 5.0V
A10	—	Monotonicity	7	guaranteed ⁽²⁾	_		$VSS \leq VAIN \leq VREF+$
A20 A20A	Vref	Reference Voltage	2.2 2.5	—	 Vdd + 0.3	V	Absolute minimum to ensure 10-bit accuracy
A25	VAIN	Analog Input Voltage	Vss	—	VREF	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	-	-	10	kΩ	
A50	IREF	VREF Input Current* ⁽³⁾	10	—	1000	μΑ	During VAIN acquisition. Based on differential of VHOLD to VAIN.
	1		_		10	μA	During A/D conversion cycle.

These parameters are characterized but not tested.

Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance † only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2. The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

- 3: VREF current is from external VREF or VDD pin, whichever is selected as reference input.
- 4: When A/D is off, it will not consume any current other than leakage current. The power-down current _specification includes any such leakage from the A/D module.

PIC16F688



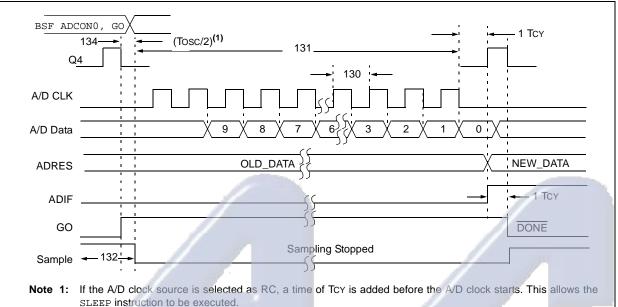


TABLE 14-11: PIC16F688 A/D CONVERSION REQUIREMENTS

		ting Conditions (unleaded on the condition of the conditions of the condition of the condi		ise stated)			
Param No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
130	TAD	A/D Clock Period	1.6	—		μs	Tosc-based, VREF ≥ 3.0V
130	Tad	A/D Internal RC Oscillator Period	3.0* 3.0*	6.0	9.0*	μs μs	TOSC-based, VREF full range ADCS<1:0> = 11 (RC mode) At VDD = 2.5V
151	1	and the market of the	2.0*	4.0	6.0*	μs	At VDD = 5.0V
131	TCNV	Conversion Time (not including Acquisition Time) ⁽¹⁾	TEC.		Sat	TAD	Set GO bit to new data in A/D Result register
132	TACQ	Acquisition Time		11.5	—	μs	
			5*	_	_	μs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).
134	TGO	Q4 to A/D Clock Start	—	Tosc/2	_		If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRESH and ADRESL registers may be read on the following TCY cycle.

2: See Table 8-1 for minimum conditions.

DS41203B-page 154

 $\ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.



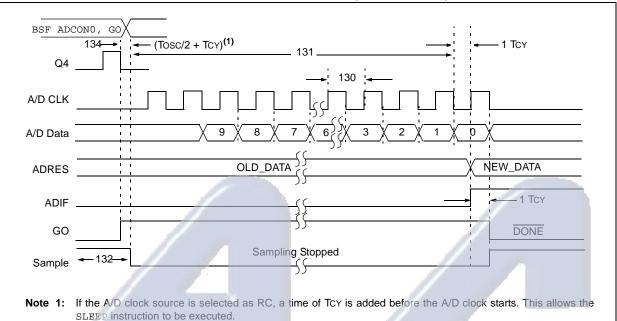


TABLE 14-12: PIC16F688 A/D CONVERSION REQUIREMENTS (SLEEP MODE)

Standard Operating Conditions (unless otherwise stated) Operating Temperature-40°C \leq TA \leq +125°C									
Param No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions		
130	Tad	A/D Internal RC Oscillator Period	3.0* 2.0*	6.0 4.0	9.0* 6.0*	μs us	ADCS<1:0> = 11 (RC mode) At VDD = 2.5V At VDD = 5.0V		
131	Tcnv	Conversion Time (not including Acquisition Time) ⁽¹⁾	lēa	i 15.	Â.	TAD	le C.V.		
132	TACQ	Acquisition Time	(2)	11.5		μs			
			5*	_		μs	The minimum time is the amplifie settling time. This may be used i the "new" input voltage has not changed by more than 1 LSb (i.e 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).		
134	TGO	Q4 to A/D Clock Start		Tosc/2 + Tcy	_		If the A/D clock source is selecte as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to b executed.		

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Table 8-1 for minimum conditions.

© 2004 Microchip Technology Inc.

www.agelectronica.com

DS41203B-page 155

PIC16F688

NOTES:



Electrónica S.A. de C.V.

DS41203B-page 156

Preliminary

© 2004 Microchip Technology Inc.

www.agelectronica.com

15.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Graphs are not available at this time.



Electrónica S.A. de C.V.

DS41203B-page 157

^{© 2004} Microchip Technology Inc.

PIC16F688

NOTES:



Electrónica S.A. de C.V.

DS41203B-page 158

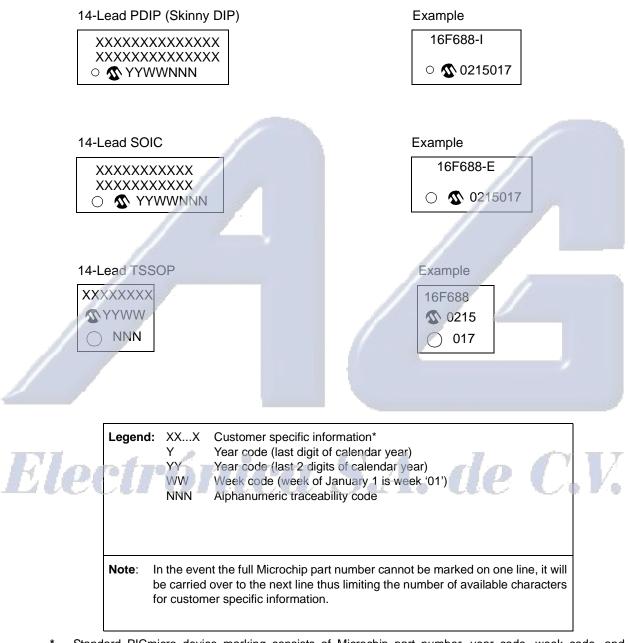
Preliminary

© 2004 Microchip Technology Inc.

www.agelectronica.com

16.0 PACKAGING INFORMATION

16.1 Package Marking Information



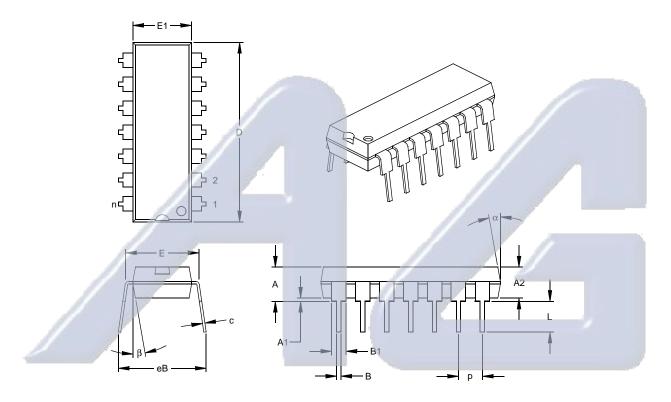
* Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

 $[\]ensuremath{\textcircled{}^{\circ}}$ 2004 Microchip Technology Inc.

16.2 **Package Details**

The following sections give the technical details of the packages.

14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)





	Units		INCHES*			MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX	F	
Number of Pins	n		14			_14			
Pitch	р		.100			2.54			
Top to Seating Plane	Α	.140	.155	.170	3.56	3.94	4.32		
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68		
Base to Seating Plane	A1	.015			0.38				
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26		
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60		
Overall Length	D	.740	.750	.760	18.80	19.05	19.30		
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43		
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38		
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78		
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56		
Overall Row Spacing §	eВ	.310	.370	.430	7.87	9.40	10.92		
Mold Draft Angle Top	α	5	10	15	5	10	15		
Mold Draft Angle Bottom	β	5	10	15	5	10	15		

* Controlling Parameter § Significant Characteristic

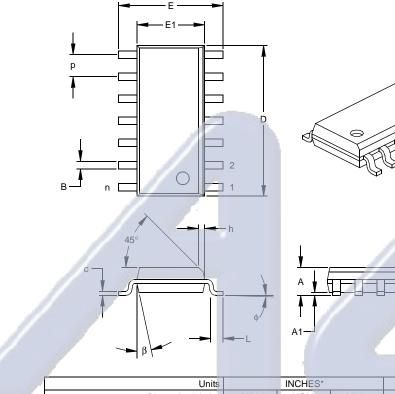
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-001 Drawing No. C04-005

8

A2

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



Ele

		INCHES*		MILLIMETERS			
Dimensior	1 Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	р		.050			1.27	
Overall Height	А	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.8
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.5
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	С	.008	.009	.010	0.20	0.23	0.2
Lead Width	В	.014	.017	.020	0.36	0.42	0.5
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	1:

* Controlling Parameter § Significant Characteristic

Notes:

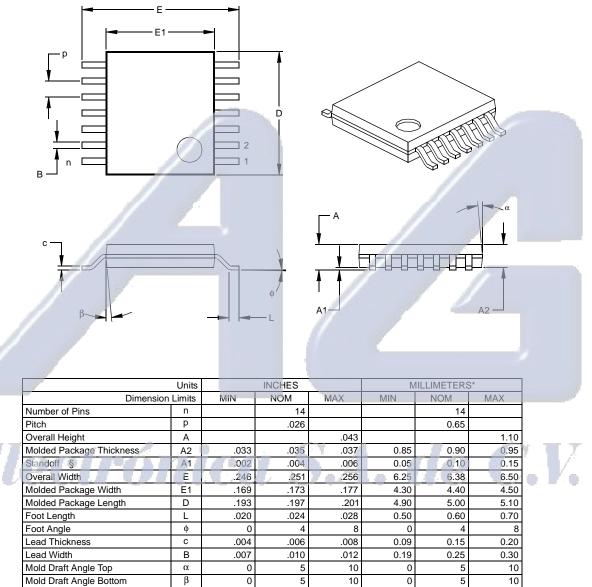
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-012

Drawing No. C04-065



PIC16F688

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side. JEDEC Equivalent: MO-153

Drawing No. C04-087

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

This is a new data sheet.

Revision B

Rewrites of the Oscillator and Special Features of the CPU Sections. General corrections to Figures and formatting.



Electrónica S

APPENDIX B: MIGRATING FROM OTHER PICmicro® DEVICES

This discusses some of the issues in migrating from other PICmicro devices to the PIC16F6XX family of devices.

B.1 PIC16F676 to PIC16F688

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F676	PIC16F688
Max Operating Speed	20 MHz	20 MHz
Max Program Memory (Words)	1024	4K
SRAM (Bytes)	64	256
A/D Resolution	10-bit	10-bit
Data EEPROM (bytes)	128	256
Timers (8/16-bit)	1/1	1/1
Oscillator Modes	8	8
Brown-out Detect	Y	Y
Internal Pull-ups	RA0/1/2/4/5	RA0/1/2/4/5, MCLR
Interrupt-on-change	RA0/1/2/3 /4/5	RA0/1/2/3/4/5
Comparator	1	2
EUSART	N	Y
Ultra Low-Power Wake-up	Ν	Y
Extended WDT	N	Y
Software Control Option of WDT/BOD	N	Ť,
INTOSC Frequencies	4 MHz	32 kHz - 8 MHz
Clock Switching	Ν	Y

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

PIC16F688

NOTES:



Electrónica S.A. de C.V.

DS41203B-page 164

Preliminary

© 2004 Microchip Technology Inc.

www.agelectronica.com

INDEX

	٨
1	ч

A/D	
Acquisition Requirements	68
Analog Port Pins	63
Associated Registers	70
Block Diagram	63
Calculating Acquisition Time	68
Channel Selection	63
Configuration and Operation	63
Configuring	67
Configuring Interrupt	67
Conversion (TAD) Cycles	65
Conversion Clock	64
Effects of Reset	70
Internal Sampling Switch (Rss) Impedance	68
Operation During Sleep	
Output Format	
Reference Voltage (VREF)	
Source Impedance	68
Specifications 153	, 154, 155
Starting a Conversion	64
TAD vs. Operating Frequencies	
Absolute Maximum Ratings	
AC Characteristics	
Industrial and Extended	
Load Conditions	
ADCON0 Register	
ADCON1 Register	66
Analog Front-end (AFE)	
Power-On Reset	
Analog Input Connections	54
Analog-to-Digital Converter Module. See A/D	
ANSEL Register	65
Assembler	
MPASM Assembler	
Auto Wake-up on SYNC Break Character	91

В

BAUDCTL Register..... Block Diagrams

K Diagranis	1 1 1 1 1 1 1 1
A/D	63
Analog Input Model	55, 68
Comparator 1	57
Comparator 2	
Comparator Modes	
Comparator Voltage Reference (CVREF)	59
Fail-Safe Clock Monitor (FSCM)	28
In-Circuit Serial Programming Connections	117
Interrupt Logic	
MCLR Circuit	
On-Chip Reset Circuit	
PIC16F688	5
RA1 Pins	
RA2 Pin	
RA3 Pin	37
RA4 Pin	
RA5 Pin	
RC0 and RC1 Pins	40
RC2 and RC3 Pins	
RC4 Pin	
RC5 Pin	
Resonator Operation	23
System Clock	21
Timer1	49

TMR0/WDT Prescaler	45
USART Receive	89
USART Transmit	87
Watchdog Timer (WDT)	113
Break Character (12-bit) Transmit and Receive	92
Brown-out Detect (BOD)	
Associated Registers	
Calibration	104
Specifications	149
Timing and Characteristics	148

www.agelectronica.com

PIC16F688

С

C Compilers	
MPLAB C17	130
MPLAB C18	
MPLAB C30	130
CALIB Register	101
Clock Accuracy with Asynchronous Operation	77
CMCON0 Register CMCON1 Register	58
Code Evenetee	
A/D Conversion	67
Assigning Prescaler to Timer0	47
Assigning Prescaler to WDT	
Indirect Addressing	
Initializing PORTA	
Initializing PORTC	40
Saving Status and W Registers in RAM	112
Ultra Low-Power Wake-up Initialization	
Code Protection	117
Comparator Module	53
Comparator Voltage Reference (CVREF)	
Associated Registers	61
Effects of a Reset	60
Response Time	
Comparator Voltage Reference (CVREF)	59
Accuracy/Error	59
Configuring	
Specifications	152
Comparators	
Associated Registers	
C2OUT as T1 Gate	. 50, 58
Configurations	
Effects of a Reset	
Interrupts	
Operation	
Operation During Sleep	
Outputs	
Response Time	
Specifications	
Synchronizing C2OUT w/ Timer1	
CONFIG Register	
Configuration Bits 10	
CPU Features	99

© 2004 Microchip Technology Inc.

D

Data EEPROM Memory71
Associated Registers75
Reading73
Writing73
Data Memory7
DC Characteristics
Extended and Industrial142
Industrial and Extended137
Demonstration Boards
PICDEM 1 132
PICDEM 17133
PICDEM 18R133
PICDEM 2 Plus132
PICDEM 3
PICDEM 4
PICDEM LIN
PICDEM USB133
PICDEM.net Internet/Ethernet
Development Support
Device Overview

Е

EEADR Register	72
EEADR Registers	71
EEADRH Registers	71
EECON1 Register7	1, 72
EECON2 Register	71
EEDAT Register	72
Electrical Specifications	. 135
Enhanced Universal Synchronous Asynchronous	
Receiver Transmitter (EUSART)	77
Errata	3
Evaluation and Programming Tools	. 133
F	

Fail-Safe Clock Monitor	28
Fail-Safe Mode	29
Reset and Wake-up from Sleep	29
Firmware Instructions	119
Flash Program Memory	71
Fuses. See Configuration Bits	1.17

G

General Purpose Register	File7
--------------------------	-------

I

I/O Ports
ID Locations
In-Circuit Debugger
In-Circuit Serial Programming (ICSP)
Indirect Addressing, INDF and FSR Registers
Instruction Format
Instruction Set119
ADDLW 121
ADDWF 121
ANDLW 121
ANDWF121
BCF121
BSF
BTFSC
BTFSS121
CALL
CLRF122
CLRW

	CLRWDT 122	
	COMF	
	DECF	
	DECFSZ 123	
	GOTO 123	
	INCF 123	
	INCFSZ 123	
	IORLW 124	
	IORWF 124	
	MOVF 123	
	MOVLW 124	
	MOVWF 124	
	NOP 124	
	RETFIE 125	
	RETLW 125	
	RETURN	
	RLF	
	RRF 126	
	SLEEP 126	
	SUBLW 126	
	SUBWF126	
	SWAPF 127	
	XORLW 127	
	XORWF 127	
	Summary Table 120	
	INTCON Register	
	Internal Oscillator Block	
	INTOSC	
	Specifications146	
	Internal Sampling Switch (Rss) Impedance	
	Interrupts	
	A/D	
	A/D67Associated Registers111Comparators58Context Saving112Interrupt-on-Change33PORTA Interrupt-on-Change110	
	A/D67Associated Registers111Comparators58Context Saving112Interrupt-on-Change33PORTA Interrupt-on-Change110RA2/INT110	
	A/D	
	A/D	
i.	A/D	
	A/D	
	A/D	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33	
	A/D	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33 L Load Conditions 144 M MCLR 103 Internal 103 103 Memory Organization 7 7 Pota 7 7	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33 L Load Conditions 144 M M 103 Internal 103 103 Internal 7 7 Data 7 7 Migrating from other PICmicro Devices 163	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33 L Load Conditions 144 M M 103 Internal 103 Internal 103 Memory Organization 7 Data 7 Program 7 Migrating from other PICmicro Devices 163 MPLAB ASM30 Assembler, Linker, Librarian 130	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33 L Load Conditions 144 M M 103 Internal 103 Internal 103 Memory Organization 7 Porgram 7 Migrating from other PICmicro Devices 163 MPLAB ASM30 Assembler, Linker, Librarian 130 MPLAB ICD 2 In-Circuit Debugger 131	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33 L Load Conditions Internal 103 Internal 103 Internal 103 Memory Organization 7 Program 7 Migrating from other PICmicro Devices 163 MPLAB ASM30 Assembler, Linker, Librarian 130 MPLAB ICD 2 In-Circuit Debugger 131 MPLAB ICE 2000 High-Performance Universal 131	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33 L Load Conditions Internal 103 Internal 103 Internal 103 Memory Organization 7 Data 7 Program 7 Migrating from other PICmicro Devices 163 MPLAB ASM30 Assembler, Linker, Librarian 130 MPLAB ICD 2 In-Circuit Debugger 131 MPLAB ICE 2000 High-Performance Universal 131	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33 L Load Conditions Internal 103 Internal 103 Internal 103 Memory Organization 7 Data 7 Program 7 Migrating from other PICmicro Devices 163 MPLAB ASM30 Assembler, Linker, Librarian 130 MPLAB ICD 2 In-Circuit Debugger 131 MPLAB ICE 2000 High-Performance Universal 131 In-Circuit Emulator 131 MPLAB ICE 4000 High-Performance Universal 131	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33 L Load Conditions Load Conditions 144 M MCLR MCLR 103 Internal 103 Internal 103 Memory Organization 7 Program 7 Migrating from other PICmicro Devices 163 MPLAB ASM30 Assembler, Linker, Librarian 130 MPLAB ICE 2000 High-Performance Universal 131 MPLAB ICE 4000 High-Performance Universal 131 In-Circuit Emulator 131	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33 L Load Conditions 144 M M 103 Internal 103 103 Internal 103 103 Memory Organization 7 7 Data 7 7 Program 7 7 Migrating from other PICmicro Devices 163 MPLAB ASM30 Assembler, Linker, Librarian 130 MPLAB ICD 2 In-Circuit Debugger 131 MPLAB ICE 2000 High-Performance Universal 131 In-Circuit Emulator 131 MPLAB ICE 4000 High-Performance Universal 131 In-Circuit Emulator 131 MPLAB Integrated Development Environment 131	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33 L Load Conditions Load Conditions 144 M MCLR MCLR 103 Internal 103 Internal 103 Memory Organization 7 Program 7 Migrating from other PICmicro Devices 163 MPLAB ASM30 Assembler, Linker, Librarian 130 MPLAB ICE 2000 High-Performance Universal 131 In-Circuit Emulator 131 MPLAB ICE 4000 High-Performance Universal 131 In-Circuit Emulator 131 MPLAB INtegrated Development Environment 131	
	A/D 67 Associated Registers 111 Comparators 58 Context Saving 112 Interrupt-on-Change 33 PORTA Interrupt-on-Change 110 RA2/INT 110 TMR0 110 TMR1 50 INTOSC Specifications 146 IOCA Register 33 L Load Conditions 144 M M 103 Internal 103 103 Internal 103 103 Memory Organization 7 7 Data 7 7 Program 7 7 Migrating from other PICmicro Devices 163 MPLAB ASM30 Assembler, Linker, Librarian 130 MPLAB ICD 2 In-Circuit Debugger 131 MPLAB ICE 2000 High-Performance Universal 131 In-Circuit Emulator 131 MPLAB ICE 4000 High-Performance Universal 131 In-Circuit Emulator 131 MPLAB Integrated Development Environment 131	

© 2004 Microchip Technology Inc.

0

OPCODE Field Descriptions	
OPTION_REG Register	14, 46
OSCCON Register	10, 30
Oscillator	
Associated Registers	
Oscillator Configurations	21
Oscillator Specifications	
Oscillator Start-up Timer (OST)	
Specifications	
Oscillator Switching	
Fail-Safe Clock Monitor	
Two-Speed Clock Start-up	27

Ρ

Packaging	159
Marking	
PDIP Details	
SOIC Details	
TSSOP Details	
PCL and PCLATH	10
Computed GOTO	
Stack	
PCON Register	
PICkit 1 Flash Starter Kit	
PICSTART Plus Development Programmer	
PIE1 Register	
PIE1 Register Pin Diagram	
Pinout Description	
PIC16F688	6
PIR1 Register	17
PORTA	
Additional Pin Functions	
Interrupt-on-Change	
Ultra Low-Power Wake-up	
Weak Pull-up	
Associated Registers	
Pin Descriptions and Diagrams	
RA0	
RA1	
RA2	37

RA4	
RA5	
Specifications	
PORTA Register	
PORTC	40
Associated Registers	30, 43
PA/PB/PC/PD. See Enhanced Universal	
Asynchronous Receiver	
Transmitter (EUSART)	40
Specifications	147
PORTC Register	
Power-Down Mode (Sleep)	
Power-on Reset (POR)	
Power-up Timer (PWRT)	
Specifications	149
Precision Internal Oscillator Parameters	146
Prescaler	
Shared WDT/Timer0	
Switching Prescaler Assignment	
PRO MATE II Universal Device Programmer	131
Product Identification System	
Program Memory	7
Map and Stack	
Programming, Device Instructions	119

R

ĸ	
RA3/MCLR/Vpp	7
RCREG	
RCSTA Register)
SPEN Bit	7
Read-Modify-Write Operations 119)
Register	
RCREG Register 84	ŧ
Registers	
ADCON0 (A/D Control 0) 66	5
ADCON1 (A/D Control 1) 66	3
ANSEL (Analog Select) 65	
BAUDCTL (Baud Rate Control) 80)
CALIB (Calibration Word) 101	
CMCON0 (Comparator Control 0)	
CMCON1 (Comparator Control 1)	
CONFIG (Configuration Word)	
EEADR (EEPROM Address)	
EECON1 (EEPROM Control 1)	
EEDAT (EEPROM Data)	
INTCON (Interrupt Control) 15	
IOCA (Interrupt-on-change PORTA)	
OPTION REG	
OSCCON (Oscillator Control)	
PCON (Power Control) 105	
PIE1 (Peripheral Interrupt Enable 1) 16	
PIR1 (Peripheral Interrupt Register 1) 17	
PORTA	
PORTC	
RCSTA (Receive Status and Control)	
Reset Values	
Reset Values (Special Registers) 108	
Special Function Register Map	
Special Register Summary	
Status	
T1CON (Timer1 Control)	-
TRISA (Tri-state PORTA)	
TRISC (Tri-state PORTC)	
TXSTA (Transmit Status and Control)	
VRCON (Voltage Reference Control)	
WDTCON (Watchdog Timer Control)	
WPUA (Weak Pull-up PORTA)	, ,
Reset	
Revision History	
-	-
D	

S

Software Simulator (MPLAB SIM)	130
Software Simulator (MPLAB SIM30)	130
SPBRG	81
SPBRGH	81
Special Function Registers	7
Status Register	13

т

T1CON Register Time-out Sequence	
•	
Timer0	
Associated Registers	47
External Clock	46
External Clock Requirements	150
Interrupt	45
Operation	
тоскі	

© 2004 Microchip Technology Inc.

Timer0 Module	45
Timer1	-
Associated Registers	52
Asynchronous Counter Mode	
Reading and Writing	
External Clock Requirements	
Interrupt	
Modes of Operations Operation During Sleep	
Oscillator	
Prescaler	
Timer1 Gate	
Inverting Gate	50
Selecting Source	
Synchronizing C2OUT w/ Timer1	,
TMR1H Register	
TMR1L Register	
Timer1 Module with Gate Control	
Timing Diagrams	
A/D Conversion	
A/D Conversion (Sleep Mode)	. 155
Asynchronous Reception	90
Asynchronous Transmission	
Asynchronous Transmission (Back to Back)	
Auto Wake-up Bit (WUE) During Sleep	91
Automatic Baud Rate Calculator	
Auto-Wake-up Bit (WUE) During Normal Operation	
Brown-out Detect (BOD)	
Brown-out Detect Situations	
CLKOUT and I/O	
Comparator Output	
External Clock	
Fail-Safe Clock Monitor (FSCM)	
INT Pin Interrupt	
Reset, WDT, OST and Power-up Timer Send Break Character Sequence	
Synchronous Reception (Master Mode, SREN)	
Synchronous Transmission	
Synchronous Transmission (Through TXEN)	
Time-out Sequence	
Case 3	
Timer0 and Timer1 External Clock	.150
Timer1 Incrementing Edge	50
Two Speed Start-up	28
USART Synchronous Receive (Master/Slave)	. 151
USART Synchronous Transmission (Master/Slave)	
Wake-up from Interrupt	. 116
Timing Parameter Symbology	. 144
TMR1H Register	
TMR1L Register	
TRISA	
TRISA Register	
TRISC Register	
Two-Speed Clock Start-up Mode	
TXREG.	
TXSTA Register	
BRGH Bit	81

U

Ultra Low-Power Wake-up		
Asynchronous Mode		
12-bit BreakTransmit and Receive		
Associated Registers, Receive		
Associated Registers, Transmit		
Auto Wake-up on SYNC Break		
Receiver 89		
Setting up 9-bit Mode with Address Detect 89 Baud Rate Generator (BRG)		
Auto Baud Rate Detect		
Baud Rate Error, Calculating		
Baud Rates, Asynchronous Modes		
Formulas		
High Baud Rate Select (BRGH Bit)		
Sampling		
Serial Port Enable (SPEN Bit)		
Synchronous Master Mode		
Associated Registers, Reception		
Associated Registers, Transmit		
Reception		
Requirements, Synchronous Receive		
Requirements, Synchronous Transmission 151		
Timing Diagram, Synchronous Receive		
Timing Diagram, Synchronous Transmission 151		
Transmission		
Synchronous Slave Mode		
Associated Registers, Receive		
Associated Registers, Transmit		
Reception		
Transmission		

V

Voltage Reference.	
See Comparator Voltage Reference (CVREF)	100
VRCON Register	61

W

Wake-up Using Interrupts Watchdog Timer (WDT)	
Associated Registers	114
Clock Source	113
Modes	113
Period	113
Specifications	149
WDTCON Register	9, 114
WPUA Register	32
WWW, On-Line Support	

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape[®] or Microsoft[®] Internet Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available at the following URL:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

ftp://ftp.microchip.com

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked
 Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- · Listing of seminars and events

SYSTEMS INFORMATION AND UPGRADE HOT LINE

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive the most current upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.



S.A. de C.V.

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

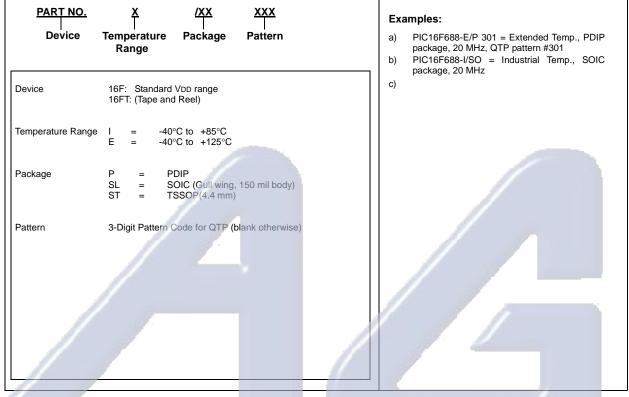
To:	roomioari abiloatorio managor	Total Pages Sent
RE	: Reader Response	
Fro	m: Name	
	Company	
	Address	
	Telephone: ()	FAX: ()
	plication (optional):	
Wo	uld you like a reply?YN	
Dev	vice: PIC16F688 Litera	ture Number: DS41203B
Que	estions:	
1.	What are the best features of this documen	t?
2.	How does this document meet your hardwa	are and software development needs?
3.	Do you find the organization of this docume	ent easy to follow? If not, why?
H	loetrónie	
4.	What additions to the document do you thin	nk would enhance the structure and subject?
5.	What deletions from the document could be	e made without affecting the overall usefulness?
6.	Is there any incorrect or misleading informa	tion (what and where)?
7.	How would you improve this document?	
	-	

DS41203B-page 170

 $\ensuremath{\textcircled{}^{\odot}}$ 2004 Microchip Technology Inc.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type.

Electrónica S.A. de C.V.

www.agelectronica.com

DS41203B-page 171