SNx400, SNx4LS00, and SNx4S00 Quadruple 2-Input Positive-NAND Gates

1 Features

- Package Options Include:
  - Plastic Small-Outline (D, NS, PS)
  - Shrink Small-Outline (DB)
  - Ceramic Flat (W)
  - Ceramic Chip Carriers (FK)
  - Standard Plastic (N)
  - Ceramic (J)
- Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package
- Inputs Are TTL Compliant; V_{IH} = 2 V and V_{IL} = 0.8 V
- Inputs Can Accept 3.3-V or 2.5-V Logic Inputs
- SN5400, SN54LS00, and SN54S00 are Characterized For Operation Over the Full Military Temperature Range of –55ºC to 125ºC

2 Applications

- AV Receivers
- Portable Audio Docks
- Blu-Ray Players
- Home Theater
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)

3 Description

The SNx4xx00 devices contain four independent, 2-input NAND gates. The devices perform the Boolean function $Y = \overline{A} \times \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LS00DB	SSOP (14)	6.20 mm × 5.30 mm
SN7400D, SN74LS00D, SN74S00D	SOIC (14)	8.65 mm × 3.91 mm
SN74LS00NSR	PDIP (14)	19.30 × 6.35 mm
SNJ5400J, SNJ54LS00J, SNJ54S00J	CDIP (14)	19.56 mm × 6.67 mm
SNJ5400W, SNJ54LS00W, SNJ54S00W	CFP (14)	9.21 mm × 5.97 mm
SN54LS00FK, SN54S00FK	LCCC (20)	8.89 mm × 8.89 mm
SN7400NS, SN74LS00NS, SN74S00NS	SO (14)	10.30 mm × 5.30 mm
SN7400PS, SN74LS00PS	SO (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram, Each Gate (Positive Logic)

Table of Contents

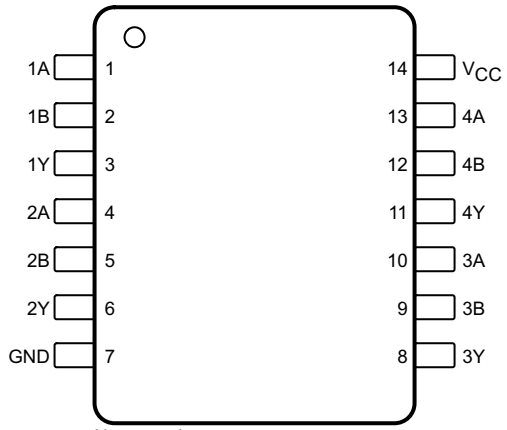
4 Revision History

Changes from Revision B (October 2003) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed *Ordering Information* table to *Device Comparison Table*; see *Package Option Addendum* at the end of the data sheet ... 1
- Changed Package thermal impedance, $R_{\theta JA}$, values in *Thermal Information* table From: 86°C/W To: 90.9°C/W (D), From: 96°C/W To: 102.8°C/W (DB), From: 80°C/W To: 54.8°C/W (N), and From: 76°C/W To: 89.7°C/W (NS) ... 5

5 Pin Configuration and Functions

SN5400 J, SN54xx00 J and W, SN74x00 D, N, and NS, or SN74LS00 D, DB, N, and NS Packages
14-Pin CDIP, CFP, SOIC, PDIP, SO, or SSOP
Top View



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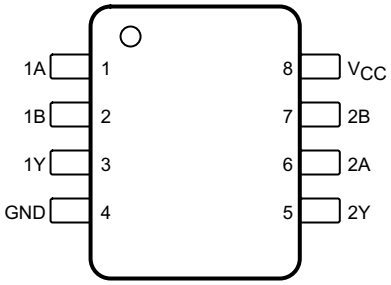
SN74xx00 PS Package
18-Pin SO
Top View



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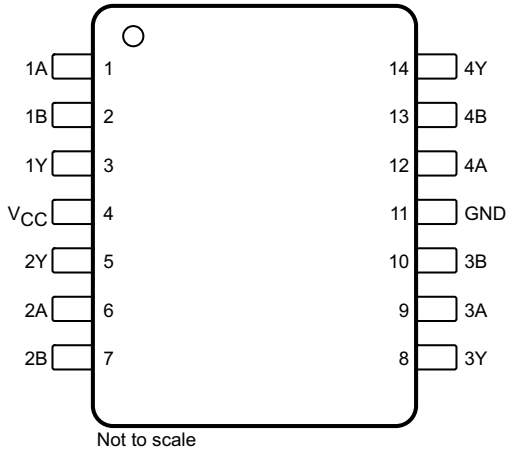
SN5400 W Package
14-Pin CFP
Top View



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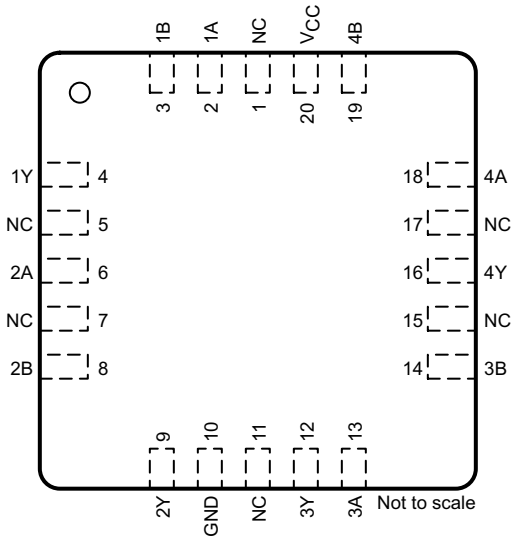
SN54xx00 FK Package
20-Pin LCCC
Top View



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Pin Functions

PIN					I/O	DESCRIPTION
NAME	CDIP, CFP, SOIC, PDIP, SO, SSOP	SO (SN74xx00)	CFP (SN5400)	LCCC		
1A	1	1	1	2	I	Gate 1 input
1B	2	2	2	3	I	Gate 1 input
1Y	3	3	3	4	O	Gate 1 output
2A	4	6	6	6	I	Gate 2 input
2B	5	7	7	8	I	Gate 2 input
2Y	6	5	5	9	O	Gate 2 output
3A	10	—	9	13	I	Gate 3 input
3B	9	—	10	14	I	Gate 3 input
3Y	8	—	8	12	O	Gate 3 output
4A	13	—	12	18	I	Gate 4 input

Pin Functions (continued)

PIN					I/O	DESCRIPTION
NAME	CDIP, CFP, SOIC, PDIP, SO, SSOP	SO (SN74xx00)	CFP (SN5400)	LCCC		
4B	12	—	13	19	I	Gate 4 input
4Y	11	—	14	16	O	Gate 4 output
GND	7	4	11	10	—	Ground
NC	—	—	—	1, 5, 7, 11, 15, 17	—	No connect
V_{CC}	14	8	4	20	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}(2)			7	V
Input voltage	SNx400 and SNxS400		5.5	V
	SNx4LS00		7	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network ground terminal.

6.2 ESD Ratings: SN74LS00

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance. Tested on SN74LS00N package.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	SN54xx00	4.5	5	5.5	V
		SN74xx00	4.75	5	5.25	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage	SNx400, SN7LS400, and SNx4S00			0.8	V
		SN54LS00			0.7	
I_{OH}	High-level output current	SN5400, SN54LS00, and SN74LS00			–0.4	mA
		SNx4S00			–1	
I_{OL}	Low-level output current	SNx400			16	mA
		SN5LS400			4	
		SN7LS400			8	
		SNx4S00			20	
T_A	Operating free-air temperature	SN54xx00	–55		125	°C
		SN74xx00	0		70	

6.4 Thermal Information

THERMAL METRIC[1][2]		SN74LS00				UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.9	102.8	54.8	89.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	53.3	42.1	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48	53.4	34.8	50.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.6	16.5	26.9	16.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.8	52.9	34.7	49.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics: SNx400

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = MIN and I_I = –12 mA				–1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, and I_{OH} = –0.4 mA		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, and I_{OL} = 16 mA			0.2	0.4	V
I_I	V_{CC} = MAX and V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = MAX and V_I = 2.4 V				40	µA
I_{IL}	V_{CC} = MAX and V_I = 0.4 V				–1.6	mA
I_{OS}	V_{CC} = MAX	SN5400	–20		–55	mA
		SN7400	–18		–55	
I_{CCH}	V_{CC} = MAX and V_I = 0 V			4	8	mA
I_{CCL}	V_{CC} = MAX and V_I = 4.5 V			12	22	mA

6.6 Electrical Characteristics: SNx4LS00

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = MIN and I_I = –18 mA				–1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = MAX, and I_{OH} = –0.4 mA		2.5	3.4		V
V_{OL}	V_{CC} = MIN and V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4	V
		I_{OL} = 8 mA (SN74LS00)		0.35	0.5	
I_I	V_{CC} = MAX and V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = MAX and V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = MAX and V_I = 0.4 V				–0.4	mA
I_{OS}	V_{CC} = MAX		–20		–100	mA
I_{CCH}	V_{CC} = MAX and V_I = 0 V			0.8	1.6	mA
I_{CCL}	V_{CC} = MAX and V_I = 4.5 V			2.4	4.4	mA

6.7 Electrical Characteristics: SNx4S00

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = MIN and I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, and I_{OH} = –1 mA	2.5	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, and I_{OL} = 20 mA			0.5	V
I_I	V_{CC} = MAX and V_I = 5.5 V			1	mA
I_{IH}	V_{CC} = MAX and V_I = 2.7 V			50	µA
I_{IL}	V_{CC} = MAX and V_I = 0.5 V			–2	mA

Electrical Characteristics: SNx4S00 (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OS}	V_{CC} = MAX	–40		–100	mA
I_{CCH}	V_{CC} = MAX and V_I = 0 V		10	16	mA
I_{CCL}	V_{CC} = MAX and V_I = 4.5 V		20	36	mA

6.8 Switching Characteristics: SNx400

V_{CC} = 5 V, T_A = 25°C, and over operating free-air temperature range (unless otherwise noted). See Figure 2.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω and C_L = 15 pF		11	22	ns
t_{PHL}					7	15	

6.9 Switching Characteristics: SNx4LS00

V_{CC} = 5 V, T_A = 25°C, and over operating free-air temperature range (unless otherwise noted). See Figure 2.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ and C_L = 15 pF		9	15	ns
t_{PHL}					10	15	

6.10 Switching Characteristics: SNx4S00

V_{CC} = 5 V, T_A = 25°C, and over operating free-air temperature range (unless otherwise noted). See Figure 2.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω and C_L = 15 pF		3	4.5	ns
			R_L = 280 Ω and C_L = 50 pF		4.5		
t_{PHL}	A or B	Y	R_L = 280 Ω and C_L = 15 pF		3	5	
			R_L = 280 Ω and C_L = 50 pF		5		

6.11 Typical Characteristics

C_L = 15 pF

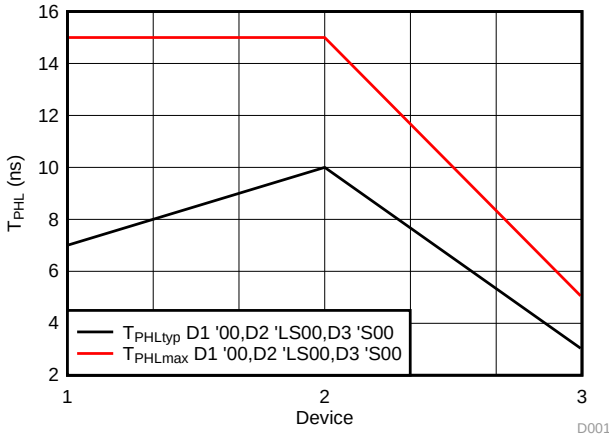
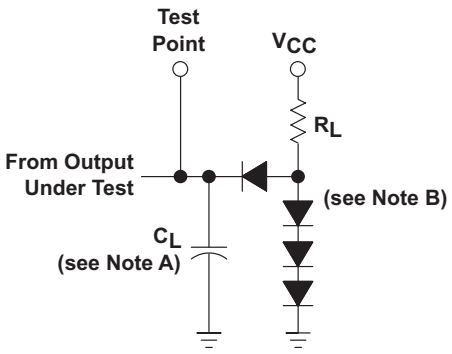
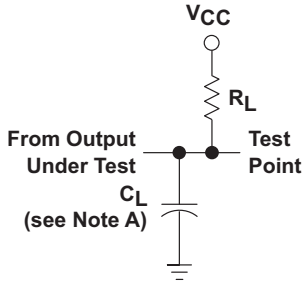


Figure 1. T_{PHL} (Across Devices)

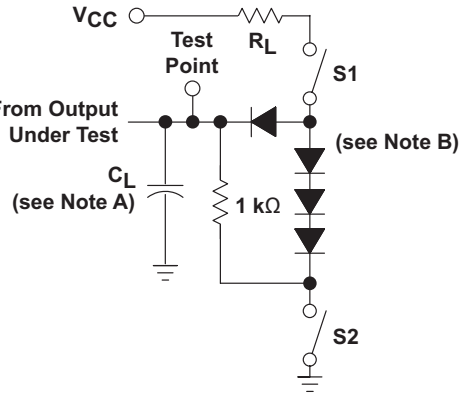
7 Parameter Measurement Information



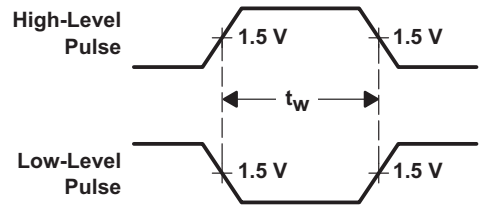
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



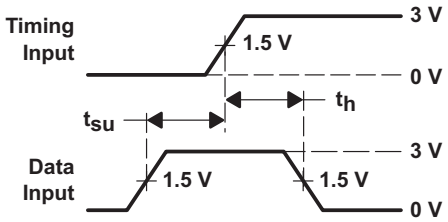
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



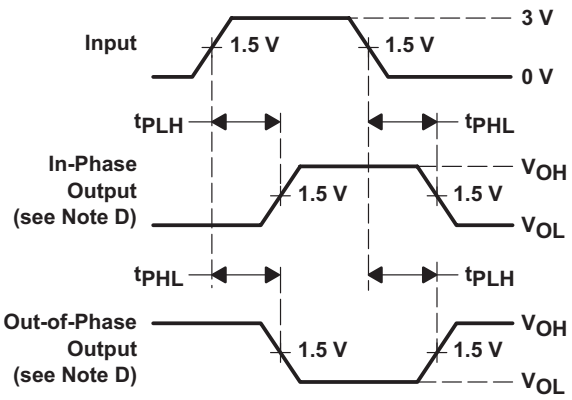
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



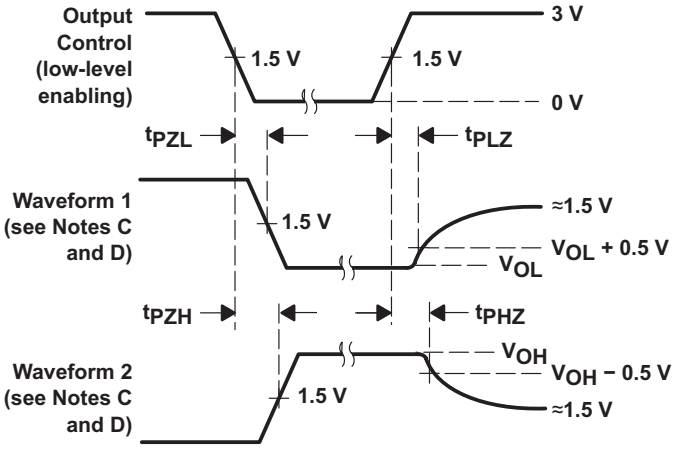
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\,\Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4xx00 devices are quadruple, 2-input NAND gates which perform the Boolean function $Y = \overline{A} \times \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

8.2 Functional Block Diagram

8.3 Feature Description

The operating voltage of SN74xx00 is from 4.75-V to 5.25-V V_{CC}. The operating voltage of SN54xx00 is from 4.5-V to 5.5-V V_{CC}. The SN54xx00 devices are rated from –55°C to 125°C whereas SN74xx00 device are rated from 0°C to 70°C.

8.4 Device Functional Modes

Table 1 lists the functions of the devices.

Table 1. Functional Table (Each Gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4xx00 devices are quadruple, 2-input NAND gate, and can be configured as dual 3-input NAND gate as shown in Figure 3.

9.2 Typical Application

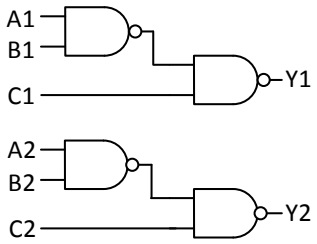


Figure 3. Typical Application Diagram

9.2.1 Design Requirements

These devices use BJT technology and have unbalanced output drive with I_{OL} and I_{OH} specified as per the *Recommended Operating Conditions*. It can be configured as a dual 3-input NAND gate as shown in Figure 3.

9.2.2 Detailed Design Procedure

- Recommended Input Conditions:
  - The inputs are TTL compliant.
  - Because the base-emitter junction at the inputs breaks down, no voltage greater than 5.5 V must be applied to the inputs.
  - Specified high and low levels: See V_{IH} and V_{IL} in *Recommended Operating Conditions*.
- Recommended Output Conditions:
  - No more than one output must be shorted at a time as per the *Electrical Characteristics: SNx400* for thermal stability and reliability.
  - For high-current applications, consider thermal characteristics of the package listed in *Thermal Information*.

Typical Application (continued)

9.2.3 Application Curves

C_L = 15 pF

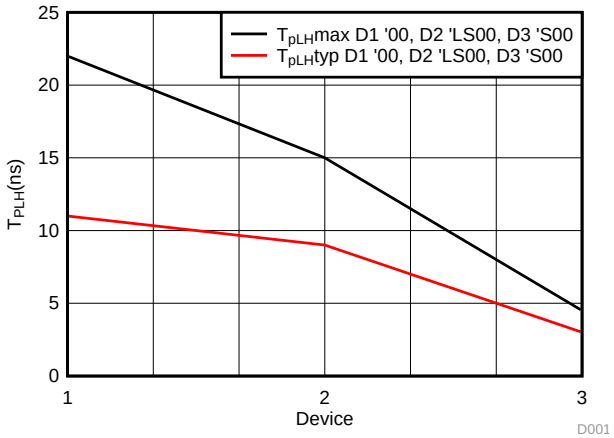


Figure 4. T_{PLH} (Across Devices)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions* for each of the SNx4LS00, SNx4S00, and SNx400 devices.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple V_{CC} pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic, devices inputs must never float.

Devices with multiple-emitter inputs (SN74 and SN74S series) need special care. Because no voltage greater than 5.5 V must be applied to the inputs (if exceeded, the base-emitter junction at the inputs breaks down), the inputs of these devices must be connected to the supply voltage, V_{CC}, through series resistor, R_S (see Figure 5). This resistor must be dimensioned such that the current flowing into the gate or gates, which results from overvoltage, does not exceed 1 mA. However, because the high-level input current of the circuits connected to the gate flows through this resistor, the resistor must be dimensioned so that the voltage drop across it still allows the required high level. Equation 1 and Equation 2 are for dimensioning resistor, R_S, and several inputs can be connected to a high level through a single resistor if the following conditions are met.

$$R_{S(min)} = \frac{V_{CCP} - 5.5\ V}{1\ mA} \quad (1)$$

$$R_{S(max)} = \frac{V_{CC(min)} - 2.4\ V}{n \times I_{IH}} \quad (2)$$

where

- n = number of inputs connected
- I_{IH} = high input current (typical 40 µA)
- $V_{CC(min)}$ = minimum supply voltage, V_{CC}
- V_{CCP} = maximum peak voltage of the supply voltage, V_{CC} (about 7 V)

11.2 Layout Example

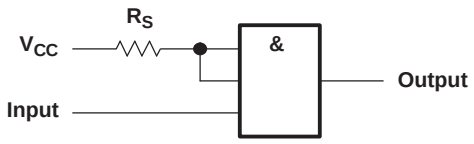


Figure 5. Series Resistor Connected to Unused Inputs of Multiple-Emitter Transistors