

SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

SDLS118 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

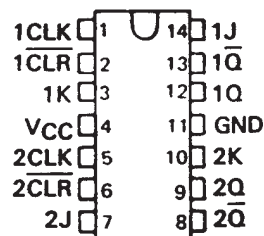
description

The '73, and 'H73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, and 'H73, are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contains two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the \bar{Q} output high.

The SN5473, SN54H73, and the SN54LS73A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7473, and the SN74LS73A are characterized for operation from 0°C to 70°C .

SN5473, SN54LS73A . . . J OR W PACKAGE
SN7473 . . . N PACKAGE
SN74LS73A . . . D OR N PACKAGE
(TOP VIEW)



'73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H		L	L	Q_0	\bar{Q}_0
H		H	L	H	L
H		L	H	L	H
H		H	H	TOGGLE	

'LS73A
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H		L	L	Q_0	\bar{Q}_0
H		H	L	H	L
H		L	H	L	H
H		H	H	TOGGLE	
H	H	X	X	Q_0	\bar{Q}_0

FOR CHIP CARRIER INFORMATION,
CONTACT THE FACTORY

SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

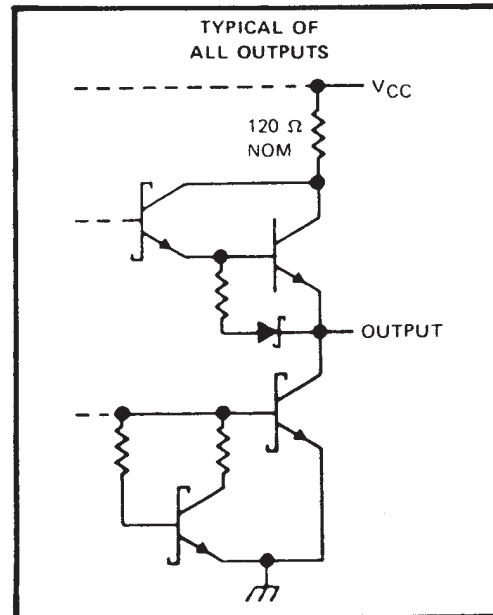
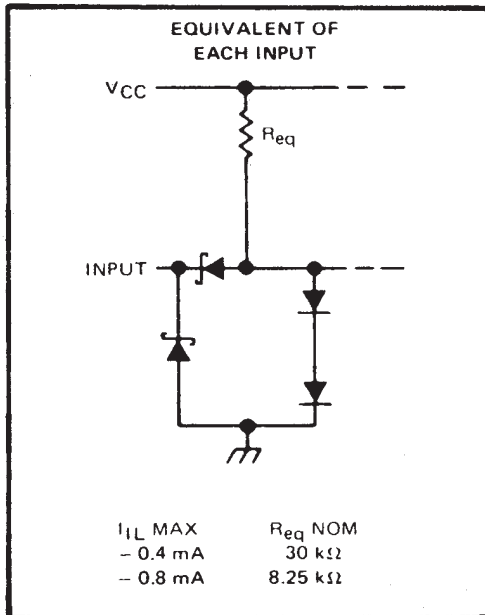
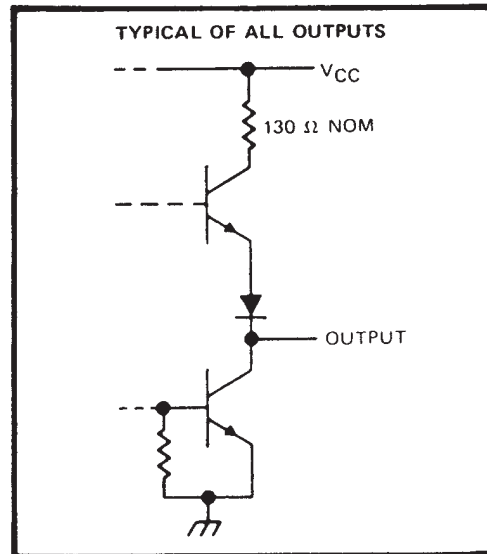
SDLS118 – DECEMBER 1983 – REVISED MARCH 1988

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

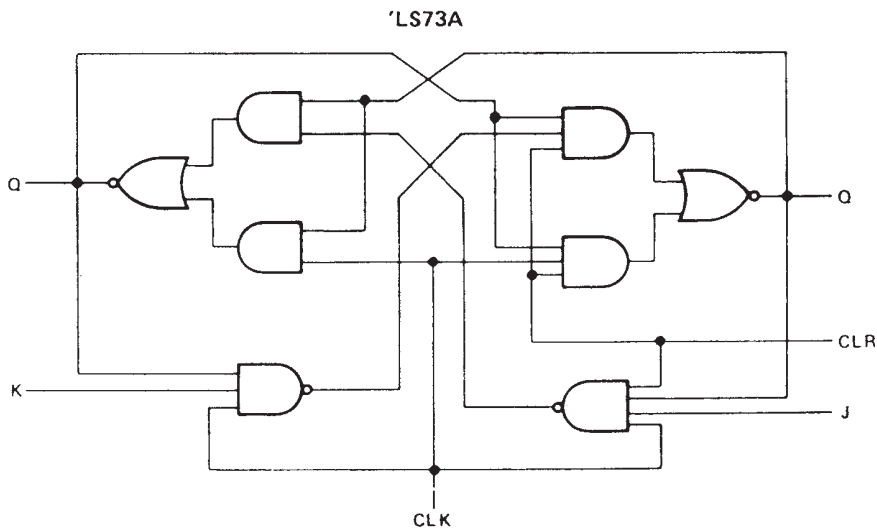
schematics of inputs and outputs



SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

SDLS118 – DECEMBER 1983 – REVISED MARCH 1988

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage: '73	5.5 V
'LS73A	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

SDLS118 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

		SN5473			SN7473			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			16			16	mA
t_w	Pulse duration	CLK high		20			20	ns
		CLK low		47			47	
		\overline{CLR} low		25			25	
t_{su}	Input setup time before CLK \uparrow			0			0	ns
t_h	Input hold time data after CLK \downarrow			0			0	ns
T_A	Operating free-air temperature	-55		125	0		70	$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN5473			SN7473			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	J or K			40			40	μA
	\overline{CLR} or CLK			80			80	
I_{IL}	J or K			-1.6			-1.6	mA
	\overline{CLR}			-3.2			-3.2	
	CLK			-3.2			-3.2	
I_{OS} [§]	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
I_{CC} [¶]	$V_{CC} = \text{MAX}$, See Note 2		10	20		10	20	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$.

[§] Not more than one output should be shorted at a time.

[¶] Average per flip-flop.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$ (see note 3)

PARAMETER [#]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				15	20		MHz
t_{PLH}	\overline{CLR}	\overline{Q}	$R_L = 400 \Omega$, $C_L = 15 \text{ pF}$		16	25	ns
t_{PHL}		Q			25	40	ns
t_{PLH}	CLK	Q or \overline{Q}			16	25	ns
t_{PHL}					25	40	ns

[#] f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

SDLS118 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

	SN54LS73A			SN74LS73A			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
V_{IH} High-level input voltage	2			2			V	
V_{IL} Low-level input voltage			0.7			0.8	V	
I_{OH} High-level output current			-0.4			-0.4	mA	
I_{OL} Low-level output current			4			8	mA	
f_{clock} Clock frequency	0		30	0		30	MHz	
t_w Pulse duration	CLK high		20	20		ns		
	\overline{CLR} low		25	20				
t_{su} Set up time-before CLK↓	data high or low		20	20		ns		
	\overline{CLR} inactive		20	20				
t_h Hold time-data after CLK↓			0	0		ns		
T_A Operating free-air temperature			-55	125		0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS73A			SN74LS73A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX}$, $I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
	$V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I	J or K			0.1			0.1	mA
	\overline{CLR}	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$		0.3			0.3	
	CLK			0.4			0.4	
I_{IH}	J or K	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$		20			20	μA
	\overline{CLR}			60			60	
	CLK			80			80	
I_{IL}	J or K	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-0.4			-0.4	mA
	\overline{CLR} or CLK			-0.8			-0.8	
$I_{OS}§$	$V_{CC} = \text{MAX}$, See Note 4	-20		-100	-20		-100	mA
I_{CC} (Total)	$V_{CC} = \text{MAX}$, See Note 2		4	6		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O = 2.25 \text{ V}$ and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				30	45		MHz
t_{PLH}	\overline{CLR} or CLK	Q or \overline{Q}	$R_L = 2 \text{ k}\Omega$, $C_L = 15 \text{ pF}$		15	20	ns
t_{PHL}					15	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9675101QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9675101QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9675101QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9675101VCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9675101VCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9675101VDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9675101VDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SN54LS73AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN54LS73AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SN7473N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7473N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7473N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7473N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS73AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS73AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS73AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS73ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS73ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SNJ54LS73AFD	OBSOLETE	LCCC	FK	20		TBD	Call TI	Level-NC-NC-NC
SNJ54LS73AFD	OBSOLETE	LCCC	FK	20		TBD	Call TI	Level-NC-NC-NC
SNJ54LS73AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS73AJ	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS73AW	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS73AW	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



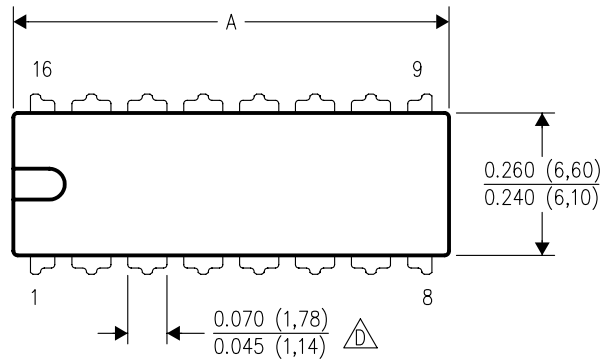
4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

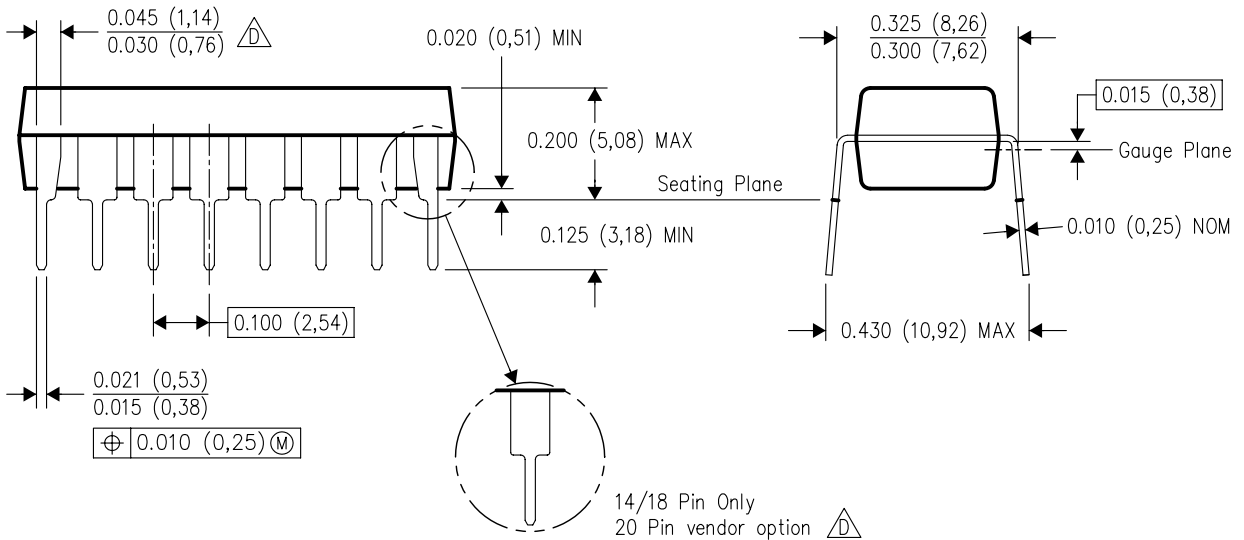
N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



DIM	PINS **			
	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

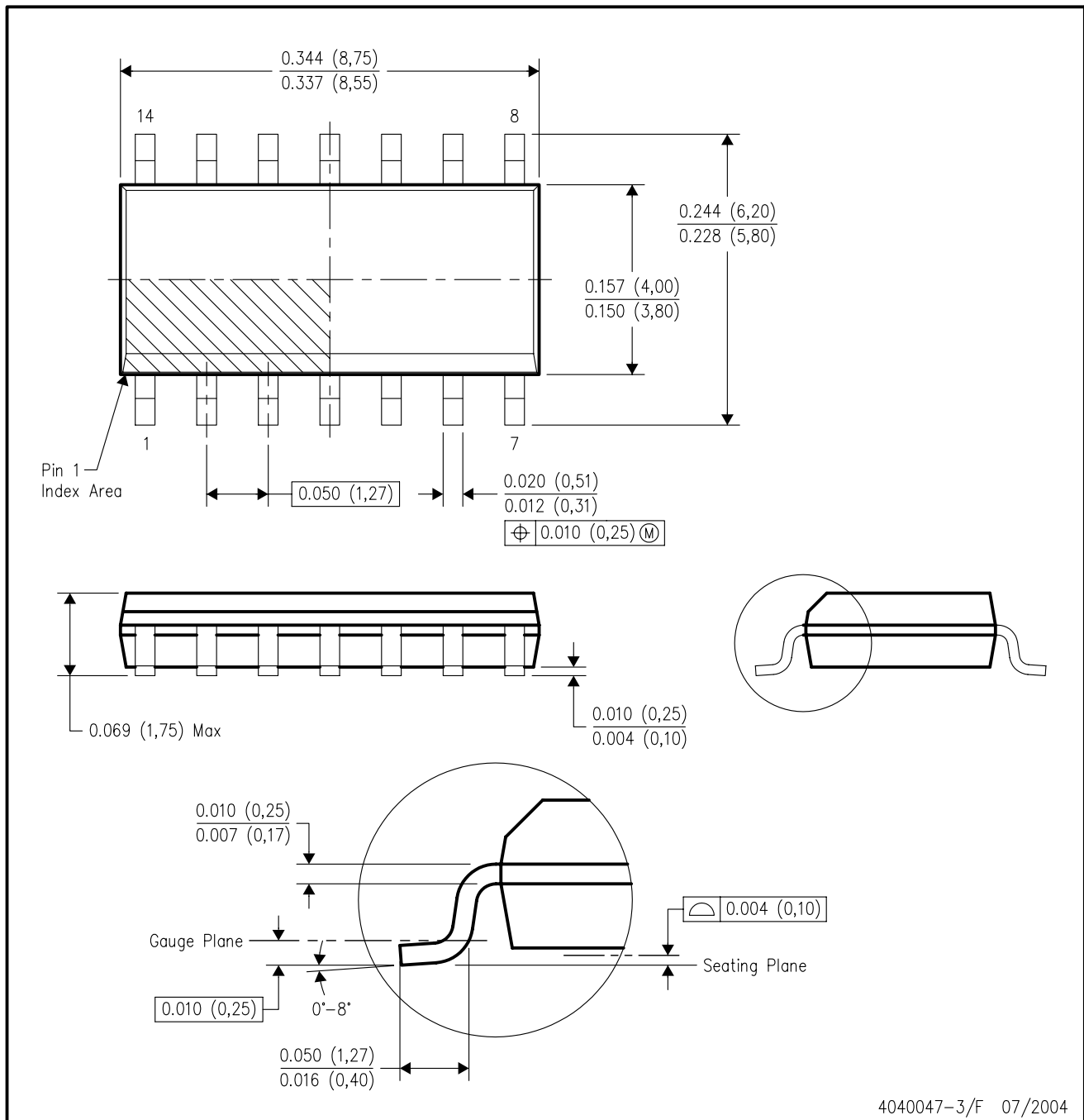


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.