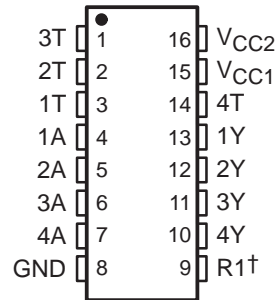


- Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-232-E and ITU Recommendation V.28
- Input Resistance . . . 3 k $\Omega$  to 7 k $\Omega$  Over Full EIA/TIA-232-E Voltage Range
- Input Threshold Adjustable to Meet Fail-Safe Requirements Without Using External Components
- Built-In Hysteresis for Increased Noise Immunity
- Inverting Output Compatible With TTL
- Output With Active Pullup for Symmetrical Switching Speeds
- Standard Supply Voltages . . . 5 V or 12 V

D OR N PACKAGE  
(TOP VIEW)



† For function of R1, see schematic

### description

The SN75154 is a monolithic low-power Schottky line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by ANSI Standard EIA/TIA-232-E. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single 5-V supply; however, a built-in option allows operation from a 12-V supply without the use of additional components. The output is compatible with most TTL circuits when either supply voltage is used.

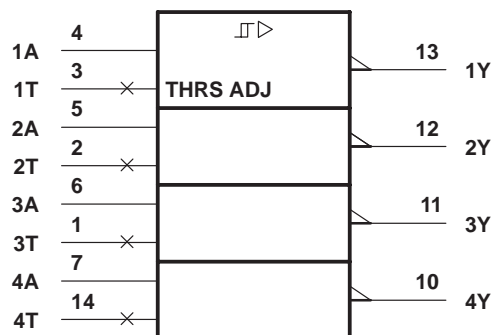
In normal operation, the threshold-control terminals are connected to the  $V_{CC1}$  terminal, even if power is being supplied via the alternate  $V_{CC2}$  terminal. This provides a wide hysteresis loop, which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

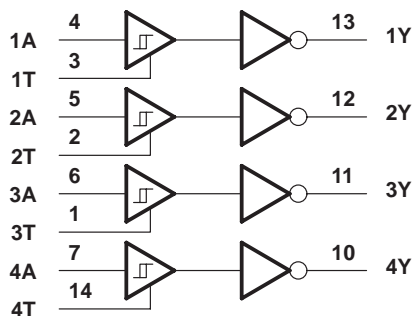
The SN75154 is characterized for operation from 0°C to 70°C.

# SN75154 QUADRUPLE LINE RECEIVER

## logic symbol†

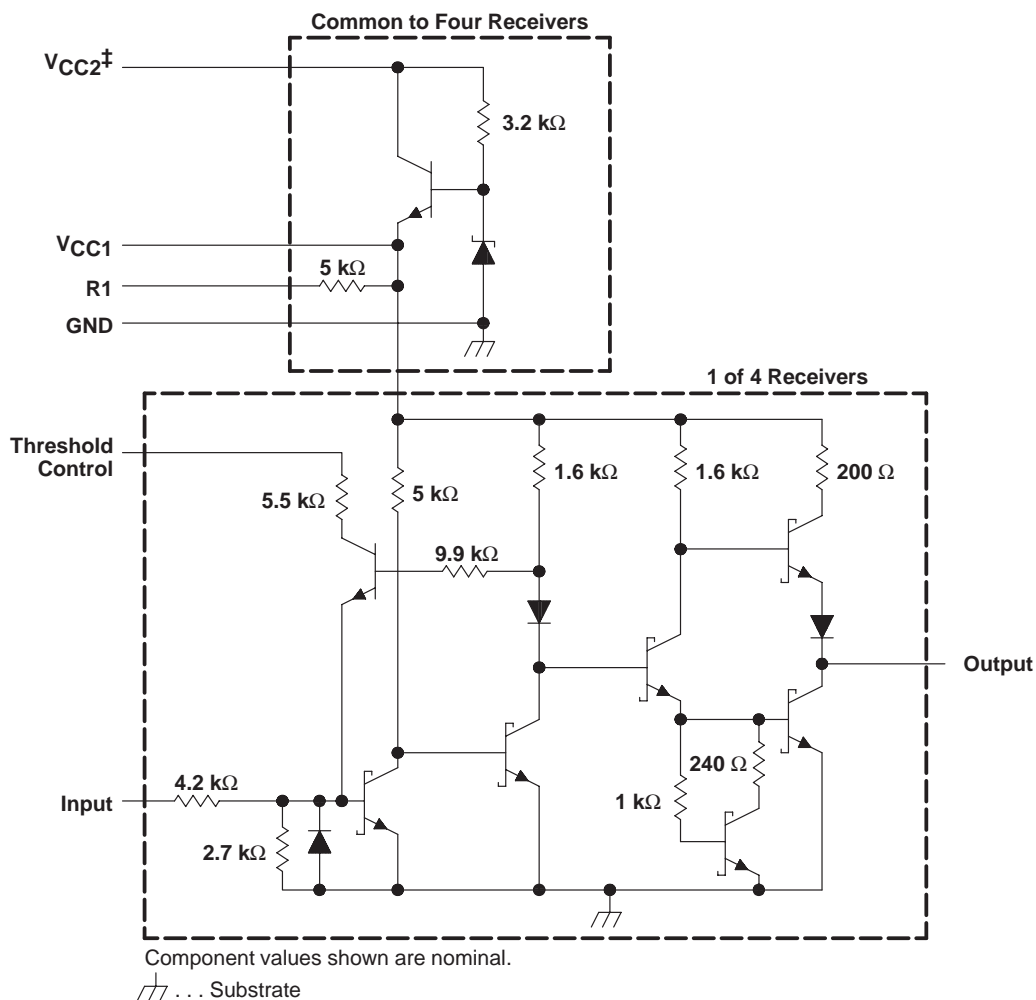


## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## schematic



‡ When  $V_{CC1}$  is used,  $V_{CC2}$  may be left open or shorted to  $V_{CC1}$ . When  $V_{CC2}$  is used,  $V_{CC1}$  must be left open or connected to the threshold control pins.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Normal supply voltage, $V_{CC1}$ (see Note 1)	7 V
Alternate supply voltage, $V_{CC2}$	14 V
Input voltage, $V_I$	$\pm 25$ V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network GND terminal.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
Normal supply voltage, $V_{CC1}$	4.5	5	5.5	V
Alternate supply voltage, $V_{CC2}$	10.8	12	13.2	V
High-level input voltage, $V_{IH}$ (see Note 2)	3		15	V
Low-level input voltage, $V_{IL}$ (see Note 2)	–15		–3	V
High-level output current, $I_{OH}$			–400	$\mu\text{A}$
Low-level output current, $I_{OL}$			16	mA
Operating free-air temperature, $T_A$	0		70	°C

NOTE 2: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic and threshold levels only, e.g., when 0 V is the maximum, the minimum limit is a more negative voltage.

# SN75154 QUADRUPLE LINE RECEIVER

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage	1	Normal operation	0.8	2.2	3	V
			Fail-safe operation	0.8	2.2	3	
V <sub>IT-</sub>	Negative-going input threshold voltage	1	Normal operation	-3	-1.1	0	V
			Fail-safe operation	0.8	1.4	3	
V <sub>hys</sub>	Hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )	1	Normal operation	0.8	3.3	6	V
			Fail-safe operation	0	0.8	2.2	
V <sub>OH</sub>	High-level output voltage	1	I <sub>OH</sub> = -400 μA	2.4	3.5		V
V <sub>OL</sub>	Low-level output voltage	1	I <sub>OL</sub> = 16 mA		0.29	0.4	V
r <sub>i</sub>	Input resistance	2	ΔV <sub>I</sub> = -25 V to -14 V	3	5	7	kΩ
			ΔV <sub>I</sub> = -14 V to -3 V	3	5	7	
			ΔV <sub>I</sub> = -3 V to 3 V	3	6	8	
			ΔV <sub>I</sub> = 3 V to 14 V	3	5	7	
			ΔV <sub>I</sub> = 14 V to 25 V	3	5	7	
V <sub>I(open)</sub>	Open-circuit input voltage	3	I <sub>I</sub> = 0	0	0.2	2	V
I <sub>OS</sub>	Short-circuit output current‡	4	V <sub>CC1</sub> = 5.5 V, V <sub>I</sub> = -5 V	-10	-20	-40	mA
I <sub>CC1</sub>	Supply current from V <sub>CC1</sub>	5	V <sub>CC1</sub> = 5.5 V, T <sub>A</sub> = 25°C		20	35	mA
I <sub>CC2</sub>	Supply current from V <sub>CC2</sub>		V <sub>CC2</sub> = 13.2 V, T <sub>A</sub> = 25°C		23	40	

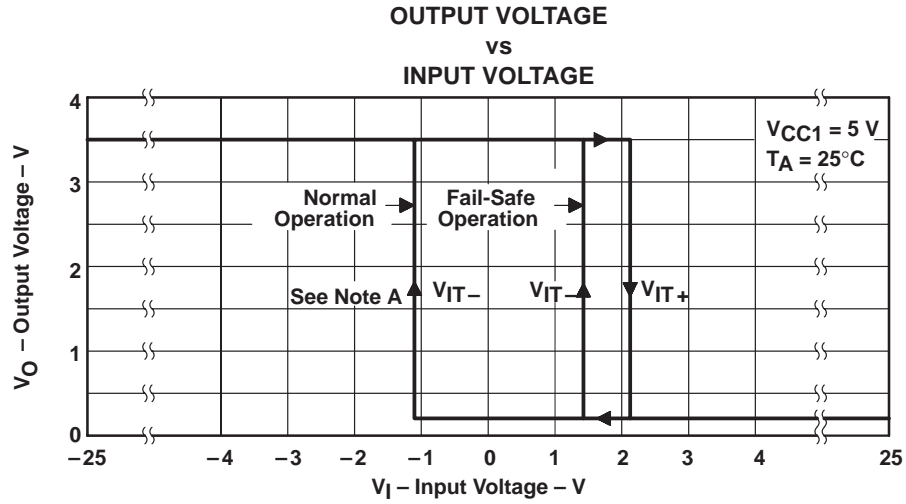
† All typical values are at V<sub>CC1</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time.

switching characteristics, V<sub>CC1</sub> = 5 V, T<sub>A</sub> = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	6	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 390 Ω		11		ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output				8		ns
t <sub>TLH</sub>	Transition time, low- to high-level output				7		ns
t <sub>THL</sub>	Transition time, high- to low-level output				2.2		ns

TYPICAL CHARACTERISTICS



NOTE A: For normal operation, the threshold controls are connected to  $V_{CC1}$ . For fail-safe operation, the threshold controls are open.

Figure 1

PARAMETER MEASUREMENT INFORMATION

dc test circuits†

TEST TABLE

TEST	MEASURE	A	T	Y	V <sub>CC1</sub>	V <sub>CC2</sub>
Open-circuit input (fail safe)	V <sub>OH</sub>	Open	Open	I <sub>OH</sub>	4.5 V	Open
	V <sub>OH</sub>	Open	Open	I <sub>OH</sub>	Open	10.8 V
V <sub>IT+</sub> min, V <sub>IT-</sub> min (fail safe)	V <sub>OH</sub>	0.8 V	Open	I <sub>OH</sub>	5.5 V	Open
	V <sub>OH</sub>	0.8 V	Open	I <sub>OH</sub>	Open	13.2 V
V <sub>IT+</sub> min (normal)	V <sub>OH</sub>	Note A	V <sub>CC1</sub>	I <sub>OH</sub>	5.5 V and T	Open
	V <sub>OH</sub>	Note A	V <sub>CC1</sub>	I <sub>OH</sub>	T	13.2 V
V <sub>IL</sub> max, V <sub>IT+</sub> min (normal)	V <sub>OH</sub>	-3 V	V <sub>CC1</sub>	I <sub>OH</sub>	5.5 V and T	Open
	V <sub>OH</sub>	-3 V	V <sub>CC1</sub>	I <sub>OH</sub>	T	13.2 V
V <sub>IH</sub> min, V <sub>IT+</sub> max, V <sub>IT-</sub> max (fail safe)	V <sub>OL</sub>	3 V	Open	I <sub>OL</sub>	4.5 V	Open
	V <sub>OL</sub>	3 V	Open	I <sub>OL</sub>	Open	10.8 V
V <sub>IH</sub> min, V <sub>IT+</sub> max (normal)	V <sub>OL</sub>	3 V	V <sub>CC1</sub>	I <sub>OL</sub>	4.5 V and T	Open
	V <sub>OL</sub>	3 V	V <sub>CC1</sub>	I <sub>OL</sub>	T	10.8 V
V <sub>IT-</sub> max (normal)	V <sub>OL</sub>	Note B	V <sub>CC1</sub>	I <sub>OL</sub>	5.5 V and T	Open
	V <sub>OL</sub>	Note B	V <sub>CC1</sub>	I <sub>OL</sub>	T	13.2 V

NOTES: A. Momentarily apply -5 V, then 0.8 V.  
 B. Momentarily apply 5 V, then GND.

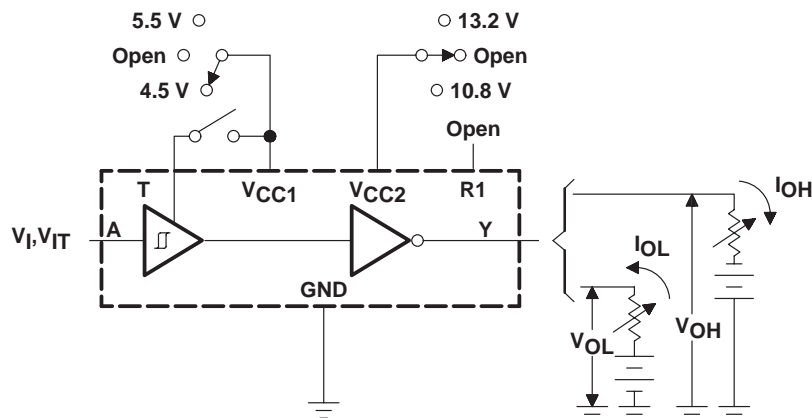
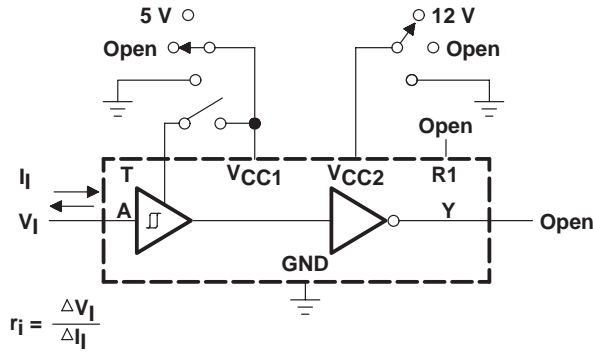


Figure 2. V<sub>IH</sub>, V<sub>IL</sub>, V<sub>IT+</sub>, V<sub>IT-</sub>, V<sub>OH</sub>, V<sub>OL</sub>

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

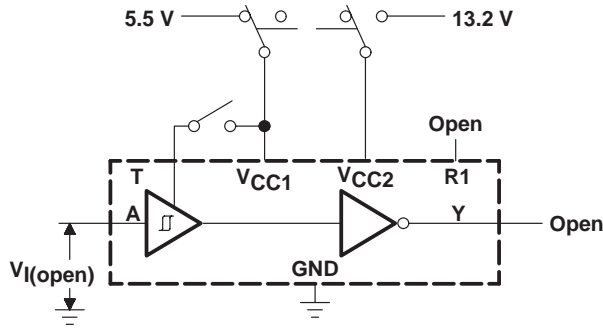
PARAMETER MEASUREMENT INFORMATION

dc test circuits† (continued)



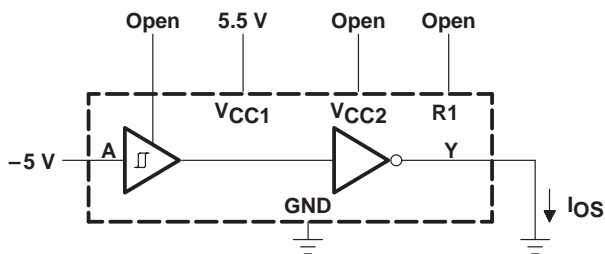
TEST TABLE		
T	V <sub>CC1</sub>	V <sub>CC2</sub>
Open	5 V	Open
Open	GND	Open
Open	Open	Open
V <sub>CC1</sub>	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
V <sub>CC1</sub>	T	12 V
V <sub>CC1</sub>	T	GND
V <sub>CC1</sub>	T	Open

Figure 3. Input Resistance



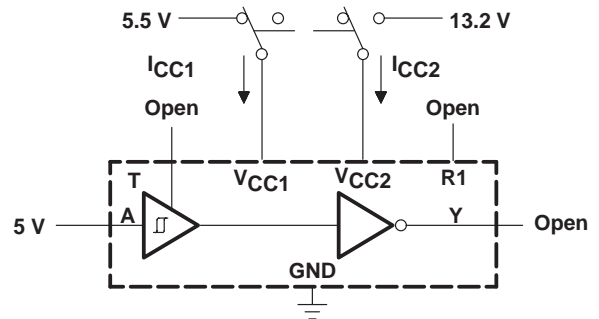
TEST TABLE		
T	V <sub>CC1</sub>	V <sub>CC2</sub>
Open	5.5 V	Open
V <sub>CC1</sub>	5.5 V	Open
Open	Open	13.2 V
V <sub>CC1</sub>	T	13.2 V

Figure 4. Input Voltage (Open)



Each output is tested separately.

Figure 5. Output Short-Circuit Current

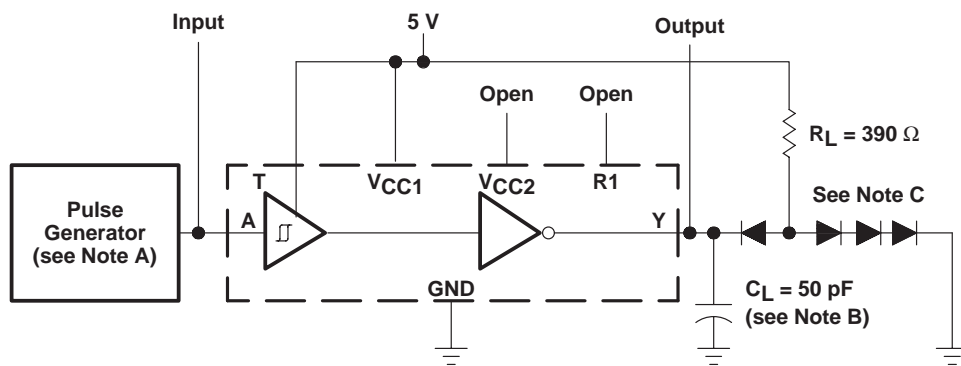


All four line receivers are tested simultaneously.

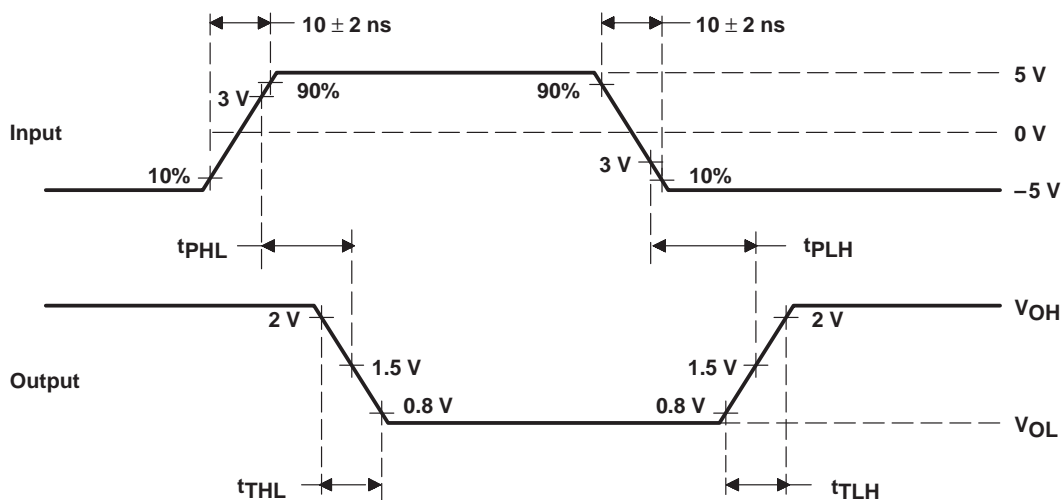
Figure 6. Supply Current

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

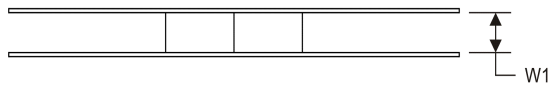
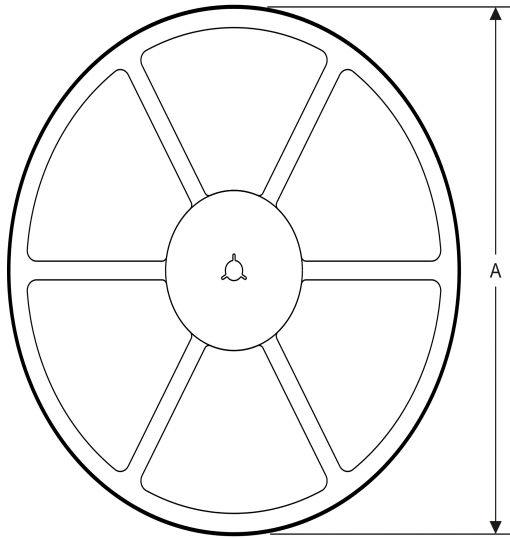
- NOTES: A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ ,  $t_w \leq 200 \text{ ns}$ , duty cycle  $\leq 20\%$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N3064.

Figure 6. Test Circuit and Voltage Waveforms



## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

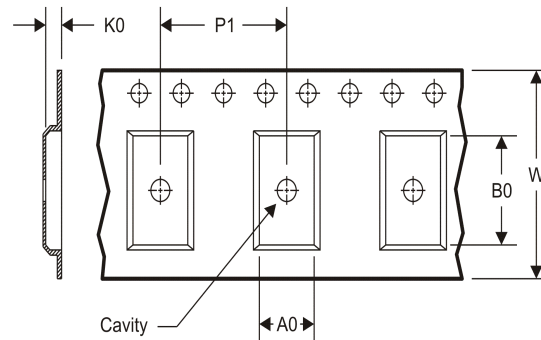


### TAPE AND REEL INFORMATION

\*All dimensions are nominal

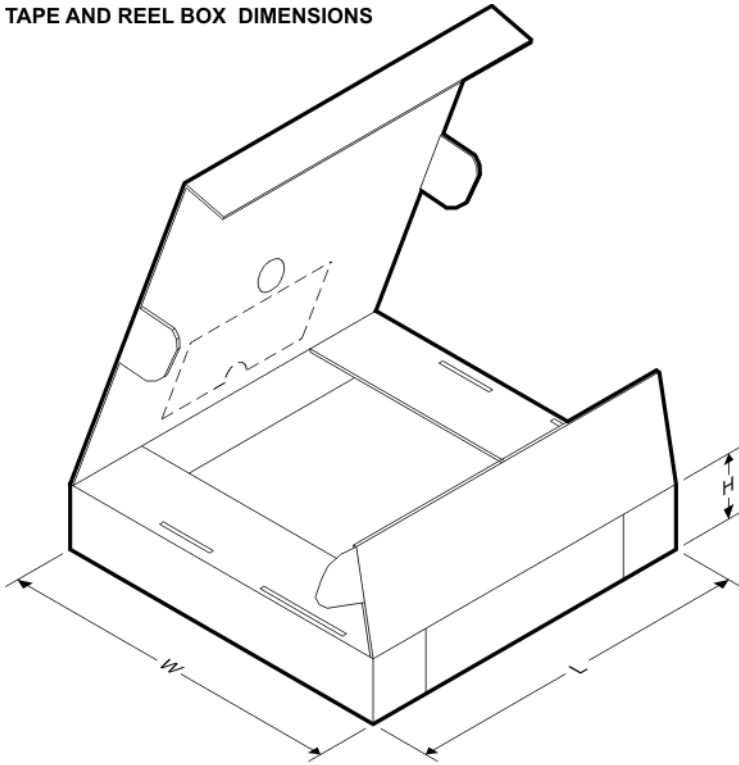
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75154DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75154NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

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**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75154DR	SOIC	D	16	2500	333.2	345.9	28.6
SN75154NSR	SO	NS	16	2000	367.0	367.0	38.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

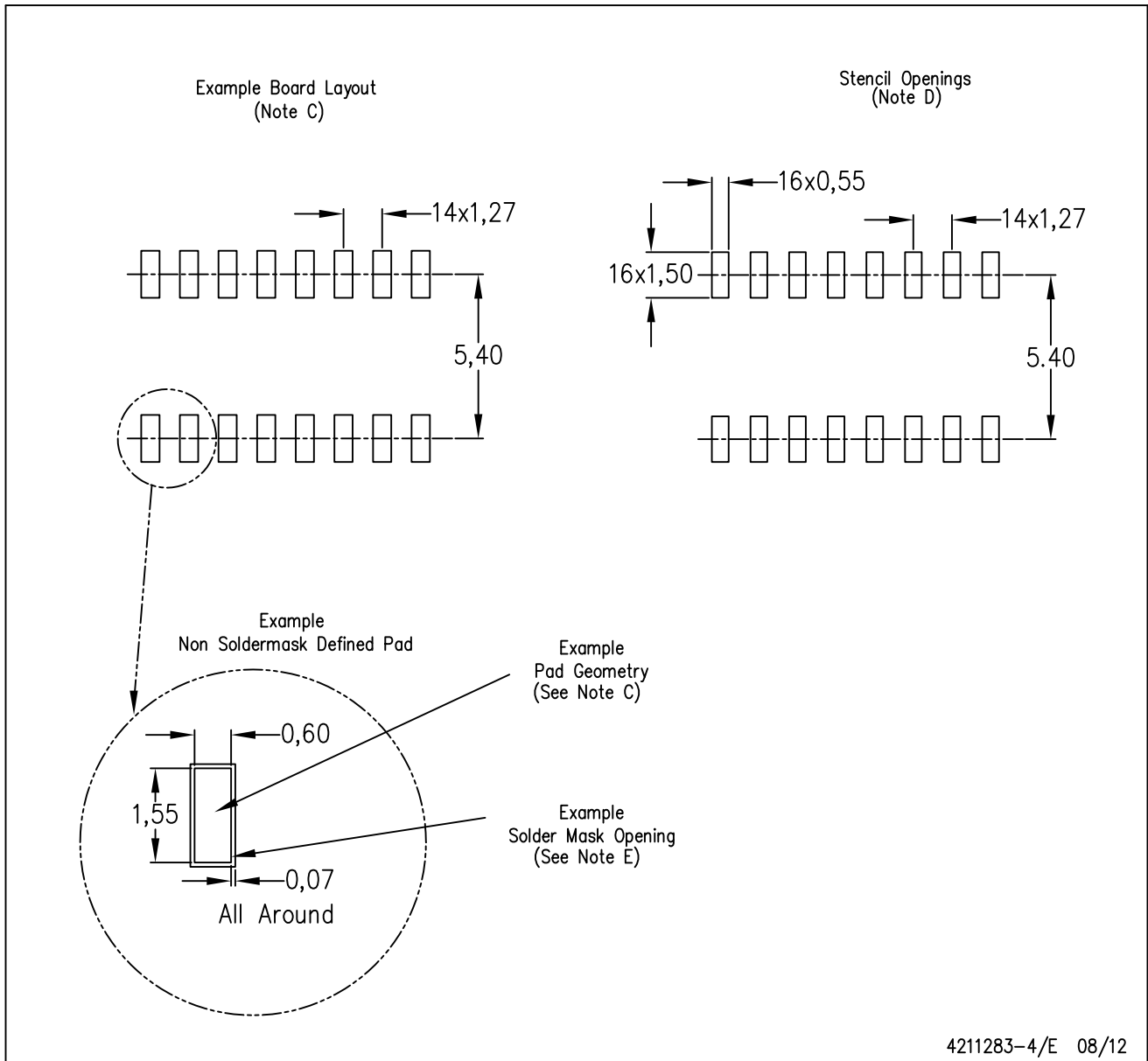
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.