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STB20NM50 - STB20NM50-1
STP20NM50 - STP20NM50FP

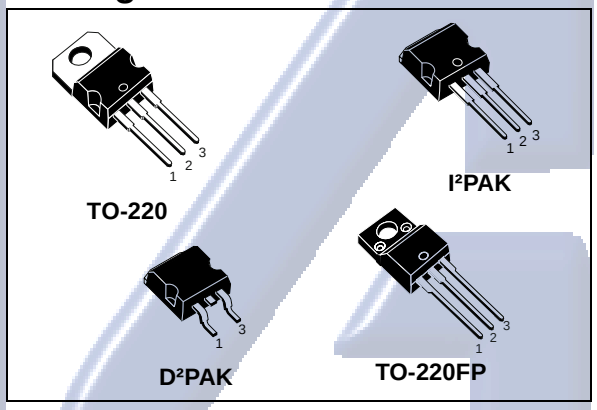
N-CHANNEL 550V@Tj_{max} - 0.20Ω - 20A - TO220/FP-D²PAK-I²PAK
Zener-Protected SuperMESH™ MOSFET

General features

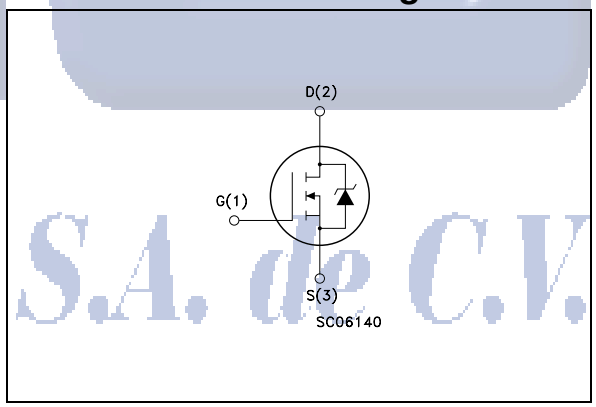
Type	$V_{DSS(@Tj\ max)}$	$R_{DS(on)}$	I_D
STB20NM50	550 V	<0.25 Ω	20 A
STB20NM50-1	550 V	<0.25 Ω	20 A
STP20NM50	550 V	<0.25 Ω	20 A
STP20NM50FP	550 V	<0.25 Ω	20 A

- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE

Package



Internal schematic diagram



Description

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and exellent avalanche characteristics and dynamic performances.

Applications

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization andhiher efficiencies

Order codes

Sales Type	Marking	Package	Packaging
STB20NM50T4	B20NM50	D²PAK	TAPE & REEL
STB20NM50-1	B20NM50-1	I²PAK	TUBE
STP20NM505	P20NM50	TO-220	TUBE
STP20NM50FP	P20NM50FP	TO-220FP	TUBE

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/D²PAK/I²PAK	TO-220FP	
V_{GS}	Gate-Source Voltage	± 30		V
I_D	Drain Current (continuous) at T_C = 25°C	20	20 (*Note* 3)	A
I_D	Drain Current (continuous) at T_C = 100°C	12.6	12.6 (*Note* 3)	A
I_{DM} *Note* 2	Drain Current (pulsed)	80	80 (*Note* 3)	A
P_{TOT}	Total Dissipation at T_C = 25°C	192	45	W
	Derating Factor	1.2	0.36	W/°C
dv/dt *Note* 1	Peak Diode Recovery voltage slope	15		V/ns
V_{ISO}	Insulation Withstand Volatge (DC)	--	2000	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-65 to 150		°C

Table 2. Thermal data

		TO-220/D²PAK/I²PAK	TO-220FP	Unit
Rthj-case	Thermal Resistance Junction-case Max	0.65	2.8	°C/W
Rthj-amb	Thermal Resistance Junction-amb Max	62.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, repetitive or Not-Repetitive (pulse width limited by Tj max)	10	A
E_{AS}	Single Pulse Avalanche Energy (starting Tj=25°C, I_D=5A, V_{DD}= 50V)	650	mJ

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2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 250µA, V_{GS}= 0	500			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating, V_{DS} = Max Rating,Tc = 125°C			1 10	µA µA
I_{GSS}	Gate Body Leakage Current (V_{DS} = 0)	V_{GS} = ±30V			±100	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static Drain-Source On Resistance	V_{GS}= 10 V, I_D= 10 A		0.20	0.25	Ω

Table 5. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} *Note* 4	Forward Transconductance	V_{DS} > $I_{D(ON)}$ x$R_{DS(ON)max}$, I_D = 10A		10		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		1480 285 34		pF pF pF
$C_{oss\ eq.}$ *Note* 5	Equivalent Ouput Capacitance	V_{GS}=0, V_{DS} =0V to 400V		130		pF
Rg	Gate Input Resistance	f=1MHz Gate DC Bias=0 Test Signal Level=20mV Open Drain		1.6		Ω
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=400V, I_D = 20A V_{GS} =10V (see Figure 15)		40 13 19	56	nC nC nC

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Table 6. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD}=250 V, I_D=10A, R_G=4.7Ω, V_{GS}=10V (see Figure 16)		24 16		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD}=400 V, I_D=20A, R_G=4.7Ω, V_{GS}=10V (see Figure 16)		9 8.5 23		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} *Note* 2	Source-drain Current Source-drain Current (pulsed)				20 80	A A
V_{SD} *Note* 4	Forward on Voltage	I_{SD}=20A, V_{GS}=0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD}=20A, di/dt = 100A/µs, V_{DD}=100 V, Tj=25°C		350 4.6 26		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD}=20A, di/dt = 100A/µs, V_{DD}=100 V, Tj=150°C		435 5.9 27		ns µC A

(1) I_{SD} ≤20A, di/dt ≤400A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

(2) Pulse width limited by safe operating area

(3) Limited only by maximum temperature allowed

(4) Pulsed: pulse duration = 300µs, duty cycle 1.5%

(5) $C_{oss\,eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

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