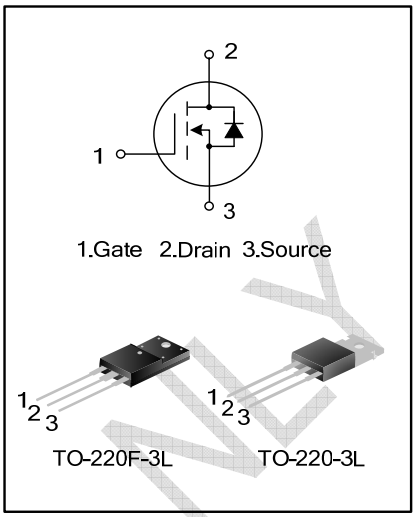
12A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF12N60T/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure DMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 12A,600V,$R_{DS(on)(typ)}$=0.58Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE

S V D X N E X X X

- Silan VDMOS Code of F-cell process
- Nominal current,using 1 or2 digits: Example:4 denotes 4A, 10 denotes 10A, 08 denotes 0.8A
- N denotes N Channel
- Special Features indication, May be omitted. Example: E denotes embeded ESD structure
- Nominal Voltage,using 2 digits Example: 60 denotes 600V, 65 denotes 650V.
- Package information. Example:F:TO-220F. T:TO-220.

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF12N60T	TO-220-3L	SVF12N60T	Pb free	Tube
SVF12N60F	TO-220F-3L	SVF12N60F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Ratings		Unit
		SVF12N60T	SVF12N60F	
Drain-Source Voltage	V_{DS}	600		V
Gate-Source Voltage	V_{GS}	±30		V
Drain Current	I_D	12		A
Drain Current Pulsed	I_{DM}	48		A
Power Dissipation(T_C=25°C)	P_D	225	51	W
-Derate above 25°C		1.8	0.41	W/°C
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	1268		mJ
Operation Junction Temperature	TJ	150		°C
Storage Temperature	T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVF12N60T	SVF12N60F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.56	2.44	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	120	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V	--	--	10	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=6.0A	--	0.58	0.8	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	1798	--	pF
Output Capacitance	C_{oss}		--	160	--	
Reverse Transfer Capacitance	C_{rss}		--	18.5	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V,I_D=12A, R_G=25Ω (Note 2,3)	--	28.6	--	ns
Turn-on Rise Time	t_r		--	74	--	
Turn-off Delay Time	$t_{d(off)}$		--	143.4	--	
Turn-off Fall Time	t_f		--	83	--	
Total Gate Charge	Q_g	V_{DS}=480V,I_D=12A, V_{GS}=10V (Note 2,3)	--	49.2	--	nC
Gate-Source Charge	Q_{gs}		--	9.0	--	
Gate-Drain Charge	Q_{gd}		--	17.8	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

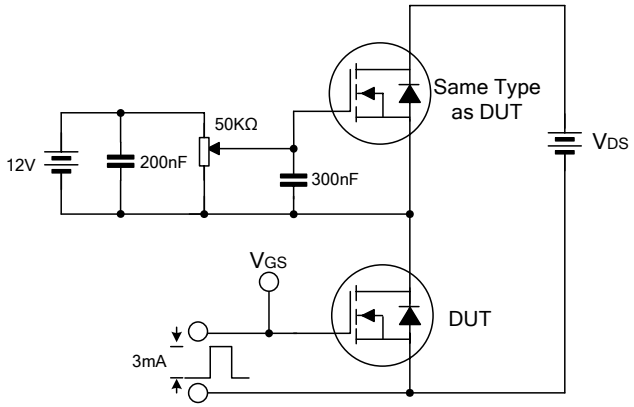
Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse p-n Junction Diode in the MOSFET	--	--	12	A
Pulsed Source Current	I_{SM}		--	--	48	
Diode Forward Voltage	V_{SD}	I_S=12A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=12A,V_{GS}=0V, dI_F/dt=100A/μS (Note 2)	--	411	--	ns
Reverse Recovery Charge	Q_{rr}		--	4.3	--	μC

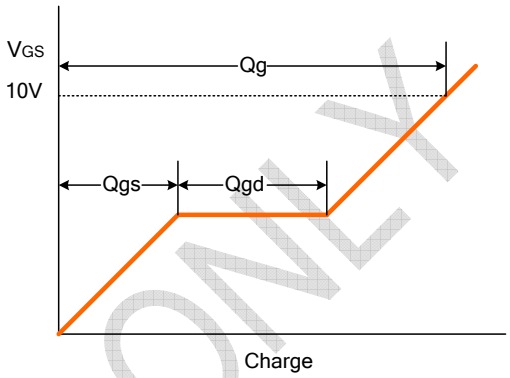
Notes:

1. L=30mH, I_{AS}=7.5A, V_{DD}=245V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

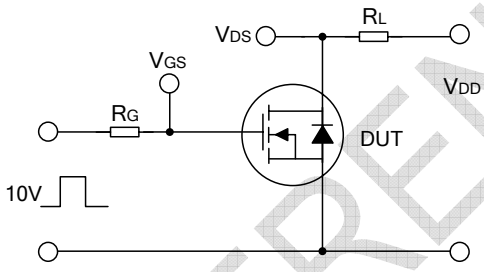
TYPICAL TEST CIRCUIT

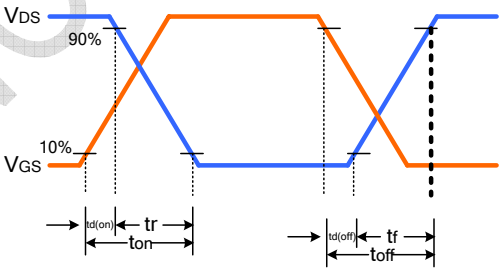
Gate Charge Test Circuit & Waveform



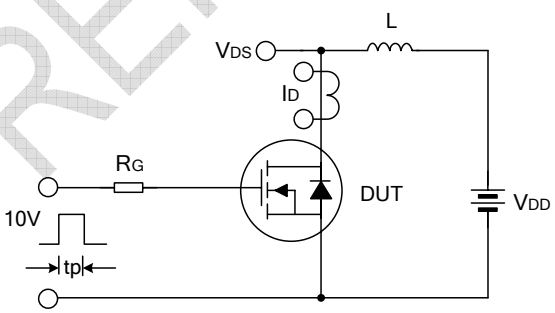


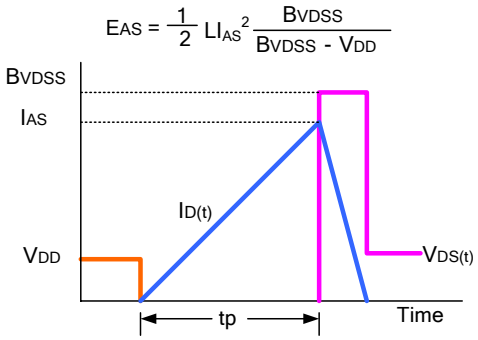
Resistive Switching Test Circuit & Waveform





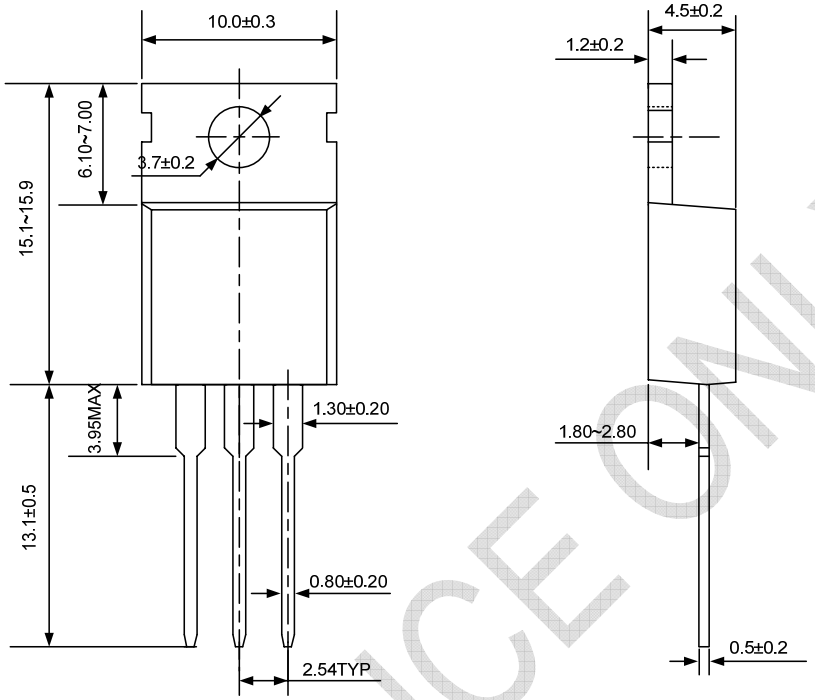
Unclamped Inductive Switching Test Circuit & Waveform





PACKAGE OUTLINE

TO-220-3L UNIT: mm



TO-220F-3L UNIT: mm