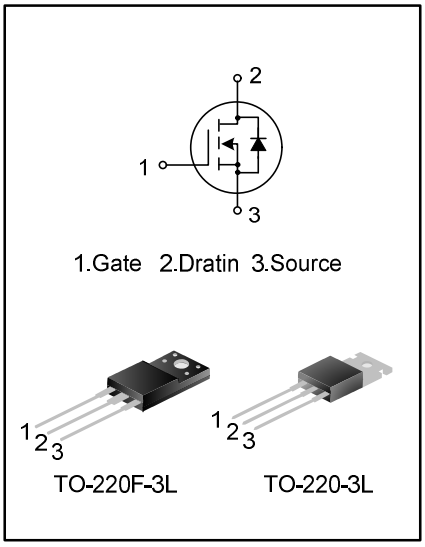
18A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF18N60F/T is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 18A,600V,$R_{DS(on)(typ.)}$=0.36Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE

S V F X N E X X X

Silan VDMOS Code of F-Cell process

Nominal current, using 1 or 2 digits:
Example:4 denotes 4A,
10 denotes 10A,
08 denotes 0.8A

N denotes N Channel

Special Features indication, May be omitted.
Example: E denotes embeded ESD structure

Nominal Voltage, using 2 digits
Example: 60 denotes 600V,
65 denotes 650V.

Package information.
Example:F:TO-220F;T:TO-220.

ORDERING INFORMATION

Part No.	Package	Marking	HAzardous Substance Control	Packing
SVF18N60F	TO-220F-3L	SVF18N60F	Pb free	Tube
SVF18N60T	TO-220-3L	SVF18N60T	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Ratings		Unit
			SVF18N60F	SVF18N60T	
Drain-Source Voltage		V_{DS}	600		V
Gate-Source Voltage		V_{GS}	±30		V
Drain Current	T_C=25°C	I_D	18		A
	T_C=100°C		11.4		
Drain Current Pulsed		I_{DM}	72		A
Power Dissipation(T_C=25°C)		P_D	54	225	W
-Derate above 25°C			0.43	1.8	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	1185		mJ
Operation Junction Temperature Range		T_J	-55～+150		°C
Storage Temperature Range		T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVF18N60F	SVF18N60T	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.31	0.56	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=9.0A	--	0.36	0.45	Ω
Gate Resistance	R_g	F=1MHz	--	5.0	--	Ω
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	--	2394.8	--	pF
Output Capacitance	C_{oss}		--	249.9	--	
Reverse Transfer Capacitance	C_{rss}		--	7.85	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V, I_D=18.0A, R_G=25Ω, (Note2,3)	--	38.92	--	ns
Turn-on Rise Time	t_r		--	60.28	--	
Turn-off Delay Time	$t_{d(off)}$		--	127.56	--	
Turn-off Fall Time	t_f		--	56.48	--	
Total Gate Charge	Q_g	V_{DS}=480V, I_D=18.0A, V_{GS}=10V, (Note 2,3)	--	46.35	--	nC
Gate-Source Charge	Q_{gs}		--	16.81	--	
Gate-Drain Charge	Q_{gd}		--	14.63	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode	--	--	18	A
Pulsed Source Current	I_{SM}	in the MOSFET	--	--	72	
Diode Forward Voltage	V_{SD}	I_S=18.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=18.0A,V_{GS}=0V,	--	615.69	--	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=100A/μs (Note 2)	--	7.40	--	μC

Notes:

1. L=30mH, I_{AS}=8.25, V_{DD}=50V, R_G=25Ω, starting TB_{JB}=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1 On-Region Characteristics

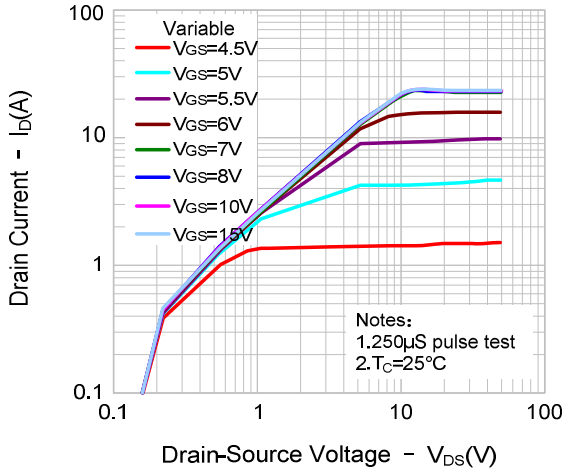


Figure 2 Transfer Characteristics

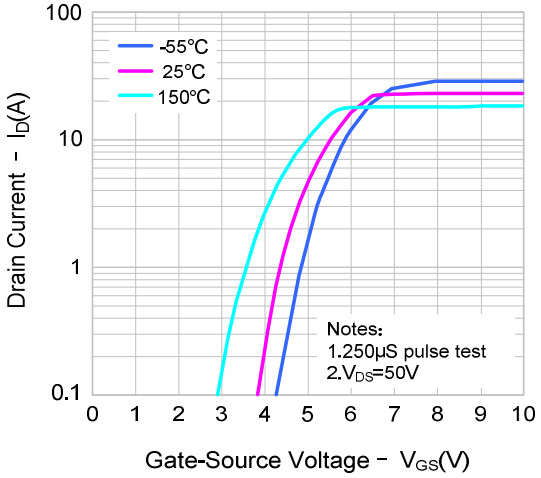


Figure 3 On-Resitance Variation vs Drain Current and Gate Voltage

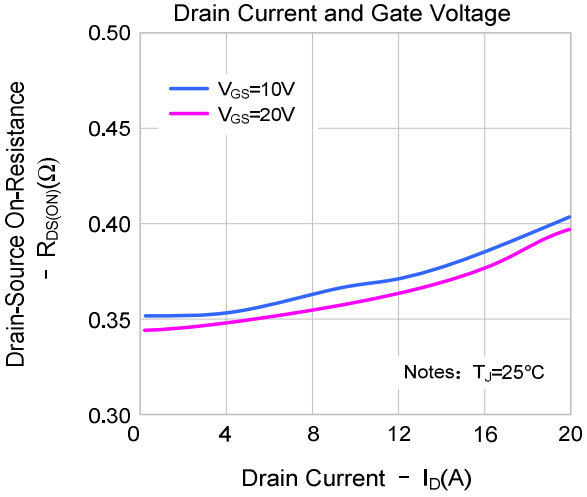


Figure 4 Body Diode Forward Voltage Variation vs Source Current and Temperature

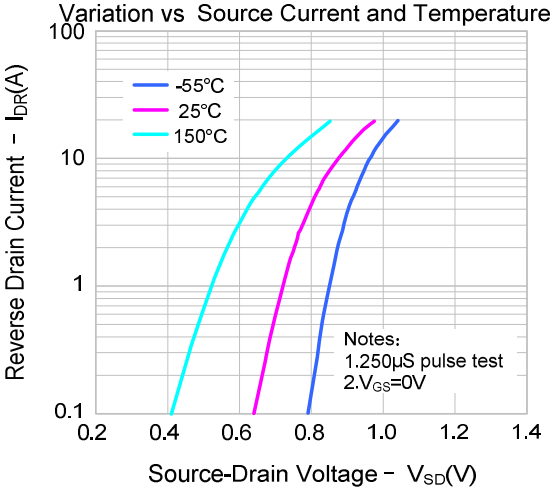


Figure 5 Capacitance Characteristics

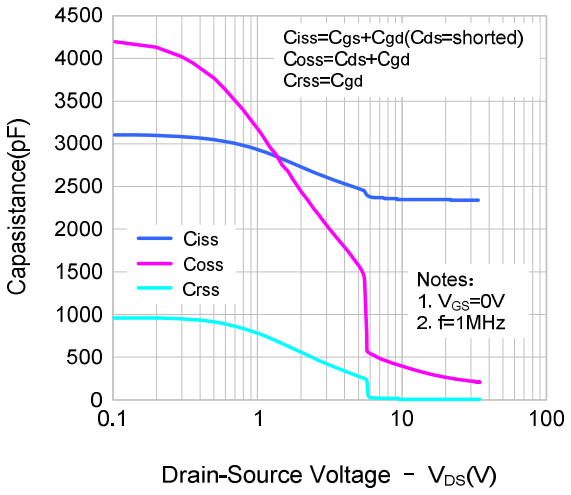
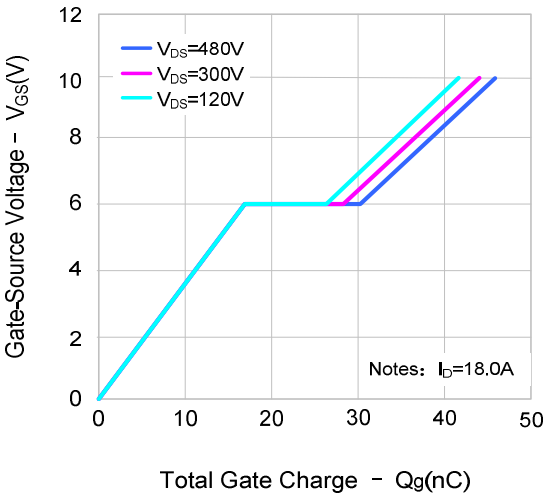


Figure 6 Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

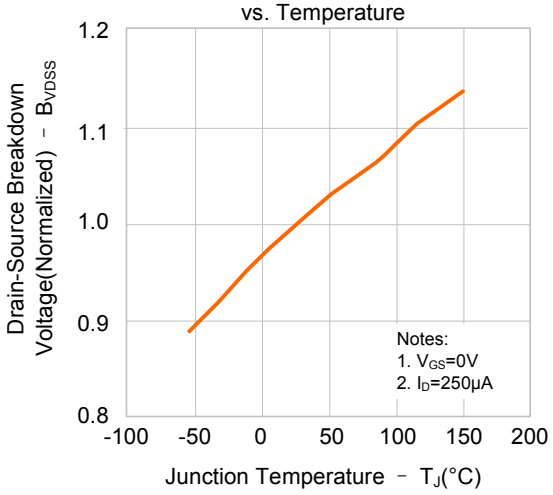


Figure 8. On-resistance Variation vs. Temperature

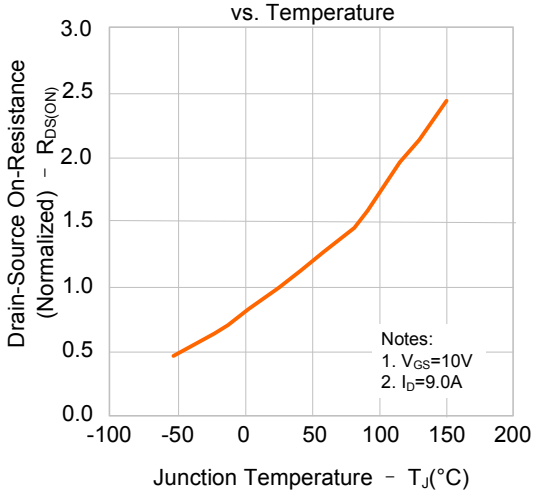


Figure 9-1. Max. Safe Operating Area(SVF18N60F)

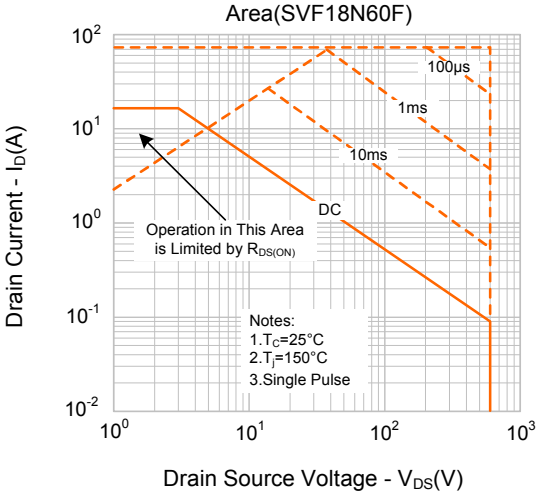


Figure 9-2. Max. Safe Operating Area(SVF18N60T)

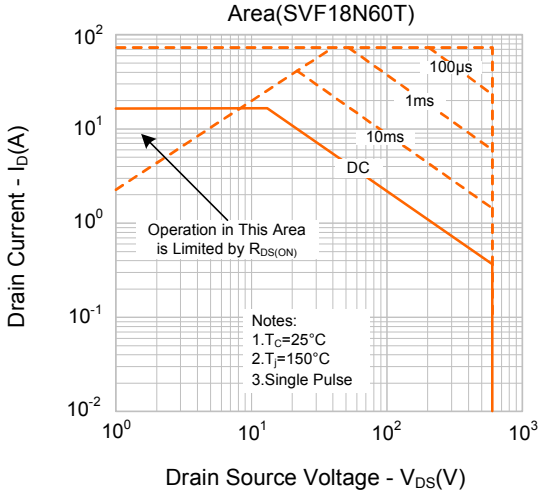
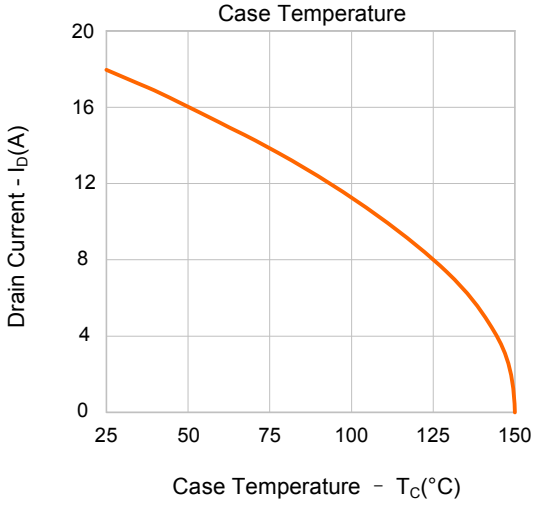
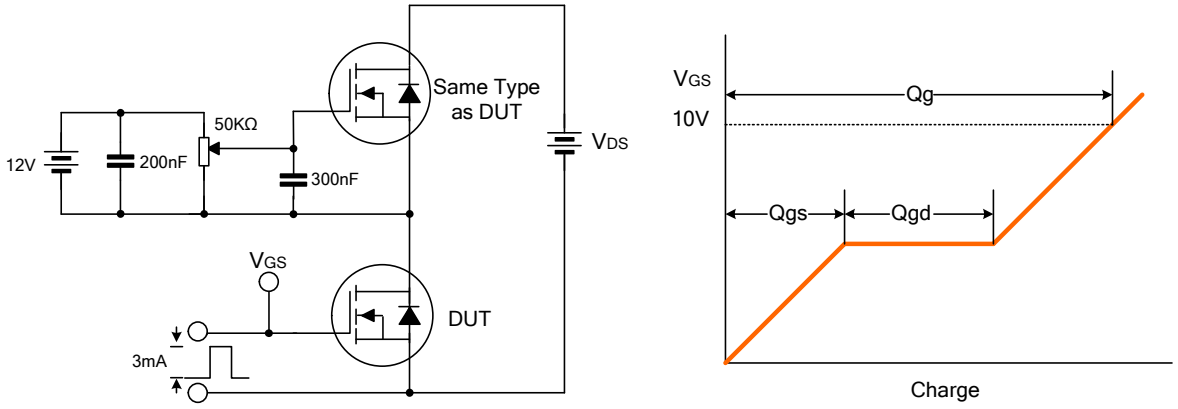


Figure 10. Maximum Drain Current vs. Case Temperature

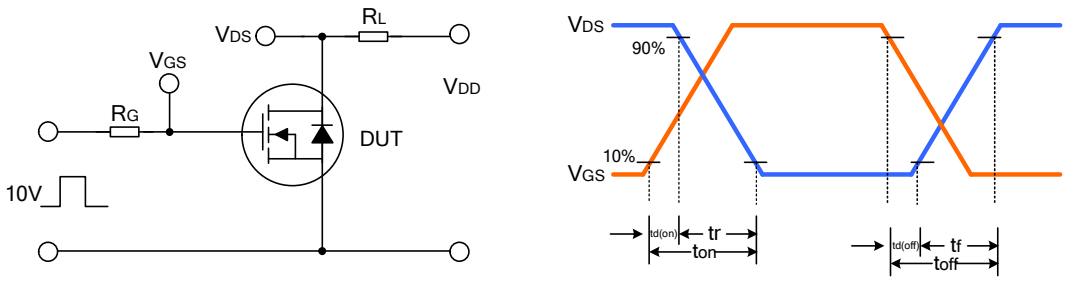


TYPICAL TEST CIRCUIT

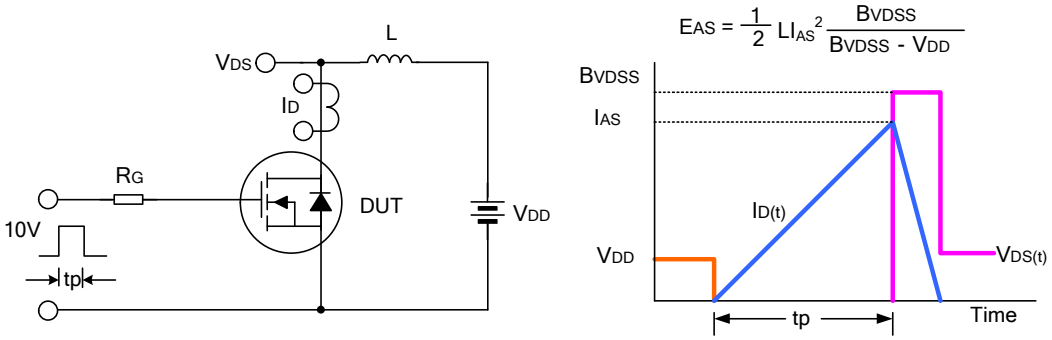
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



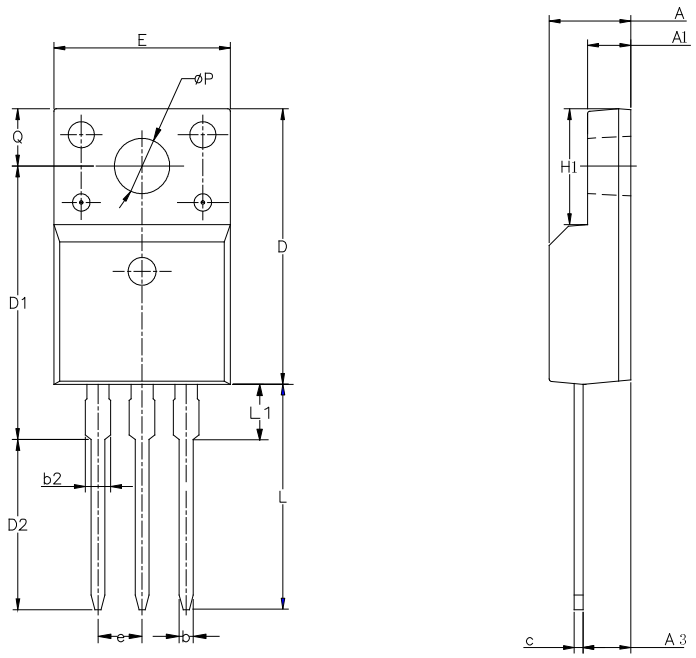
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220F-3L

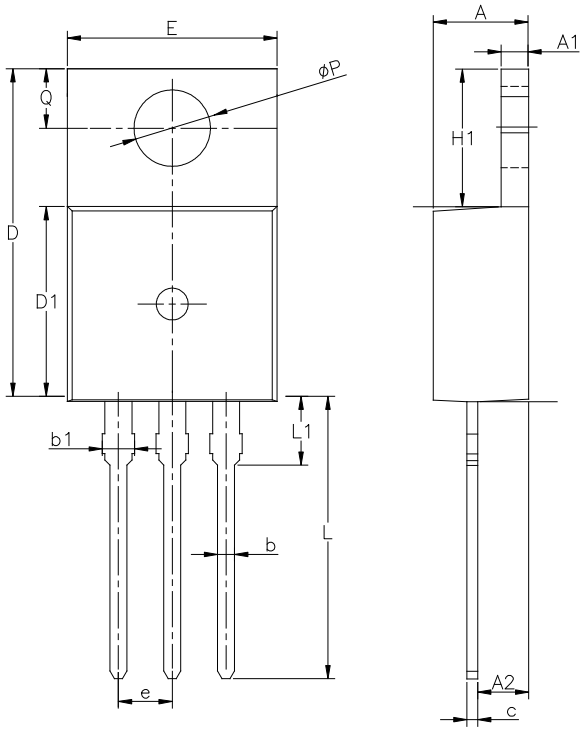
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
øP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-220-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
øP	3.40	3.70	3.90
Q	2.60	—	3.20

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1. Modify ELECTRICAL CHARACTERISTICS and Figure 3 and Figure 6

Rev.:	1.5	Author:	Yin Zi

Revision History:

1. Modify the package information of TO-220F-3L
2. Modify the package information of TO-220-3L

Rev.:	1.4	Author:	Yin Zi

Revision History:

1. Modify the thermal characteristics

Rev.:	1.3	Author:	Yin Zi

Revision History:

1. Add the package of TO-220-3L

Rev.:	1.2	Author:	Yin Zi

Revision History:

1. Modify the ordering information

Rev.:	1.1	Author:	Zhang Kefeng

Revision History:

1. Change the schematic diagram of MOS

Rev.:	1.0	Author:	Zhang Kefeng

Revision History:

1. Initial release