TIP140, TIP141, TIP142, (NPN); TIP145, TIP146, TIP147, (PNP)

Darlington Complementary Silicon Power Transistors

Designed for general−purpose amplifier and low frequency switching applications.

Features

- High DC Current Gain −
  Min h_{FE} = 1000 @ I_C
  = 5.0 A, V_{CE} = 4 V
- Collector−Emitter Sustaining Voltage − @ 30 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) − TIP140, TIP145
  = 80 Vdc (Min) − TIP141, TIP146
  = 100 Vdc (Min) − TIP142, TIP147
- Monolithic Construction with Built−In Base−Emitter Shunt Resistor
- These are Pb−Free Devices*

MAXIMUM RATINGS

Rating	Symbol	TIP140 TIP145	TIP141 TIP146	TIP142 TIP147	Unit
Collector − Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector − Base Voltage	V_{CB}	60	80	100	Vdc
Emitter − Base Voltage	V_{EB}	5.0			Vdc
Collector Current − Continuous − Peak (Note 1)	I_C	10 15			Adc
Base Current − Continuous	I_B	0.5			Adc
Total Power Dissipation @ T_C = 25°C	P_D	125			W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	35.7	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

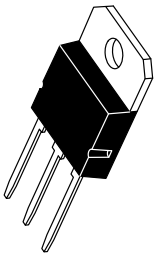
1. 5 ms, ≤ 10% Duty Cycle.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

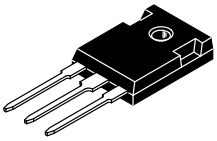
ON Semiconductor®

http://onsemi.com

10 AMPERE DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 60−100 VOLTS, 125 WATTS



SOT−93 (TO−218)
CASE 340D
STYLE 1



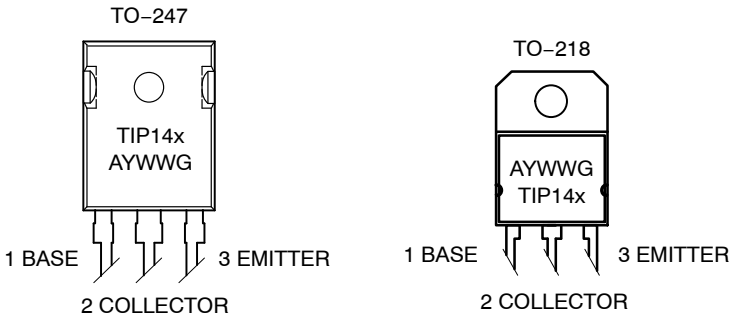
TO−247
CASE 340L
STYLE 3

NOTE: Effective June 2012 this device will be available only in the TO−247 package. Reference FPCN# 16827.

ORDERING INFORMATION

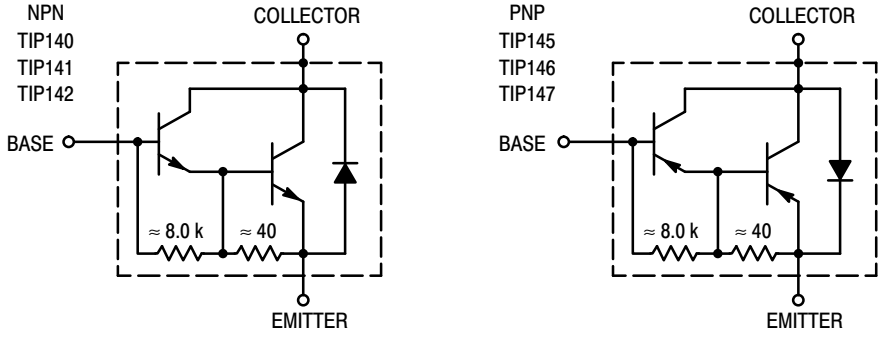
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MARKING DIAGRAMS



TIP14x	= Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

DARLINGTON SCHEMATICS



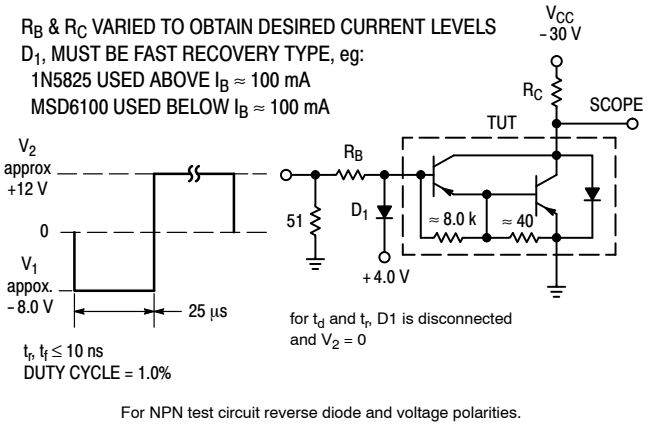
ORDERING INFORMATION

Device	Package	Shipping
TIP140G	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP141G	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP142G	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP145G	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP146G	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP147G	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP140G	TO−247 (Pb−Free)	30 Units / Rail
TIP141G	TO−247 (Pb−Free)	30 Units / Rail
TIP142G	TO−247 (Pb−Free)	30 Units / Rail
TIP145G	TO−247 (Pb−Free)	30 Units / Rail
TIP146G	TO−247 (Pb−Free)	30 Units / Rail
TIP147G	TO−247 (Pb−Free)	30 Units / Rail

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Sustaining Voltage (Note 2)		$V_{CEO(sus)}$				Vdc
(I_C = 30 mA, I_B = 0)	TIP140, TIP145		60	–	–	
	TIP141, TIP146		80	–	–	
	TIP142, TIP147		100	–	–	
Collector Cutoff Current		I_{CEO}				mA
(V_{CE} = 30 Vdc, I_B = 0)	TIP140, TIP145		–	–	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	TIP141, TIP146		–	–	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	TIP142, TIP147		–	–	2.0	
Collector Cutoff Current		I_{CBO}				mA
(V_{CB} = 60 V, I_E = 0)	TIP140, TIP145		–	–	1.0	
(V_{CB} = 80 V, I_E = 0)	TIP141, TIP146		–	–	1.0	
(V_{CB} = 100 V, I_E = 0)	TIP142, TIP147		–	–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 V)		I_{EBO}	–	–	2 0	mA
ON CHARACTERISTICS (Note 2)						
DC Current Gain		h_{FE}				–
(I_C = 5.0 A, V_{CE} = 4.0 V)			1000	–	–	
(I_C = 10 A, V_{CE} = 4.0 V)			500	–	–	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5.0 A, I_B = 10 mA)			–	–	2.0	
(I_C = 10 A, I_B = 40 mA)			–	–	3.0	
Base−Emitter Saturation Voltage (I_C = 10 A, I_B = 40 mA)		$V_{BE(sat)}$	–	–	3.5	Vdc
Base−Emitter On Voltage		$V_{BE(on)}$	–	–	3.0	Vdc
(I_C = 10 A, V_{CE} = 4.0 Vdc)						
SWITCHING CHARACTERISTICS						
Resistive Load (See Figure 1)						
Delay Time	(V_{CC} = 30 V, I_C = 5.0 A, I_B = 20 mA, Duty Cycle ≤ 2.0%, I_{B1} = I_{B2}, R_C & R_B Varied, T_J = 25°C)	t_d	–	0.15	–	μs
Rise Time		t_r	–	0.55	–	μs
Storage Time		t_s	–	2.5	–	μs
Fall Time		t_f	–	2.5	–	μs

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 1. Switching Times Test Circuit

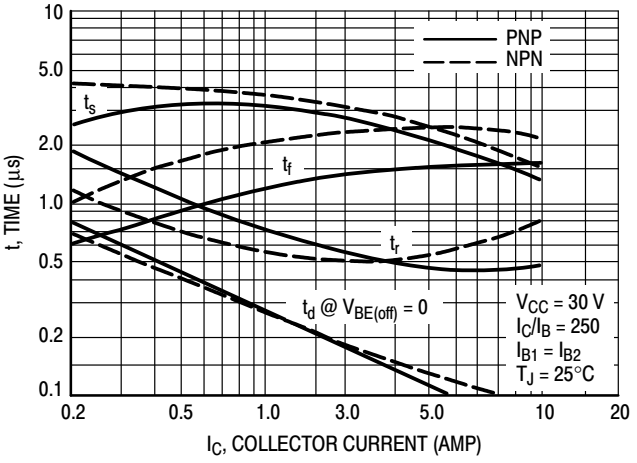
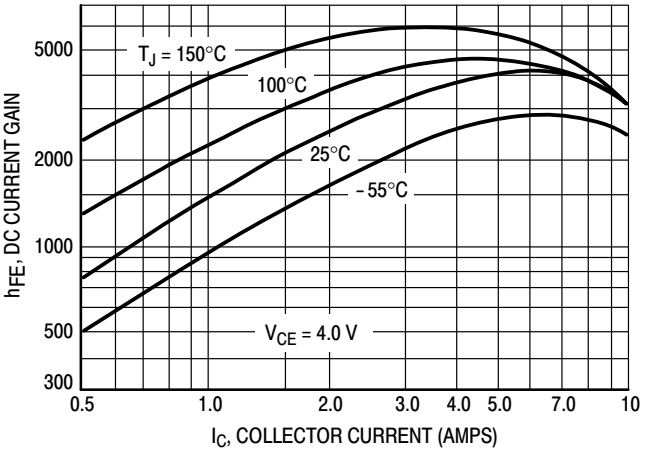


Figure 2. Switching Times

TYPICAL CHARACTERISTICS

NPN
TIP140, TIP141, TIP142



PNP
TIP145, TIP146, TIP147

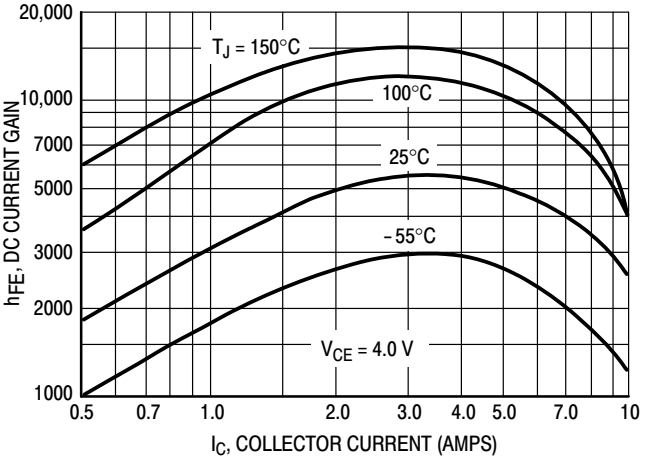
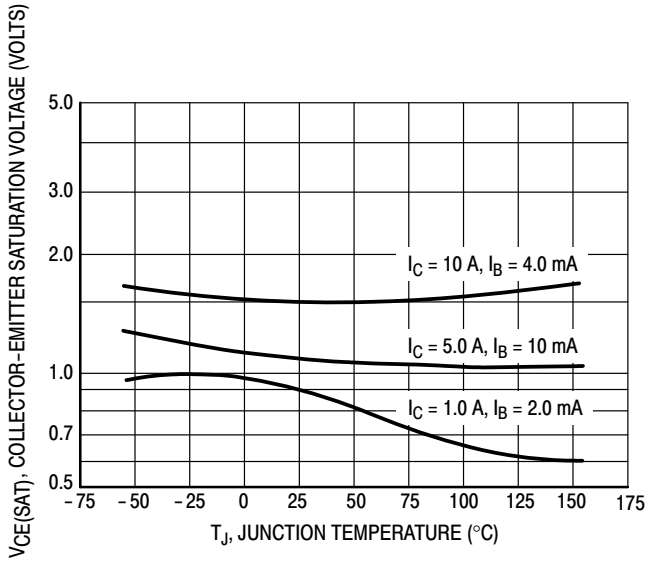


Figure 3. DC Current Gain versus Collector Current



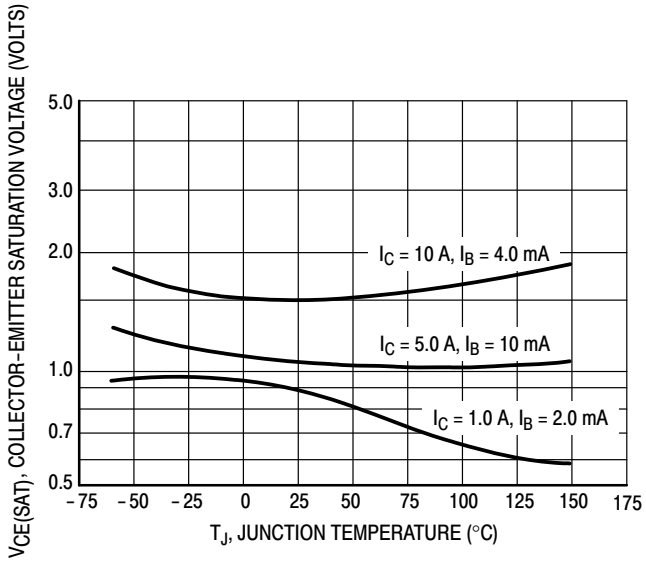
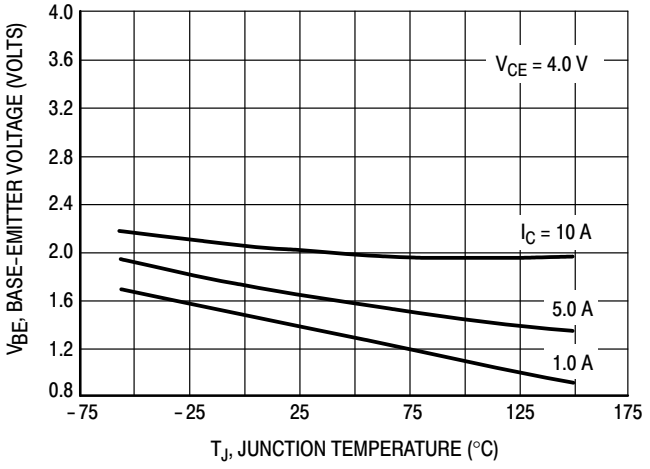


Figure 4. Collector−Emitter Saturation Voltage



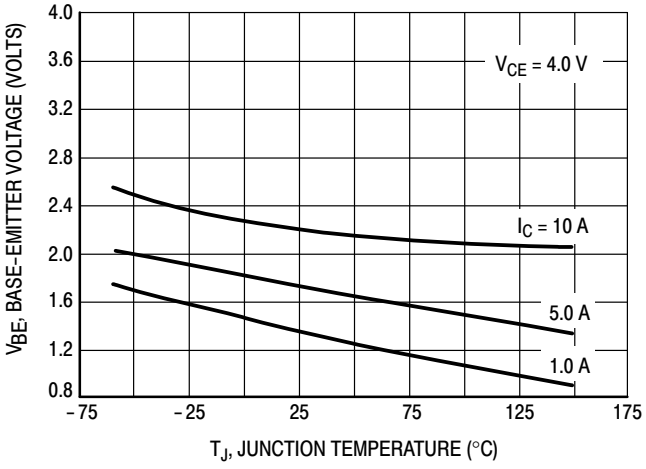


Figure 5. Base−Emitter Voltage

ACTIVE−REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

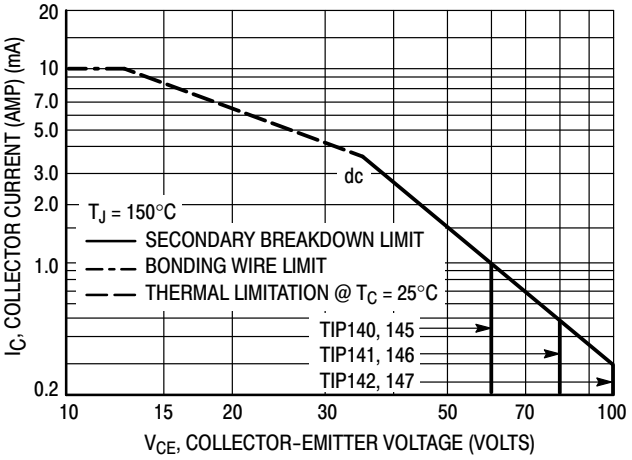


Figure 6. Active−Region Safe Operating Area

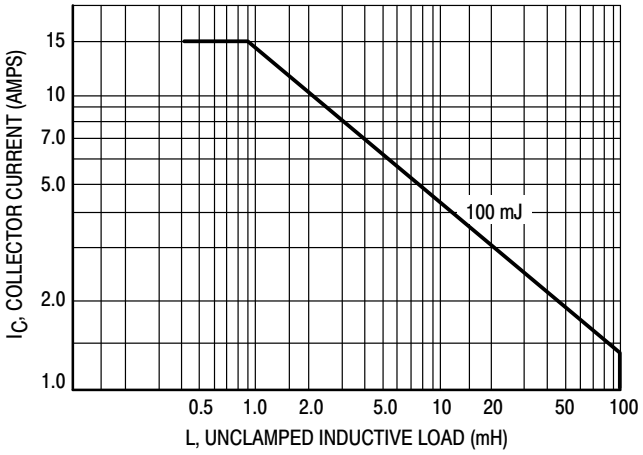
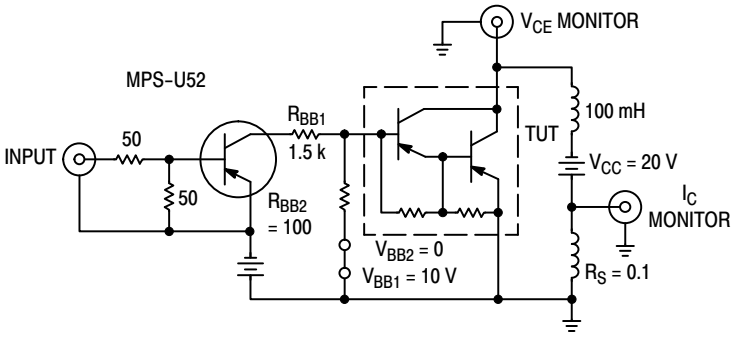
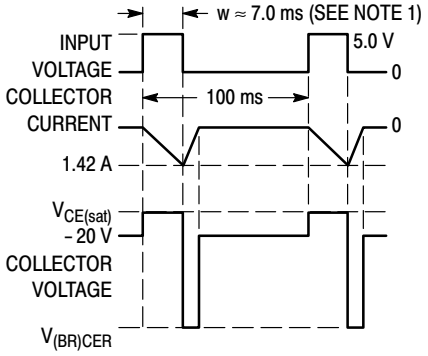


Figure 7. Unclamped Inductive Load



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTE 1: Input pulse width is increased until I_{CM} = 1.42 A.
NOTE 2: For NPN test circuit reverse polarities.

Figure 8. Inductive Load

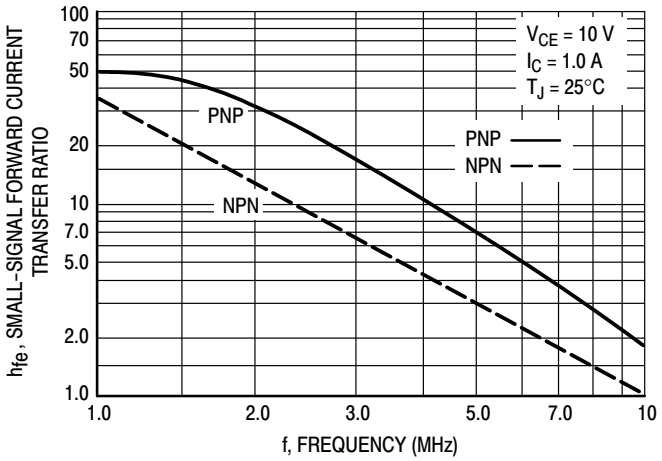


Figure 9. Magnitude of Common Emitter Small−Signal Short−Circuit Forward Current Transfer Ratio

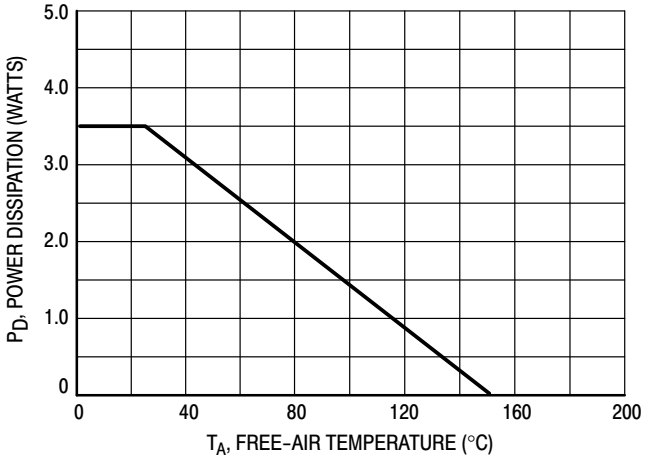


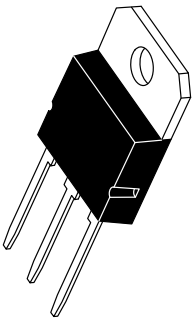
Figure 10. Free−Air Temperature Power Derating

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

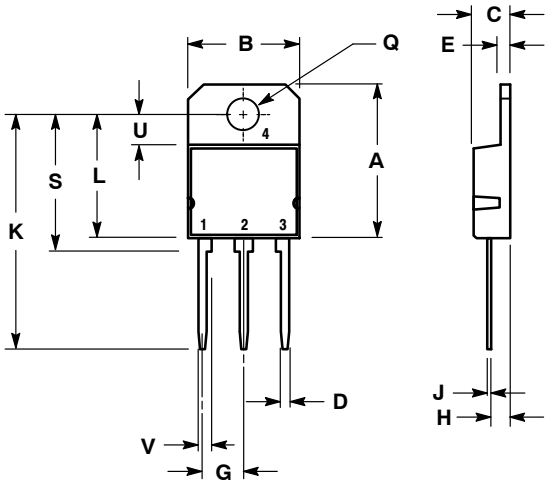
ON Semiconductor®

SOT−93 (TO−218)
CASE 340D−02
ISSUE E

DATE 01/03/2002



SCALE 1:1



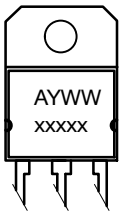
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
xxxxx = Device Code

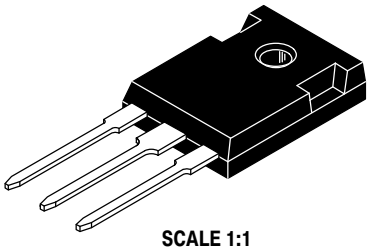
DOCUMENT NUMBER:	**98ASB42643B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOT−93**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

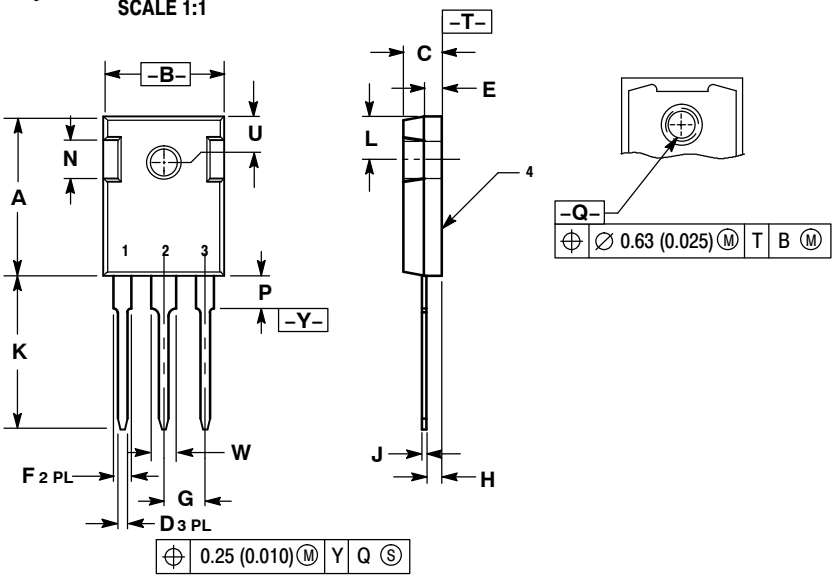
ON Semiconductor®

TO−247
CASE 340L−02
ISSUE F

DATE 26 OCT 2011



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	8.30
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)

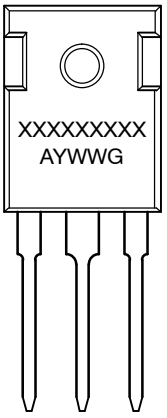
STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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ISSUE	REVISION	DATE
D	CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80–21.46/0.819–0.845. DIM K WAS 19.81–20.32/0.780–0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES.	25 AUG 2000
E	DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN.	26 FEB 2010
F	ADDED STYLES 5 AND 6. REQ. BY J. PEREZ.	26 OCT 2011

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