

# TIP41, TIP41A, TIP41B, TIP41C (NPN); TIP42, TIP42A, TIP42B, TIP42C (PNP)



ON Semiconductor®

<http://onsemi.com>

## Complementary Silicon Plastic Power Transistors

Designed for use in general purpose amplifier and switching applications.

### Features

- ESD Ratings: Machine Model, C; > 400 V  
Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94 V-0 @ 0.125 in
- Pb-Free Packages are Available\*

**6 AMPERE  
COMPLEMENTARY SILICON  
POWER TRANSISTORS  
40–60–80–100 VOLTS,  
65 WATTS**

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	$V_{CEO}$	40 60 80 100	Vdc
Collector–Base Voltage TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	$V_{CB}$	40 60 80 100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current– Continuous Peak	$I_C$	6.0 10	Adc
Base Current	$I_B$	2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	65 0.52	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016	W W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (Note 1)	E	62.5	mJ
Operating and Storage Junction, Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

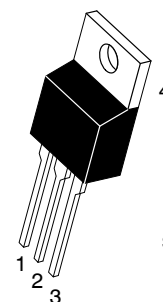
### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	57	$^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $I_C = 2.5\text{ A}$ ,  $L = 20\text{ mH}$ , P.R.F. = 10 Hz,  $V_{CC} = 10\text{ V}$ ,  $R_{BE} = 100\ \Omega$ .

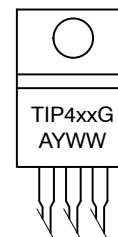
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



TO-220AB  
CASE 221A  
STYLE 1

STYLE 1:  
PIN 1: BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

### MARKING DIAGRAM



TIP4xx = Device Code  
xx = 1, 1A, 1B, 1C  
2, 2A, 2B, 2C  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

## TIP41, TIP41A, TIP41B, TIP41C (NPN); TIP42, TIP42A, TIP42B, TIP42C (PNP)

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

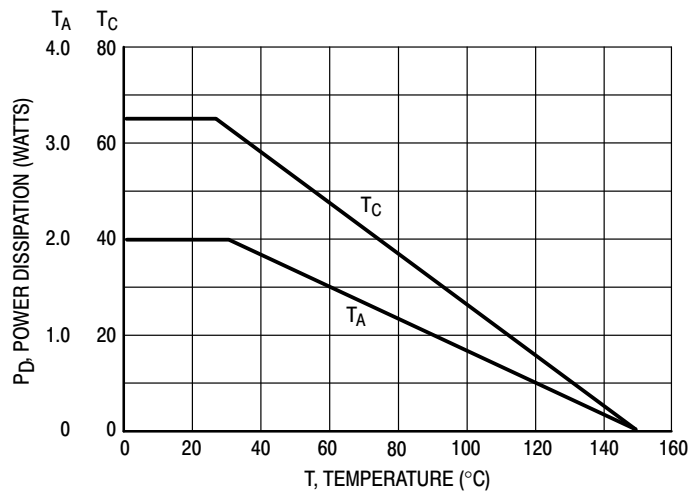
Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (Note 2) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	$V_{CE(sus)}$	40 60 80 100	– – – –	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ )	TIP41, TIP41A, TIP42, TIP42A TIP41B, TIP41C, TIP42B, TIP42C	$I_{CEO}$	– –	0.7 0.7	mAdc
Collector Cutoff Current ( $V_{CE} = 40\text{ Vdc}$ , $V_{EB} = 0$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB} = 0$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB} = 0$ ) ( $V_{CE} = 100\text{ Vdc}$ , $V_{EB} = 0$ )	TIP41, TIP42 TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	$I_{CES}$	– – – –	400 400 400 400	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	–	1.0	mAdc
<b>ON CHARACTERISTICS (Note 2)</b>					
DC Current Gain ( $I_C = 0.3\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )		$h_{FE}$	30 15	– 75	–
Collector–Emitter Saturation Voltage ( $I_C = 6.0\text{ Adc}$ , $I_B = 600\text{ mAdc}$ )		$V_{CE(sat)}$	–	1.5	Vdc
Base–Emitter On Voltage ( $I_C = 6.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )		$V_{BE(on)}$	–	2.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>					
Current–Gain — Bandwidth Product ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )		$f_T$	3.0	–	MHz
Small–Signal Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )		$h_{fe}$	20	–	–

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

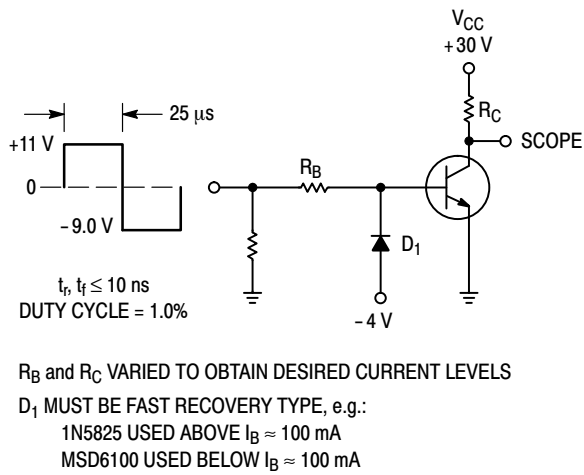
### ORDERING INFORMATION

Device	Package	Shipping
TIP41	TO-220	50 Units / Rail
TIP41G	TO-220 (Pb-Free)	50 Units / Rail
TIP41A	TO-220	50 Units / Rail
TIP41AG	TO-220 (Pb-Free)	50 Units / Rail
TIP41B	TO-220	50 Units / Rail
TIP41BG	TO-220 (Pb-Free)	50 Units / Rail
TIP41C	TO-220	50 Units / Rail
TIP41CG	TO-220 (Pb-Free)	50 Units / Rail
TIP42	TO-220	50 Units / Rail
TIP42G	TO-220 (Pb-Free)	50 Units / Rail
TIP42A	TO-220	50 Units / Rail
TIP42AG	TO-220 (Pb-Free)	50 Units / Rail
TIP42B	TO-220	50 Units / Rail
TIP42BG	TO-220 (Pb-Free)	50 Units / Rail
TIP42C	TO-220	50 Units / Rail
TIP42CG	TO-220 (Pb-Free)	50 Units / Rail

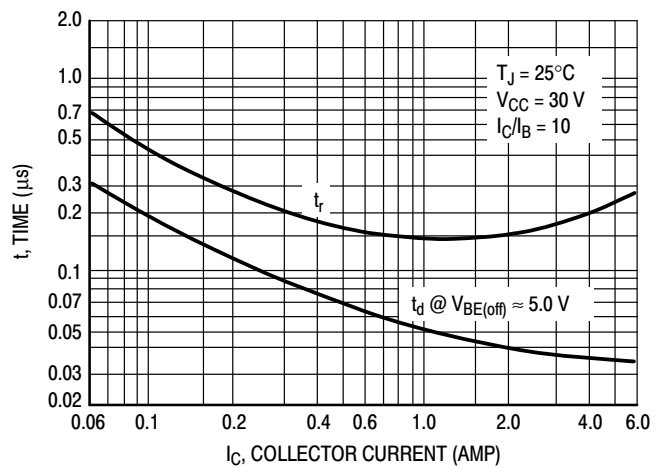
**TIP41, TIP41A, TIP41B, TIP41C (NPN); TIP42, TIP42A, TIP42B, TIP42C (PNP)**



**Figure 1. Power Derating**



**Figure 2. Switching Time Test Circuit**



**Figure 3. Turn-On Time**

TIP41, TIP41A, TIP41B, TIP41C (NPN); TIP42, TIP42A, TIP42B, TIP42C (PNP)

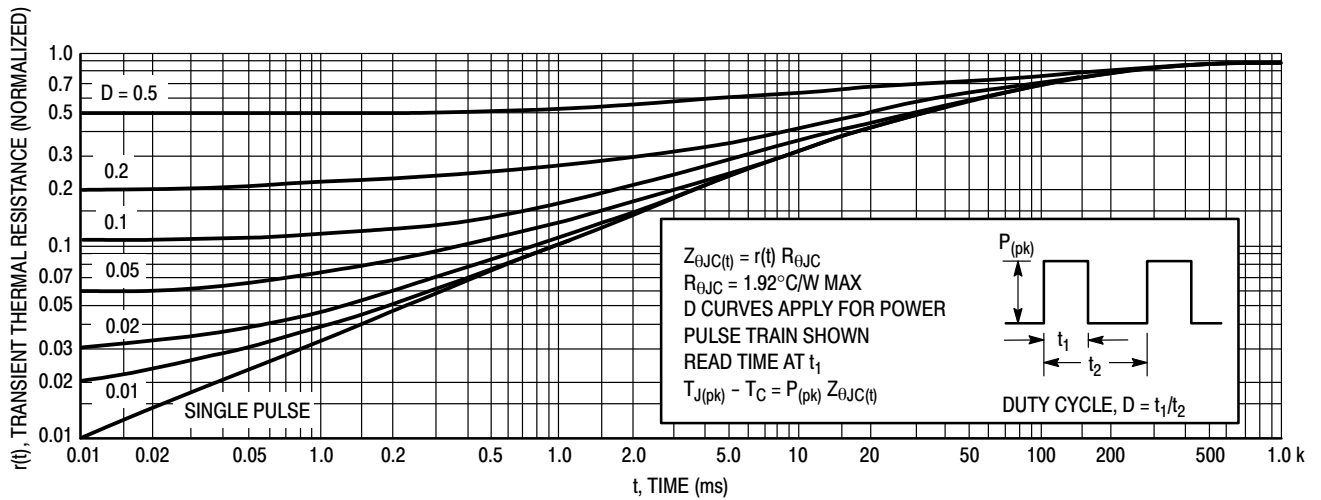


Figure 4. Thermal Response

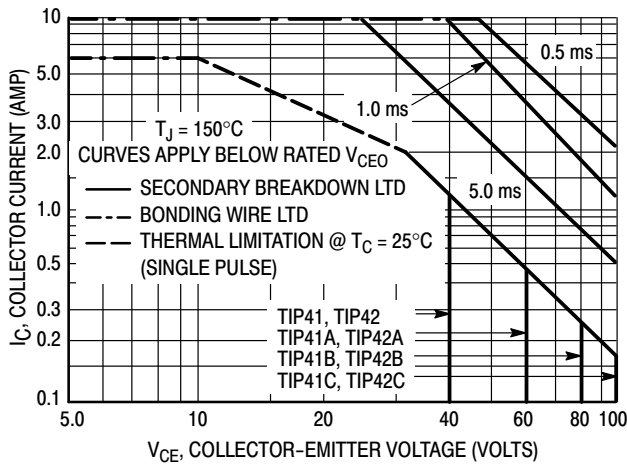


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

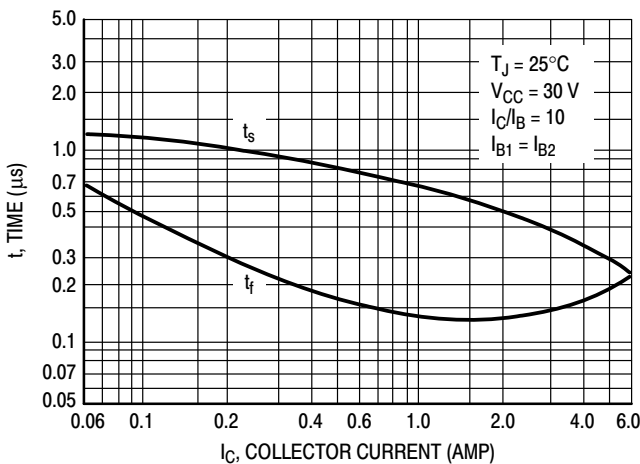


Figure 6. Turn-Off Time

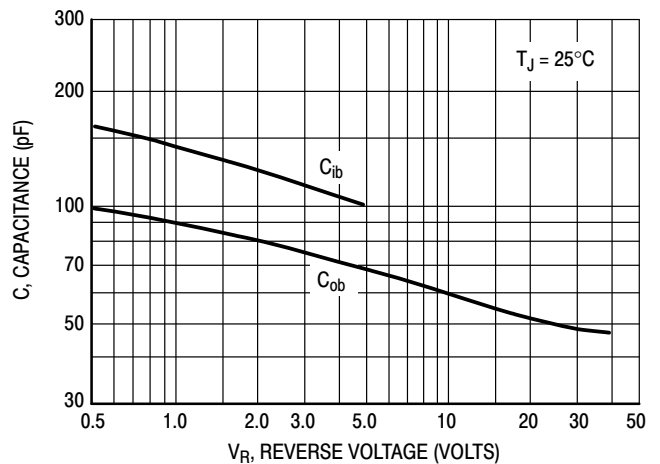


Figure 7. Capacitance

TIP41, TIP41A, TIP41B, TIP41C (NPN); TIP42, TIP42A, TIP42B, TIP42C (PNP)

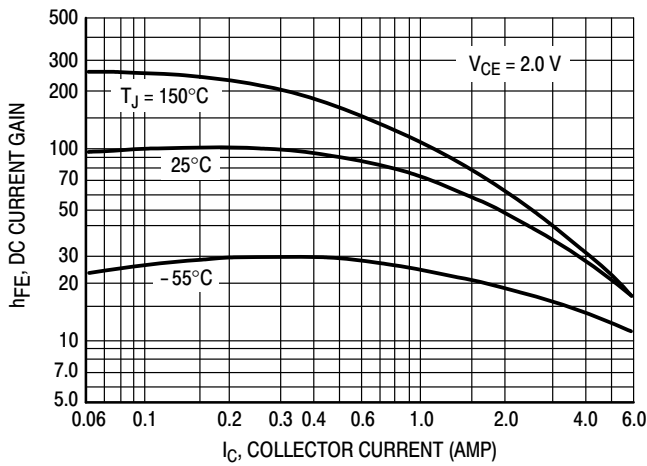


Figure 8. DC Current Gain

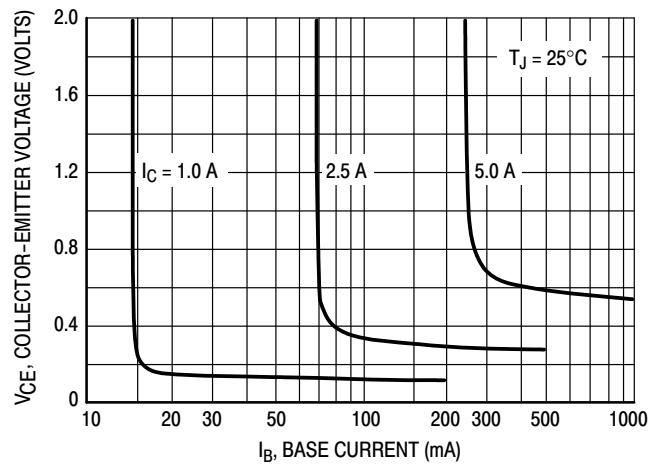


Figure 9. Collector Saturation Region

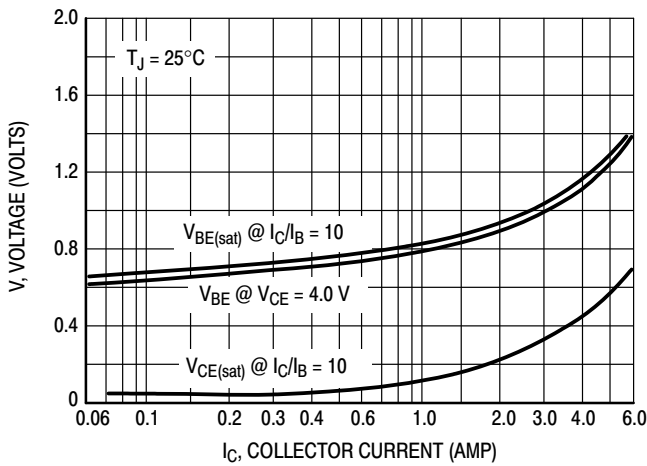


Figure 10. "On" Voltages

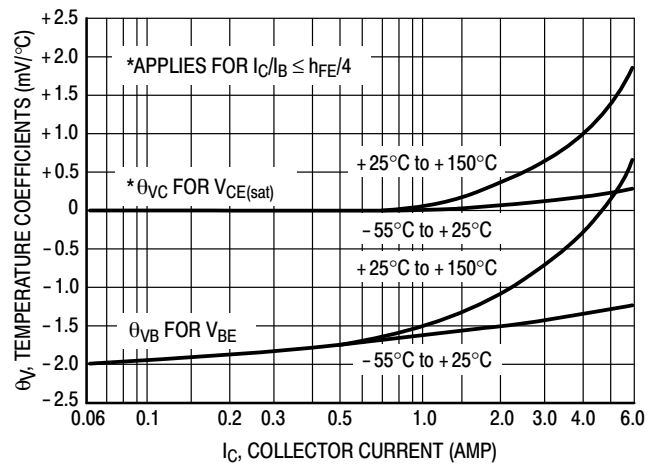


Figure 11. Temperature Coefficients

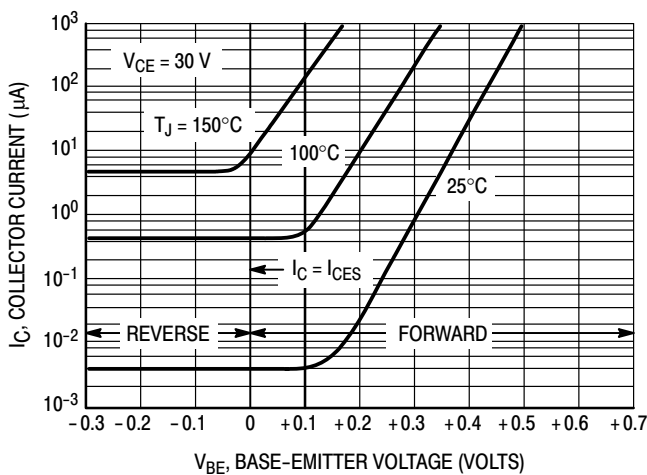


Figure 12. Collector Cut-Off Region

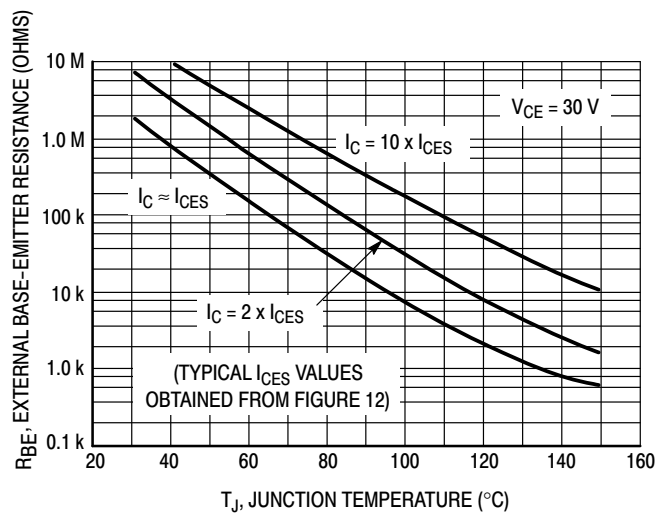
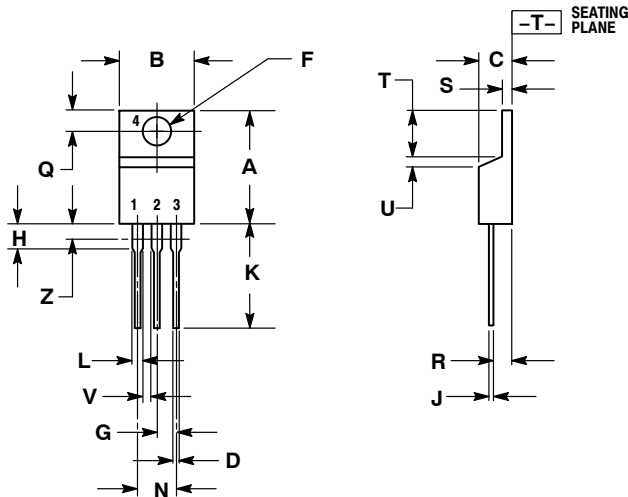


Figure 13. Effects of Base-Emitter Resistance

# TIP41, TIP41A, TIP41B, TIP41C (NPN); TIP42, TIP42A, TIP42B, TIP42C (PNP)

## PACKAGE DIMENSIONS

TO-220  
CASE 221A-09  
ISSUE AG




### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.036	0.64	0.91
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

### STYLE 1:

- PIN 1. BASE
- COLLECTOR
- EMITTER
- COLLECTOR

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TIP41A/D