

TL06xx Low-Power JFET-Input Operational Amplifiers

1 Features

- Very Low Power Consumption
- Typical Supply Current: 200 μ A (Per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common-Mode Input Voltage Range Includes V_{CC+}
- Output Short-Circuit Protection
- High Input Impedance: JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate: 3.5 V/ μ s Typical
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Tablets
- White goods
- Personal electronics
- Computers

3 Description

The JFET-input operational amplifiers of the TL06x series are designed as low-power versions of the TL08x series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and input bias currents. The TL06x series features the same terminal assignments as the TL07x and TL08x series.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL06xxD	SOIC (14)	8.65 mm x 3.91 mm
TL06xxJ	CDIP (14)	19.56 mm x 6.92 mm
TL06xxN	PDIP (14)	19.30 mm x 6.35 mm
TL06xxNS	SO (14)	10.30 mm x 5.30 mm
TL06xxPW	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic Symbol

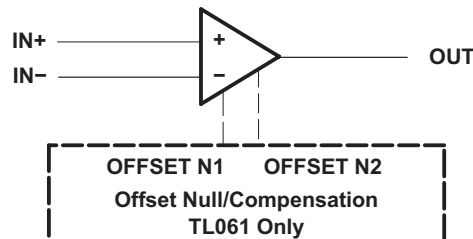


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4 Revision History

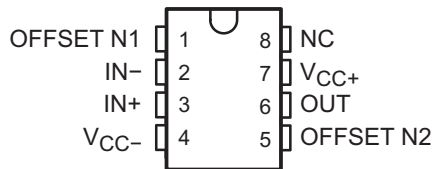
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (January 2014) to Revision L	Page
• Added <i>Applications</i>	1
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

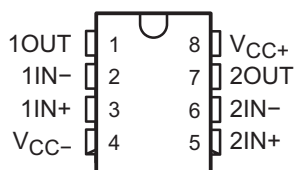
Changes from Revision J (September 2004) to Revision K	Page
• Updated document to new TI data sheet format - no specification changes.	1
• Deleted <i>Ordering Information</i> table.	1
• Updated <i>Features</i> with Military Disclaimer.	1

5 Pin Configuration and Functions

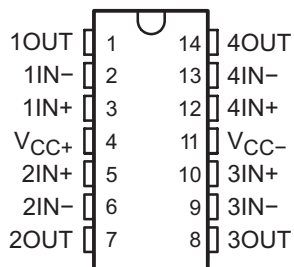
TL061x D, P, and PS Package
8-Pin SOIC, PDIP, and SO
Top View



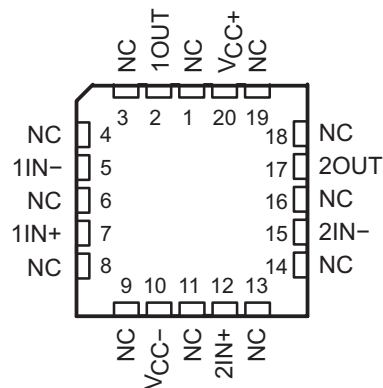
TL062x D, JG, P, PS, and PW Package
8-Pin SOIC, CDIP, PDIP, SO, and TSSOP
Top View



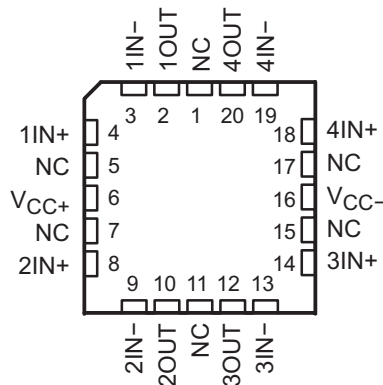
TL064x D, J, N, NS, PW, and W Package
14-Pin SOIC, CDIP, PDIP, SO, TSSOP and CFP
Top View



TL062 FK Package
20-Pin LCCC
Top View



TL064 FK Package
20-Pin LCCC
Top View



Pin Functions

NAME	PIN					TYPE	DESCRIPTION
	TL061	TL062		TL064			
	D, P, PS	D, JG, P, PS, PW	FK	D, J, N, NS, PW, W	FK		
1IN-	—	2	5	2	3	I	Negative input
1IN+	—	3	7	3	4	I	Positive input
1OUT	—	1	2	1	2	O	Output
2IN-	—	6	15	6	9	I	Negative input
2IN+	—	5	12	5	8	I	Positive input
2OUT	—	7	17	7	10	O	Output
3IN-	—	—	—	9	13	I	Negative input
3IN+	—	—	—	10	14	I	Positive input
3OUT	—	—	—	8	12	O	Output
4IN-	—	—	—	13	19	I	Negative input
4IN+	—	—	—	12	18	I	Positive input
4OUT	—	—	—	14	20	O	Output
IN-	2	—	—	—	—	I	Negative input

Pin Functions (continued)

NAME	PIN					TYPE	DESCRIPTION
	TL061	TL062		TL064			
	D, P, PS	D, JG, P, PS, PW	FK	D, J, N, NS, PW, W	FK		
IN+	3	—	—	—	—	I	Positive input
NC	8	—	1	—	1	—	Do not connect
			3		5		
			4		7		
			6		11		
			8		15		
			9		17		
			11				
			13				
			14				
			16				
18							
19							
OFFSET N1	1	—	—	—	—	—	Input offset adjustment
OFFSET N2	5	—	—	—	—	—	Input offset adjustment
OUT	6	—	—	—	—	O	Output
V _{CC-}	4	4	10	11	16	—	Power supply
V _{CC+}	7	8	20	4	6	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC+}	Supply voltage ⁽²⁾		18	V
V _{CC-}			-18	
V _{ID}	Differential input voltage ⁽³⁾		±30	V
V _I	Input voltage ⁽²⁾⁽⁴⁾		±15	V
	Duration of output short circuit ⁽⁵⁾		Unlimited	
T _J	Operating virtual junction temperature		150	°C
	Case temperature for 60 seconds	FK package	260	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package	300	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, N, NS, P, PS, or PW package	260	°C
T _{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

(3) Differential voltages are at IN+, with respect to IN-.

(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC+} Supply voltage		5	15	V
V_{CC-} Supply voltage		-5	-15	V
V_{CM} Common-mode voltage		$V_{CC-} + 4$	$V_{CC+} - 4$	V
T_A Ambient temperature	TL06xM	-55	125	°C
	TL06xQ	-40	125	
	TL06xI	-40	85	
	TL06xC	0	70	

6.4 Thermal Information - 8 Pins

THERMAL METRIC ⁽¹⁾	TL06xx					UNIT
	D (SOIC)	P (PDIP)	PS (SO)	PW (TSSOP)	JG (CDIP)	
	8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance ⁽²⁾⁽³⁾	97	85	95	149	—	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance ⁽⁴⁾⁽⁵⁾	—	—	—	—	14.5	°C/W

6.5 Thermal Information - 14 Pins

THERMAL METRIC ⁽¹⁾	TL06xx							UNIT
	D (SOIC)	N (PDIP)	NS (SO)	PS (SO)	PW (TSSOP)	J (CDIP)	W (CFP)	
	14 PINS	14 PINS	14 PINS	8 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance ⁽²⁾⁽³⁾	86	80	76	95	113	—	—	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance ⁽²⁾⁽³⁾	—	—	—	—	—	15.05	14.65	°C/W

**TL061, TL061A, TL061B
TL062, TL062A, TL062B, TL064, TL064A, TL064B**

SLOS078L – NOVEMBER 1978 – REVISED MAY 2015

6.6 Thermal Information - 20 Pins

THERMAL METRIC ⁽¹⁾		TL06xx	UNIT
		FK (LCCC)	
		20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽²⁾⁽³⁾	—	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance ⁽⁴⁾⁽⁵⁾	5.61	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) Maximum power dissipation is a function of T_{J(max)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} – T_A)/R_{θJA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) Maximum power dissipation is a function of T_{J(max)}, R_{θJC}, and T_C. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} – T_C) / R_{θJC}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with MIL-STD-883.

6.7 Electrical Characteristics for TL06xC and TL06xxC

 V_{CC±} = ±15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	TL061C, TL062C, TL064C			TL061AC, TL062AC, TL064AC			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage V _O = 0, R _S = 50 Ω	T _A = 25°C		3	15	3		6	mV
		T _A = Full range		20		7.5			
α _{VIO}	Temperature coefficient of input offset voltage V _O = 0, R _S = 50 Ω, T _A = Full range	10			10			μV/°C	
I _{IO}	Input offset current V _O = 0	T _A = 25°C		5	200	5	100	pA	
		T _A = Full range		5		3		nA	
I _{IB}	Input bias current ⁽²⁾ V _O = 0	T _A = 25°C		30	400	30	200	pA	
		T _A = Full range		10		7		nA	
V _{ICR}	Common-mode input voltage range T _A = 25°C	±11	–12 to 15	±11	–12 to 15			V	
V _{OM}	Maximum peak output voltage swing R _L = 10 kΩ, T _A = 25°C	±10	±13.5	±10	±13.5			V	
		R _L ≥ 10 kΩ, T _A = Full range		±10					
A _{VD}	Large-signal differential voltage amplification V _O = ±10 V, R _L ≥ 2 kΩ	T _A = 25°C		3	6	4	6	V/mV	
		T _A = Full range		3		4			
B ₁	Unity-gain bandwidth R _L = 10 kΩ, T _A = 25°C	1			1			MHz	
r _i	Input resistance T _A = 25°C	10 ¹²			10 ¹²			Ω	
CMRR	Common-mode rejection ratio V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω, T _A = 25°C	70	86	80	86			dB	
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO}) V _{CC} = ±9 V to ±15 V, V _O = 0, R _S = 50 Ω, T _A = 25°C	70	95	80	95			dB	
P _D	Total power dissipation (each amplifier) V _O = 0, No load, T _A = 25°C	6		7.5	6		7.5	mW	
I _{CC}	Supply current (each amplifier) V _O = 0, No load, T _A = 25°C	200		250	200		250	μA	
V _{O1} /V _{O2}	Crosstalk attenuation A _{VD} = 100, T _A = 25°C	120			120			dB	

- (1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06xC, TL06xAC, and TL06xBC and –40°C to 85°C for TL06xI.
- (2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in [Figure 12](#). Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

6.8 Electrical Characteristics for TL06xxC and TL06xl

 $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	TL061BC, TL062BC, TL064BC			TL061I, TL062I, TL064I			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO}	Input offset voltage $V_O = 0, R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		2	3	$T_A = 25^\circ\text{C}$		mV	
		$T_A = \text{Full range}$		5		$T_A = \text{Full range}$			
α_{VIO}	Temperature coefficient of input offset voltage $V_O = 0, R_S = 50\ \Omega, T_A = \text{Full range}$	10			10			$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current $V_O = 0$	$T_A = 25^\circ\text{C}$		5	100	$T_A = 25^\circ\text{C}$		pA	
		$T_A = \text{Full range}$		3		$T_A = \text{Full range}$		nA	
I_{IB}	Input bias current ⁽²⁾ $V_O = 0$	$T_A = 25^\circ\text{C}$		30	200	$T_A = 25^\circ\text{C}$		pA	
		$T_A = \text{Full range}$		7		$T_A = \text{Full range}$		nA	
V_{ICR}	Common-mode input voltage range $T_A = 25^\circ\text{C}$	± 11	-12 to 15	± 11	-12 to 15			V	
V_{OM}	Maximum peak output voltage swing $R_L = 10\ \text{k}\Omega, T_A = 25^\circ\text{C}$	± 10	± 13.5	± 10	± 13.5			V	
	$R_L \geq 10\ \text{k}\Omega, T_A = \text{Full range}$	± 10		± 10					
A_{VD}	Large-signal differential voltage amplification $V_O = \pm 10\ \text{V}, R_L \geq 2\ \text{k}\Omega$	$T_A = 25^\circ\text{C}$		4	6	$T_A = 25^\circ\text{C}$		V/mV	
		$T_A = \text{Full range}$		4		$T_A = \text{Full range}$			
B_1	Unity-gain bandwidth $R_L = 10\ \text{k}\Omega, T_A = 25^\circ\text{C}$	1			1			MHz	
r_i	Input resistance $T_A = 25^\circ\text{C}$	10^{12}			10^{12}			Ω	
CMRR	Common-mode rejection ratio $V_{IC} = V_{ICRmin}, V_O = 0, R_S = 50\ \Omega, T_A = 25^\circ\text{C}$	80	86	80	86			dB	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$) $V_{CC} = \pm 9\ \text{V to } \pm 15\ \text{V}, V_O = 0, R_S = 50\ \Omega, T_A = 25^\circ\text{C}$	80	95	80	95			dB	
P_D	Total power dissipation (each amplifier) $V_O = 0, \text{No load}, T_A = 25^\circ\text{C}$	6		7.5		6		7.5	mW
I_{CC}	Supply current (each amplifier) $V_O = 0, \text{No load}, T_A = 25^\circ\text{C}$	200		250		200		250	μA
V_{O1}/V_{O2}	Crosstalk attenuation $A_{VD} = 100, T_A = 25^\circ\text{C}$	120			120			dB	

- (1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06xC, TL06xAC, and TL06xBC and -40°C to 85°C for TL06xl.
- (2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 12. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

6.9 Electrical Characteristics for TL06xM and TL064M

 $V_{CC\pm} = \pm 15\ \text{V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	TL061M, TL062M			TL064M			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage $V_O = 0, R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		3	6	$T_A = 25^\circ\text{C}$		mV
		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		9		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		
α_{VIO}	Temperature coefficient of input offset voltage $V_O = 0, R_S = 50\ \Omega, T_A = -55^\circ\text{C to } 125^\circ\text{C}$	10			10			$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current $V_O = 0$	$T_A = 25^\circ\text{C}$		5	100	$T_A = 25^\circ\text{C}$		pA
		$T_A = -55^\circ\text{C}$		20 ⁽²⁾		$T_A = -55^\circ\text{C}$		20 ⁽²⁾
		$T_A = 125^\circ\text{C}$		20		$T_A = 125^\circ\text{C}$		20
I_{IB}	Input bias current ⁽³⁾ $V_O = 0$	$T_A = 25^\circ\text{C}$		30	200	$T_A = 25^\circ\text{C}$		pA
		$T_A = -55^\circ\text{C}$		50 ⁽²⁾		$T_A = -55^\circ\text{C}$		50 ⁽²⁾
		$T_A = 125^\circ\text{C}$		50		$T_A = 125^\circ\text{C}$		50
V_{ICR}	Common-mode input voltage range $T_A = 25^\circ\text{C}$	± 11	-12 to 15	± 11	-12 to 15			V

- (1) All characteristics are measured under open-loop conditions, with zero common-mode voltage, unless otherwise specified.
- (2) This parameter is not production tested.
- (3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 12. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

Electrical Characteristics for TL06xM and TL064M (continued)

$V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	TL061M, TL062M			TL064M			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
V_{OM}	Maximum peak output voltage swing	$R_L = 10\text{ k}\Omega, T_A = 25^\circ\text{C}$			± 10	± 13.5		V	
		$R_L \geq 10\text{ k}\Omega, T_A = -55^\circ\text{C to } 125^\circ\text{C}$			± 10				
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}, R_L \geq 2\text{ k}\Omega$	$T_A = 25^\circ\text{C}$		4	6	4	6	V/mV
			$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		4		4		
B_1	Unity-gain bandwidth	$R_L = 10\text{ k}\Omega, T_A = 25^\circ\text{C}$						MHz	
r_i	Input resistance	$T_A = 25^\circ\text{C}$				10^{12}	10^{12}	Ω	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, V_O = 0, R_S = 50\ \Omega, T_A = 25^\circ\text{C}$			80	86	80	86	dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9\text{ V to } \pm 15\text{ V}, V_O = 0, R_S = 50\ \Omega, T_A = 25^\circ\text{C}$			80	95	80	95	dB
P_D	Total power dissipation (each amplifier)	$V_O = 0, \text{No load}, T_A = 25^\circ\text{C}$			6	7.5	6	7.5	mW
I_{CC}	Supply current (each amplifier)	$V_O = 0, \text{No load}, T_A = 25^\circ\text{C}$			200	250	200	250	μA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100, T_A = 25^\circ\text{C}$			120		120		dB

6.10 Operating Characteristics

$V_{CC\pm} = \pm 15\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
SR	Slew rate at unity gain ⁽¹⁾	$V_I = 10\text{ V}, R_L = 10\text{ k}\Omega,$	$C_L = 100\text{ pF},$ see Figure 16	1.5	3.5	V/ μs
t_r	Rise-time	$V_I = 20\text{ V}, R_L = 10\text{ k}\Omega,$	$C_L = 100\text{ pF},$ see Figure 16	0.2		μs
	Overshoot factor			10%		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 1\text{ kHz}$	42		nV/ $\sqrt{\text{Hz}}$

(1) Slew rate at $-55^\circ\text{C to } 125^\circ\text{C}$ is 0.7 V/ μs min.

6.11 Typical Characteristics

Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

Table 1. Table of Graphs

	FIGURE
Maximum peak output voltage versus Supply voltage	Figure 1
Maximum peak output voltage versus Free-air temperature	Figure 2
Maximum peak output voltage versus Load resistance	Figure 3
Maximum peak output voltage versus Frequency	Figure 4
Differential voltage amplification versus Free-air temperature	Figure 5
Large-signal differential voltage amplification versus Frequency	Figure 6
Phase shift versus Frequency	Figure 6
Supply current versus Supply voltage	Figure 7
Supply current versus Free-air temperature	Figure 8
Total power dissipation versus Free-air temperature	Figure 9
Common-mode rejection ratio versus Free-air temperature	Figure 10
Normalized unity-gain bandwidth versus Free-air temperature	Figure 11
Normalized slew rate versus Free-air temperature	Figure 11
Normalized phase shift versus Free-air temperature	Figure 11
Input bias current versus Free-air temperature	Figure 12
Voltage-follower large-signal pulse response versus Time	Figure 13
Output voltage versus Elapsed time	Figure 14
Equivalent input noise voltage versus Frequency	Figure 15

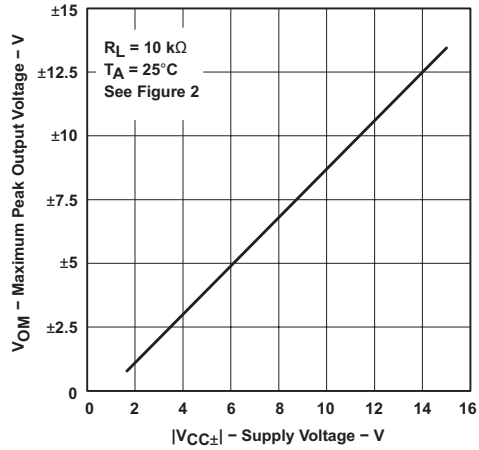


Figure 1. Maximum Peak Output Voltage vs Supply Voltage

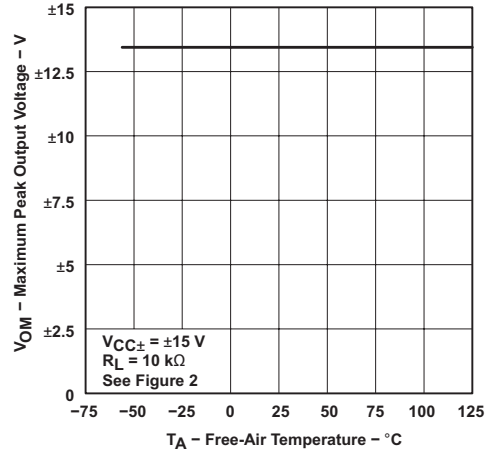


Figure 2. Maximum Peak Output Voltage vs Free-Air Temperature

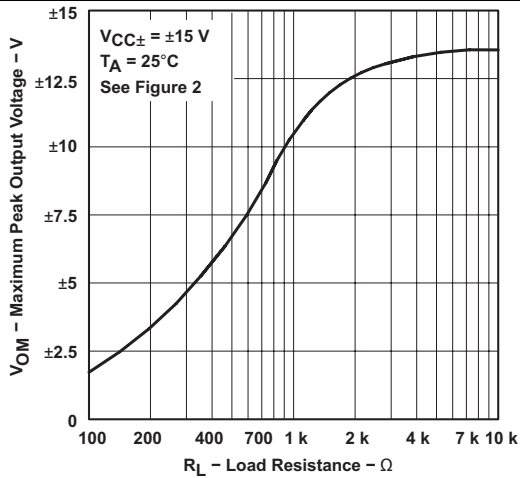


Figure 3. Maximum Peak Output Voltage vs Load Resistance

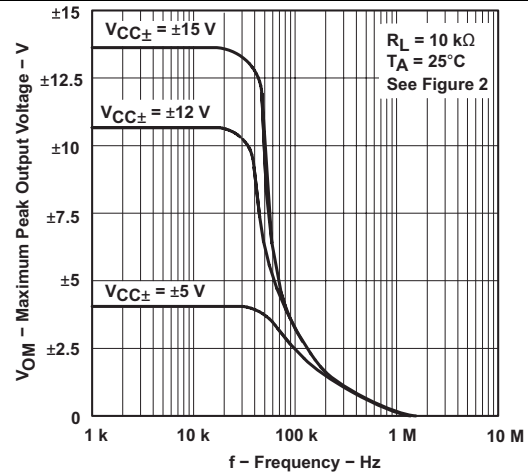


Figure 4. Maximum Peak Output Voltage vs Frequency

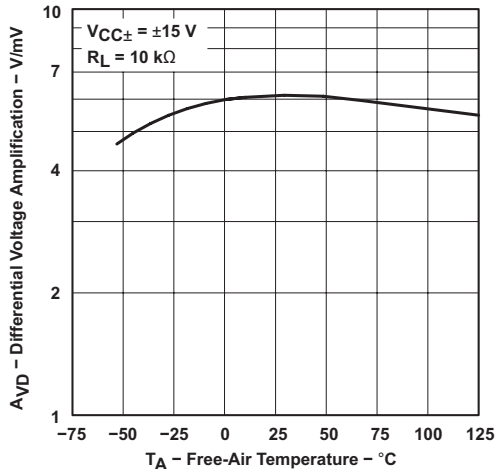


Figure 5. Differential Voltage Amplification vs Free-Air Temperature

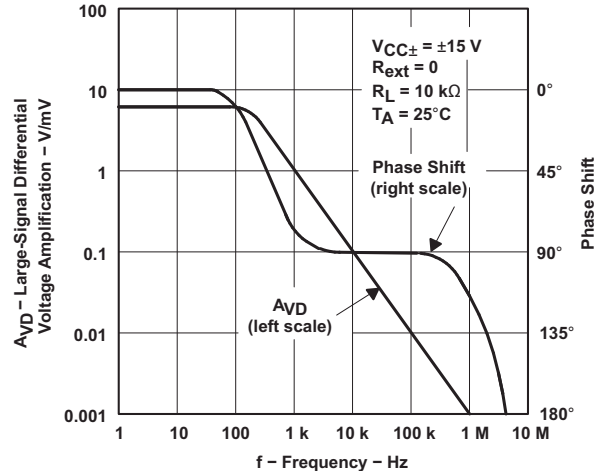


Figure 6. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

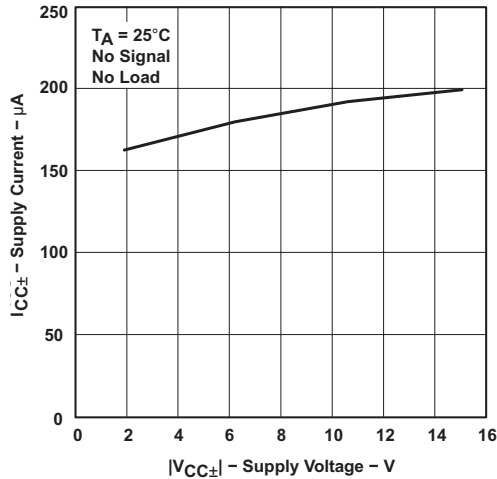


Figure 7. Supply Current vs Supply Voltage

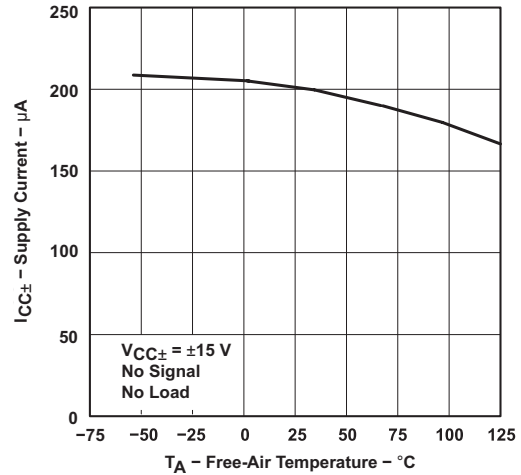


Figure 8. Supply Current vs Free-Air Temperature

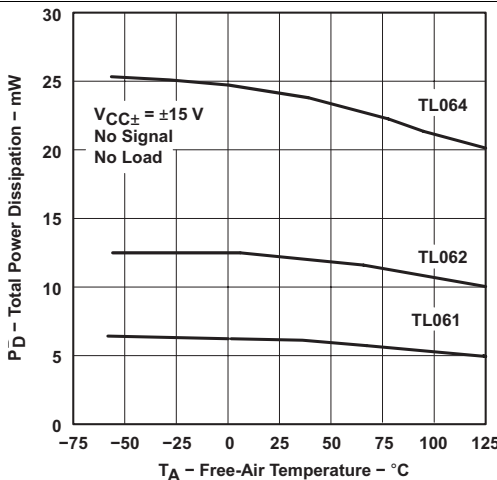


Figure 9. Total Power Dissipation vs Free-Air Temperature

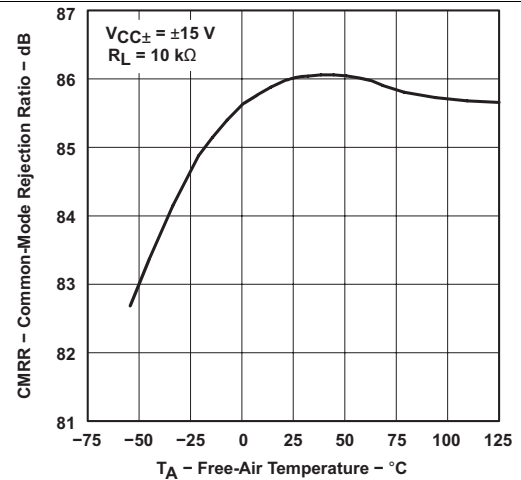


Figure 10. All Except TL06_C Common-Mode Rejection Ratio vs Free-Air Temperature

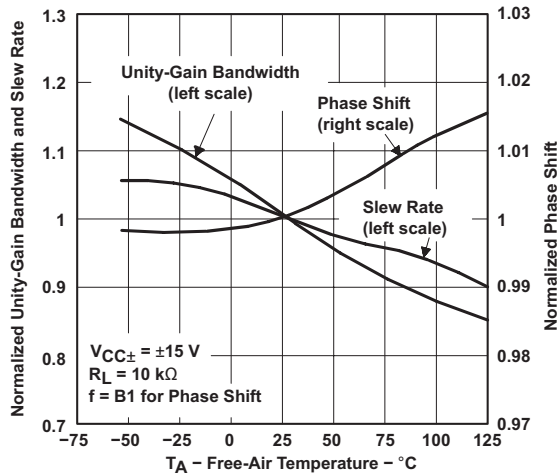


Figure 11. Normalized Unity-Gain Bandwidth, Slew Rate, and Phase Shift vs Free-Air Temperature

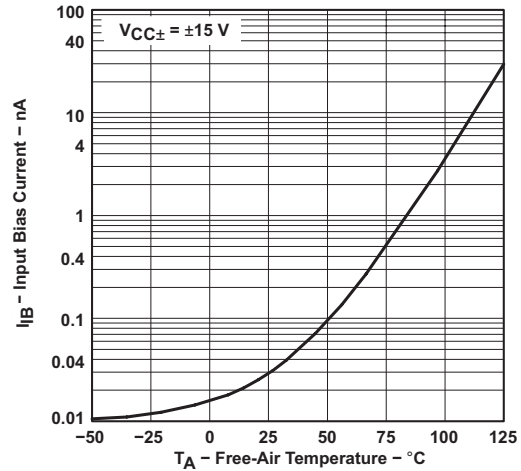


Figure 12. Input Bias Current vs Free-Air Temperature

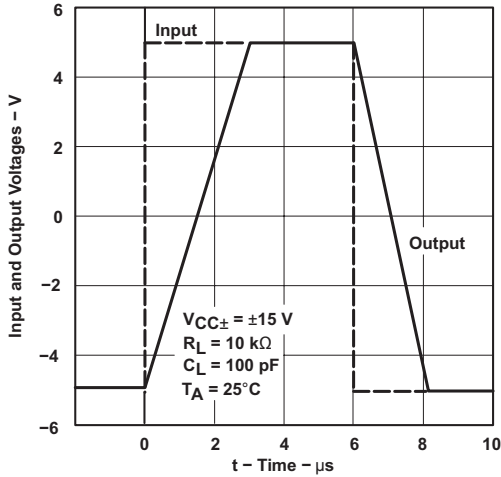


Figure 13. Voltage-Follower Large-Signal Pulse Response vs Time

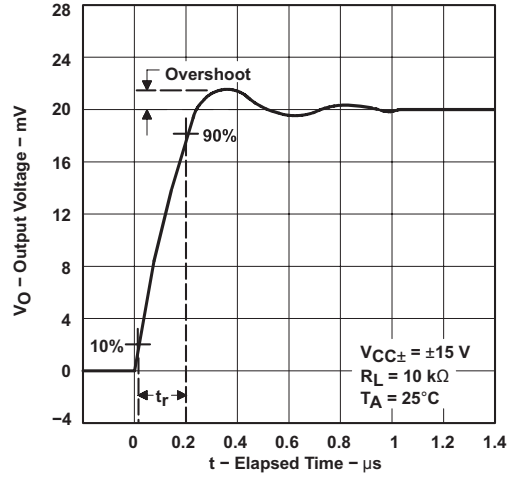


Figure 14. Output Voltage vs Elapsed Time

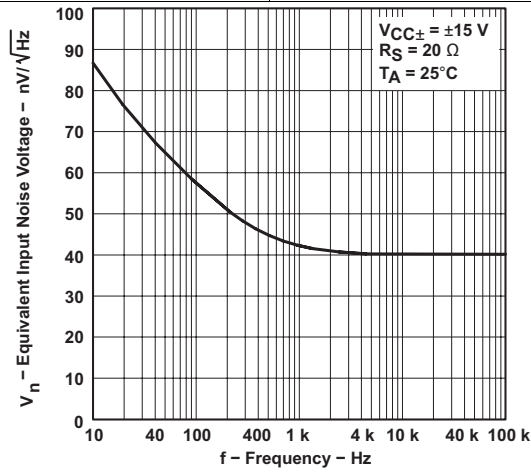


Figure 15. Equivalent Input Noise Voltage vs Frequency

7 Parameter Measurement Information

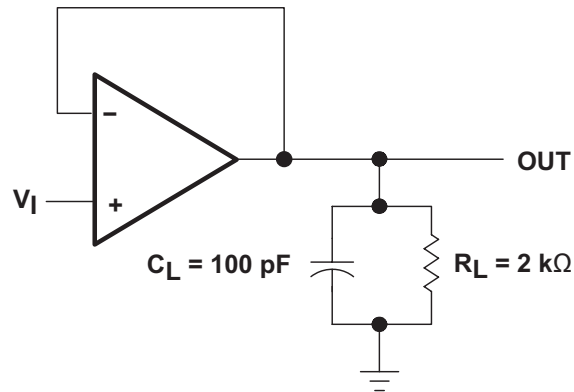


Figure 16. Unity-Gain Amplifier

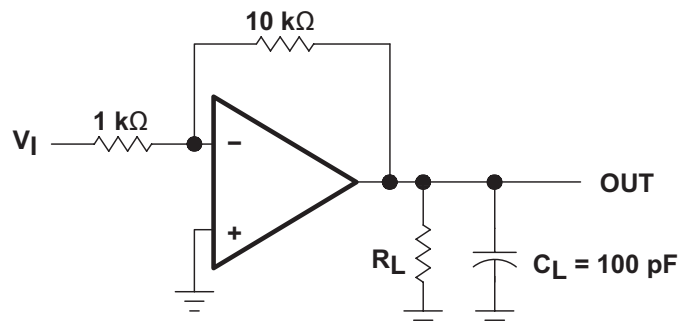


Figure 17. Gain-of-10 Inverting Amplifier

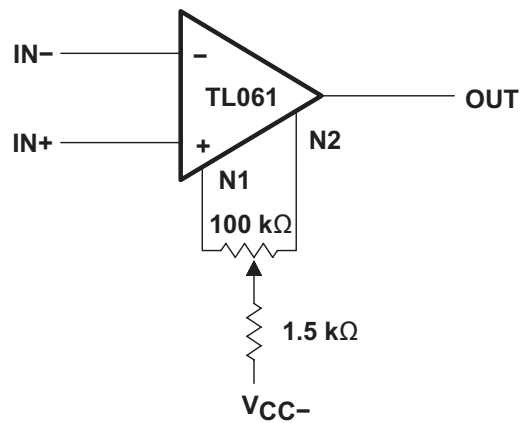


Figure 18. Input Offset-Voltage Null Circuit

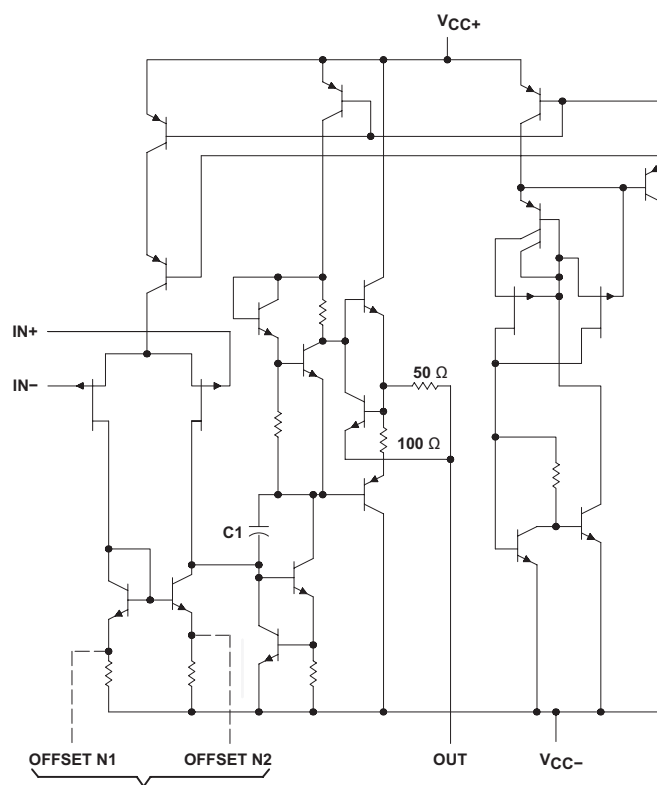
8 Detailed Description

8.1 Overview

The JFET-input operational amplifiers of the TL06x series are designed as low-power versions of the TL08x series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and input bias currents. The TL06x series features the same terminal assignments as the TL07x and TL08x series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in an integrated circuit.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C, and the M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

8.2 Functional Block Diagram



TL061 Only
 C1 = 10 pF on TL061, TL062, and TL064
 Component values shown are nominal.

8.3 Feature Description

8.3.1 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage and converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of this device is 86 dB.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 3.5-V/ μ s slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TL06x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

9.2 Typical Applications

9.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

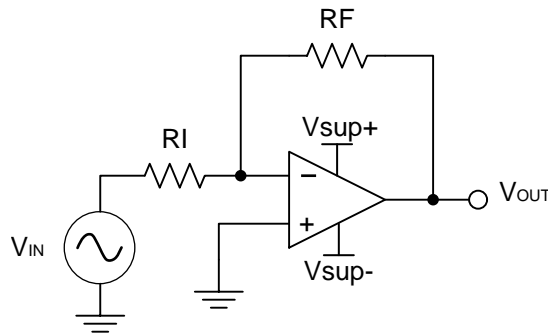


Figure 19. Schematic for Inverting Amplifier Application

9.2.1.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ± 0.5 V to ± 1.8 V. Setting the supply at ± 12 V is sufficient to accommodate this application.

9.2.1.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_v = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for R_I or R_F . Choosing a value in the kilohm range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 k Ω for R_I which means 36 k Ω will be used for R_F . This was determined by Equation 3.

$$A_v = -\frac{R_F}{R_I} \quad (3)$$

Typical Applications (continued)

9.2.1.3 Application Curve

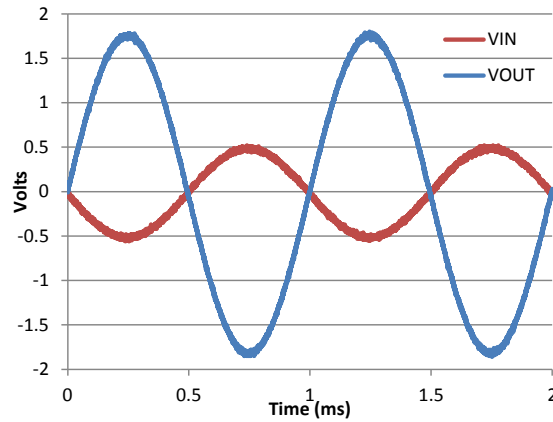


Figure 20. Input and Output Voltages of the Inverting Amplifier

9.3 System Examples

9.3.1 General Applications

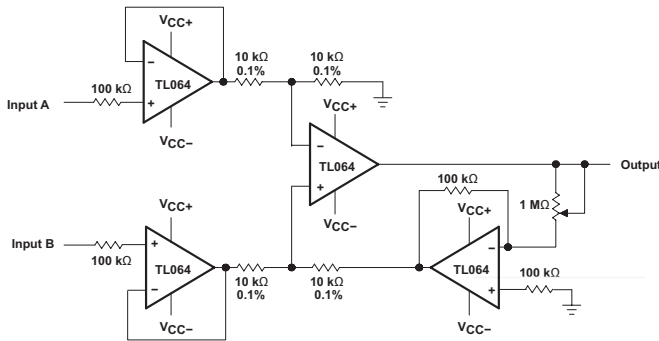


Figure 21. Instrumentation Amplifier

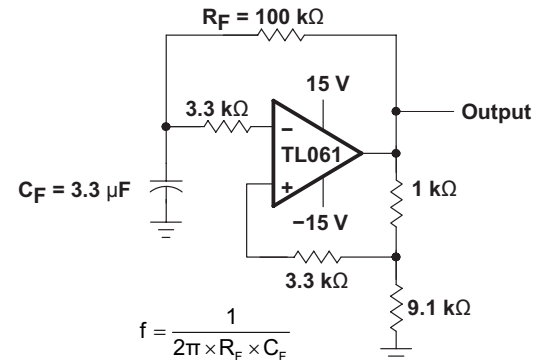


Figure 22. 0.5-Hz Square-Wave Oscillator

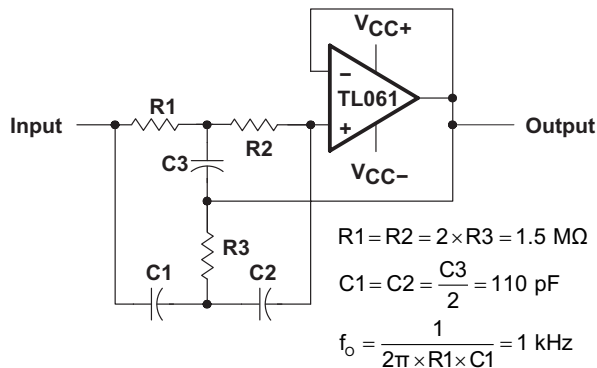


Figure 23. High-Q Notch Filter

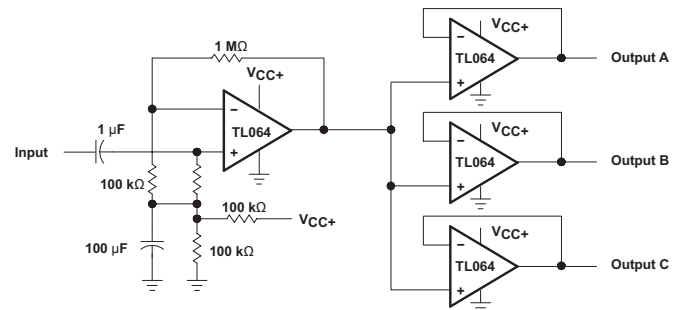


Figure 24. Audio-Distribution Amplifier

System Examples (continued)

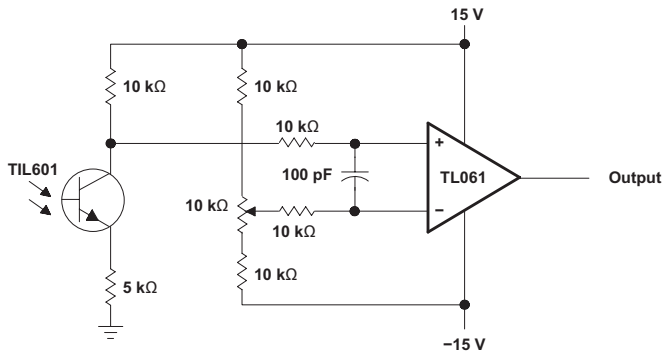


Figure 25. Low-Level Light Detector Preamplifier

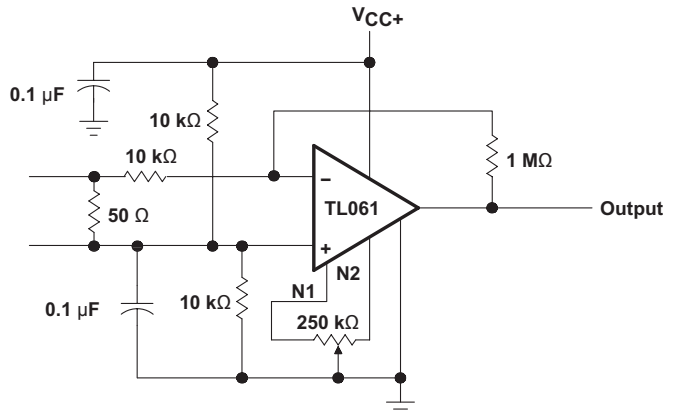


Figure 26. AC Amplifier

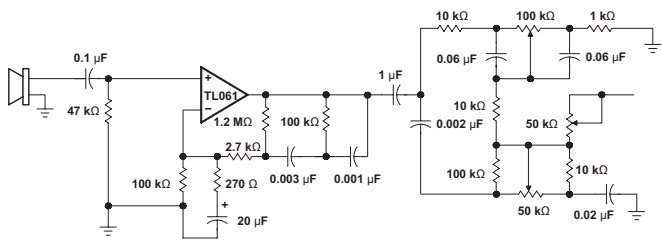


Figure 27. Microphone Preamplifier With Tone Control

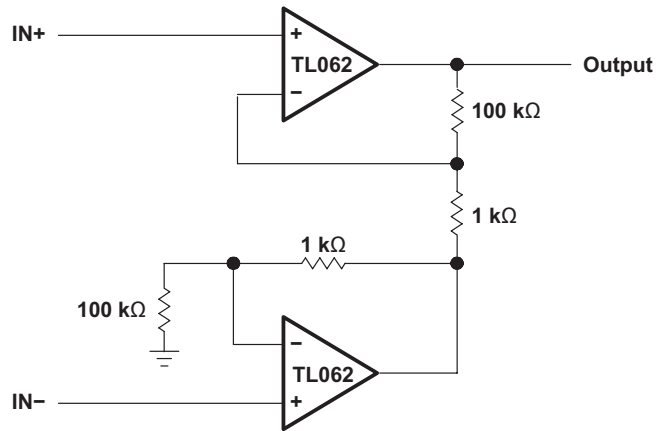


Figure 28. Instrumentation Amplifier

System Examples (continued)

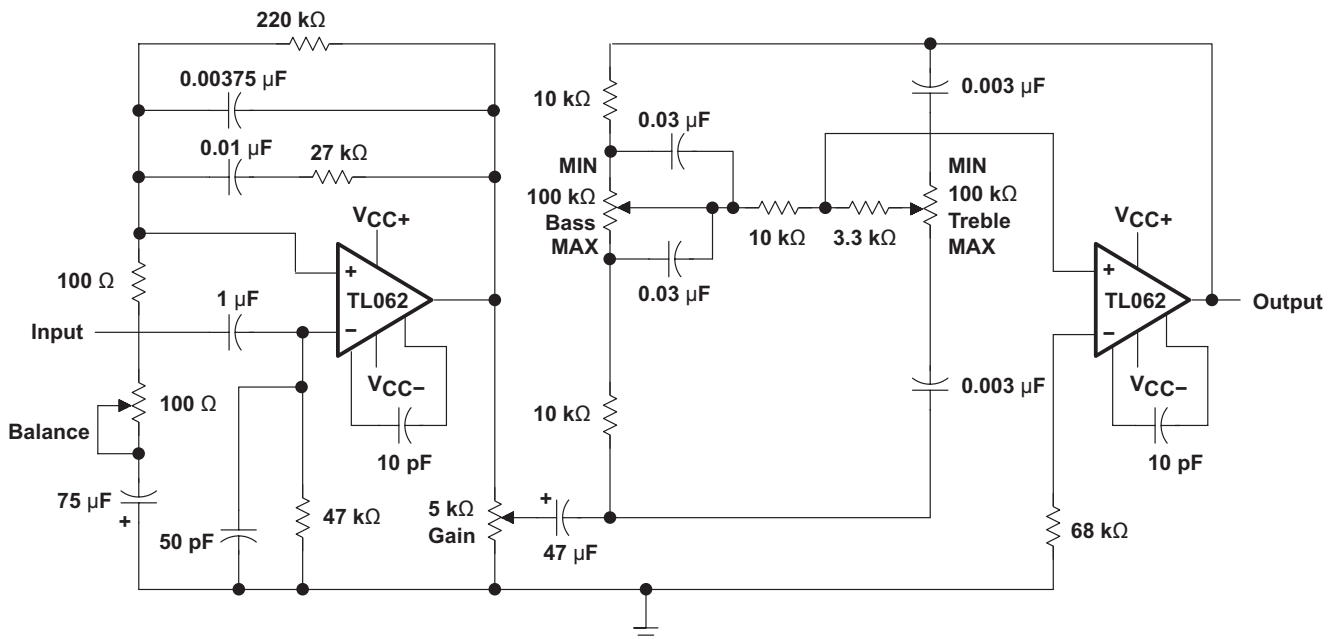
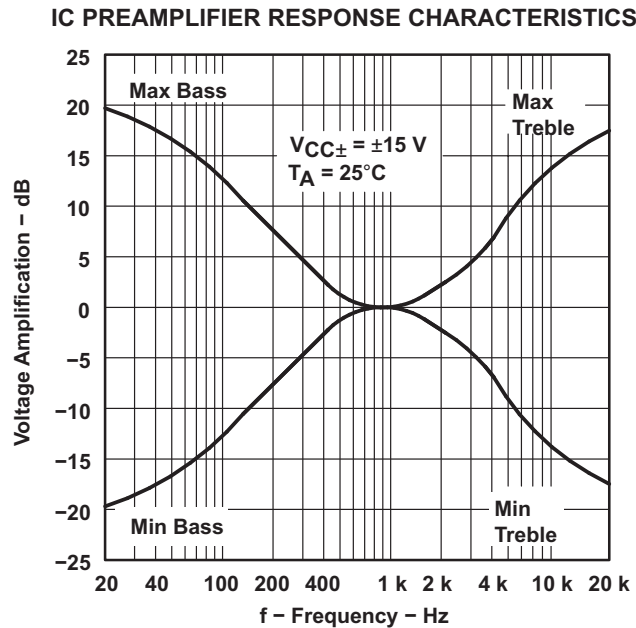


Figure 29. IC Preamplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single supply, or outside the range of ± 18 V for a dual supply can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#).

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Examples*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

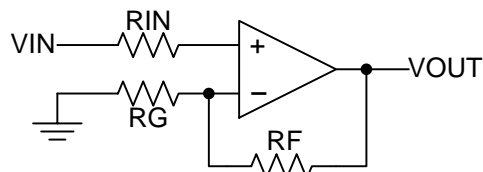


Figure 30. Operational Amplifier Schematic for Noninverting Configuration

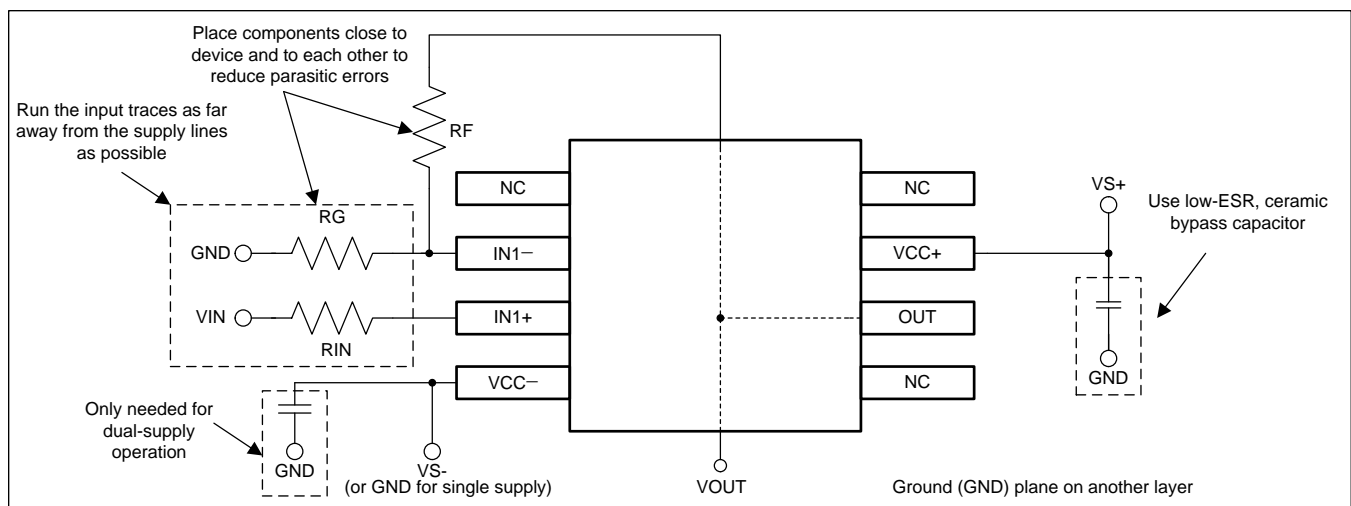
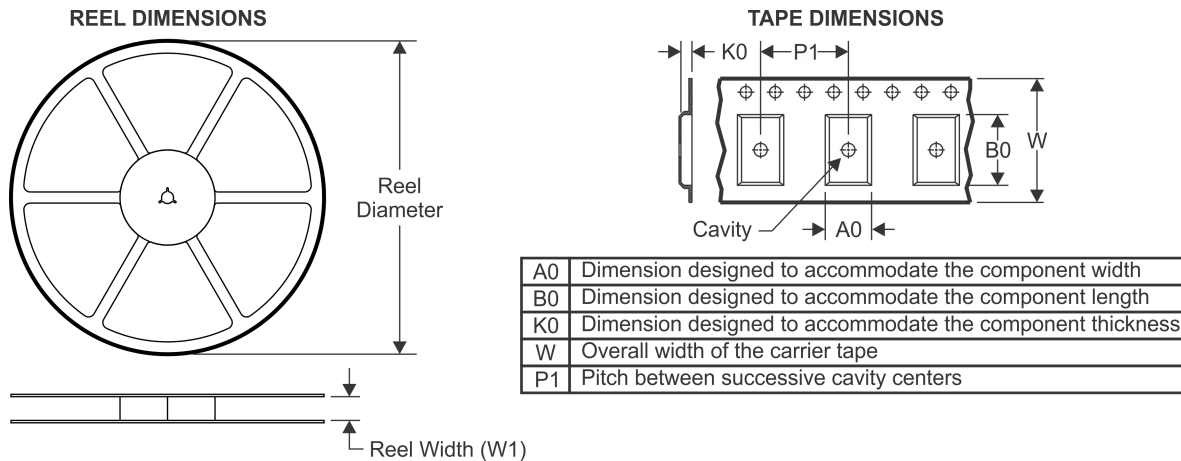
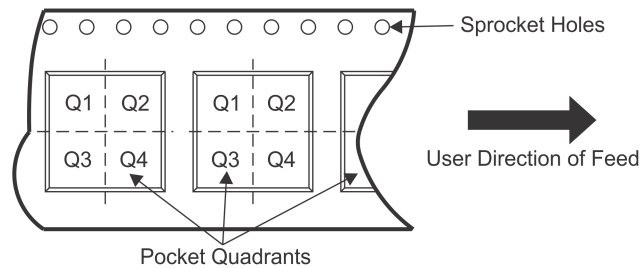


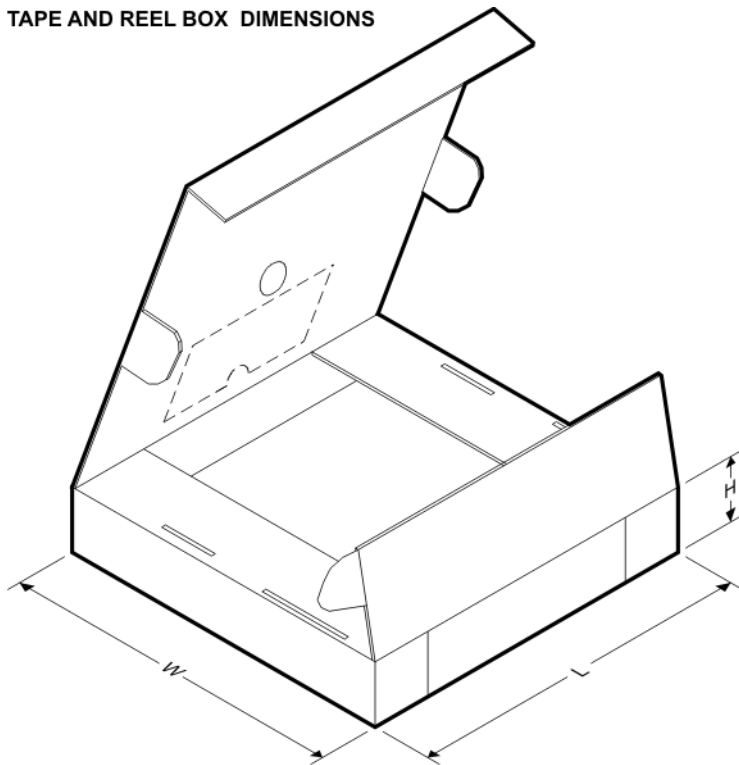
Figure 31. Operational Amplifier Board Layout for Noninverting Configuration

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL061ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL061IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL061IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL062BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL062CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL062CPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL062IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL064ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL064BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL064IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL064INSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL064IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


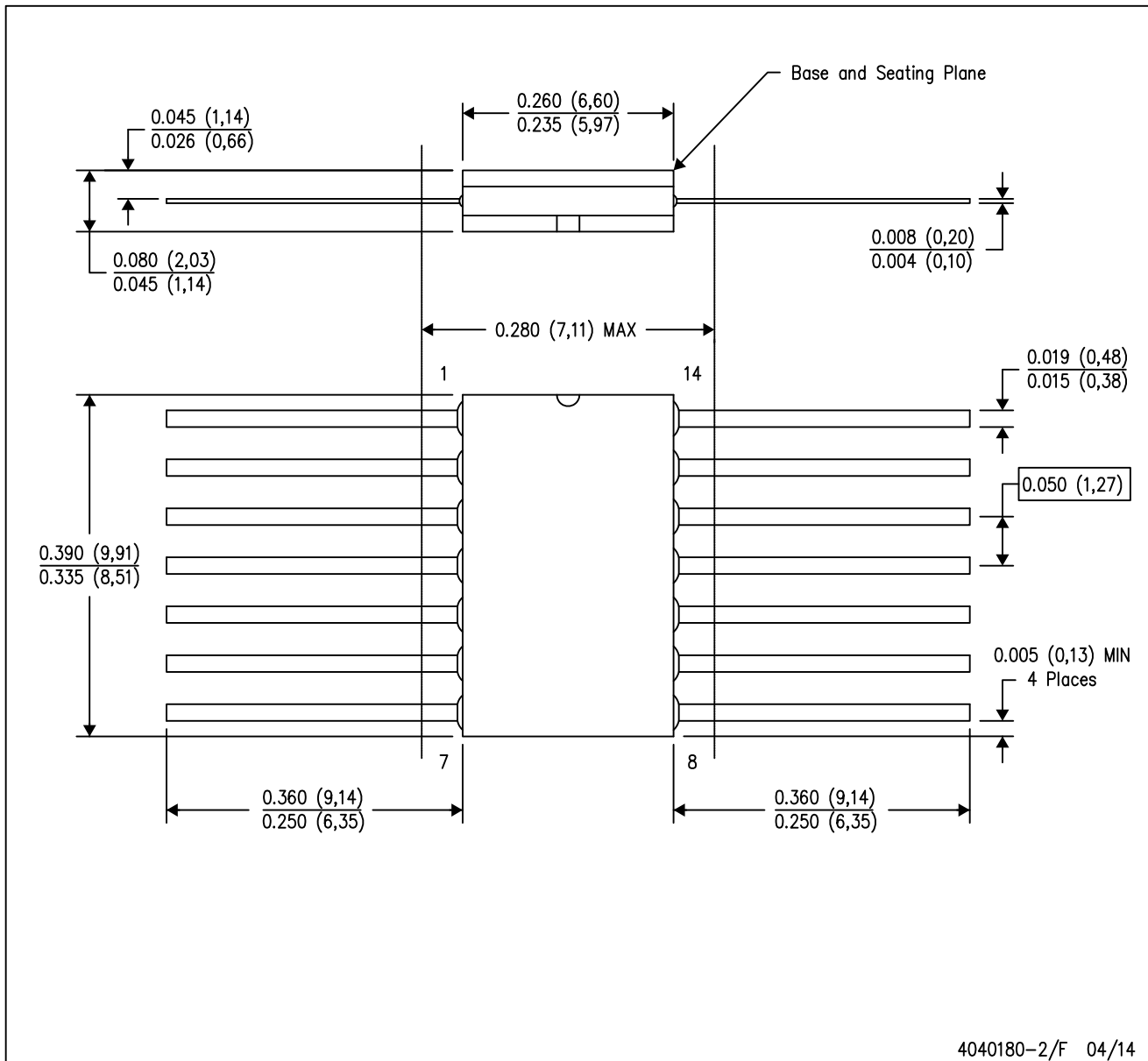
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL061ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL061CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL061CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL061CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL061IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL061IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062ACPSR	SO	PS	8	2000	367.0	367.0	38.0
TL062BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL062CDR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL062CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL062CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL062CPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
TL062IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL062IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL062IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL064ACDR	SOIC	D	14	2500	367.0	367.0	38.0
TL064BCDR	SOIC	D	14	2500	367.0	367.0	38.0
TL064CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL064IDR	SOIC	D	14	2500	367.0	367.0	38.0
TL064IDRG4	SOIC	D	14	2500	367.0	367.0	38.0
TL064INSR	SO	NS	14	2000	367.0	367.0	38.0
TL064IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

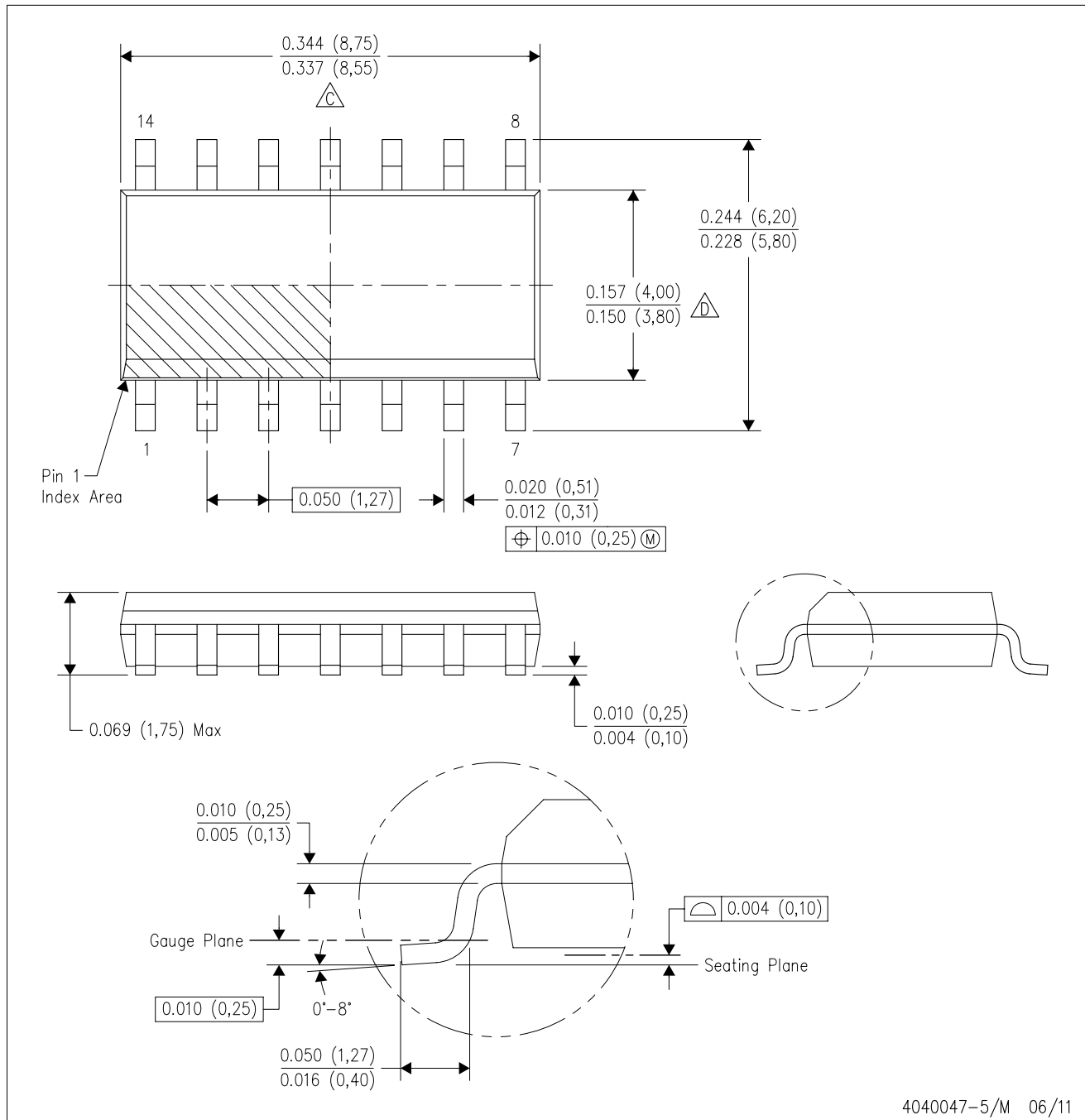


LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



D (R-PDSO-G14)

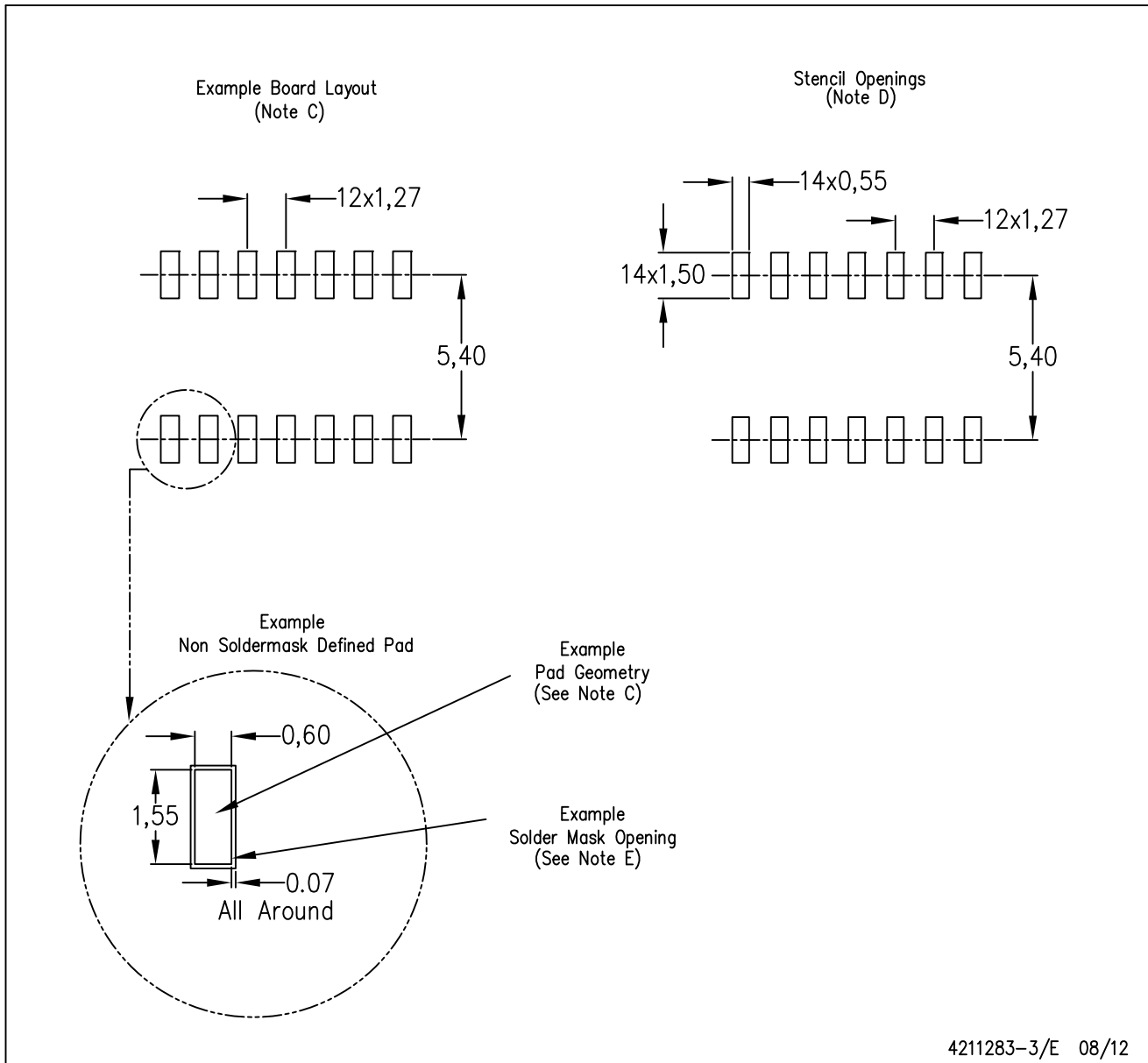
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

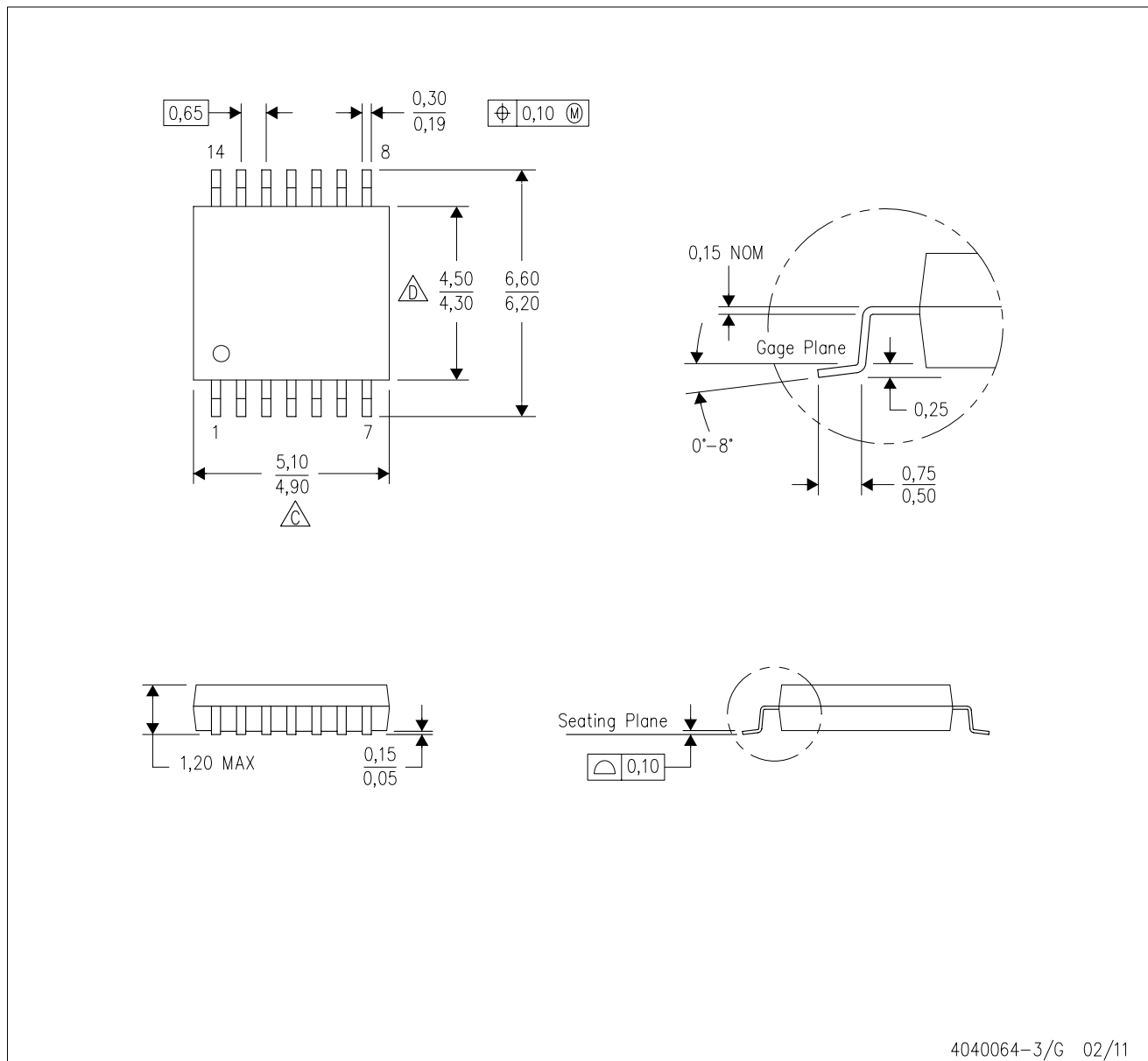




- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G14)

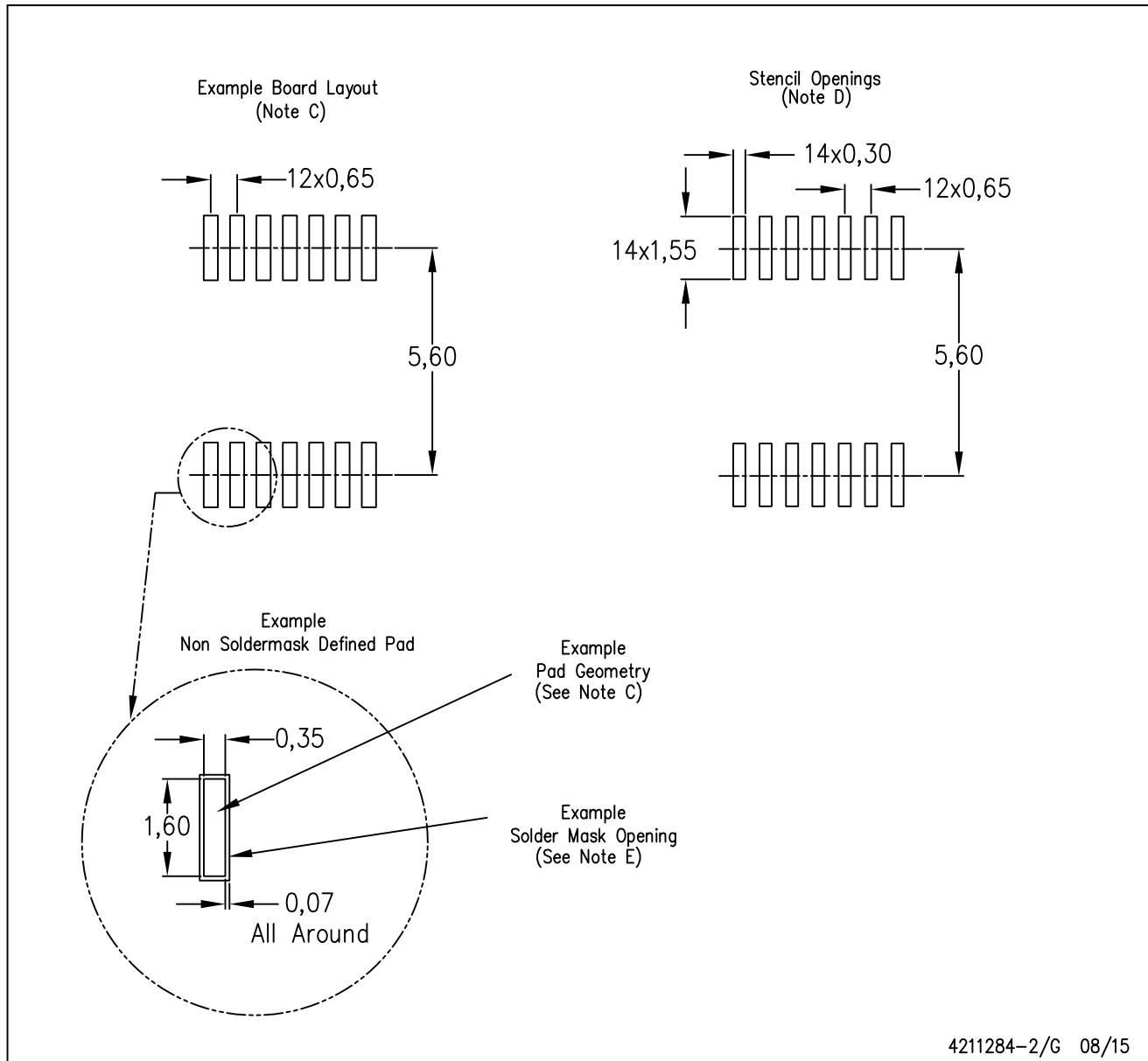
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

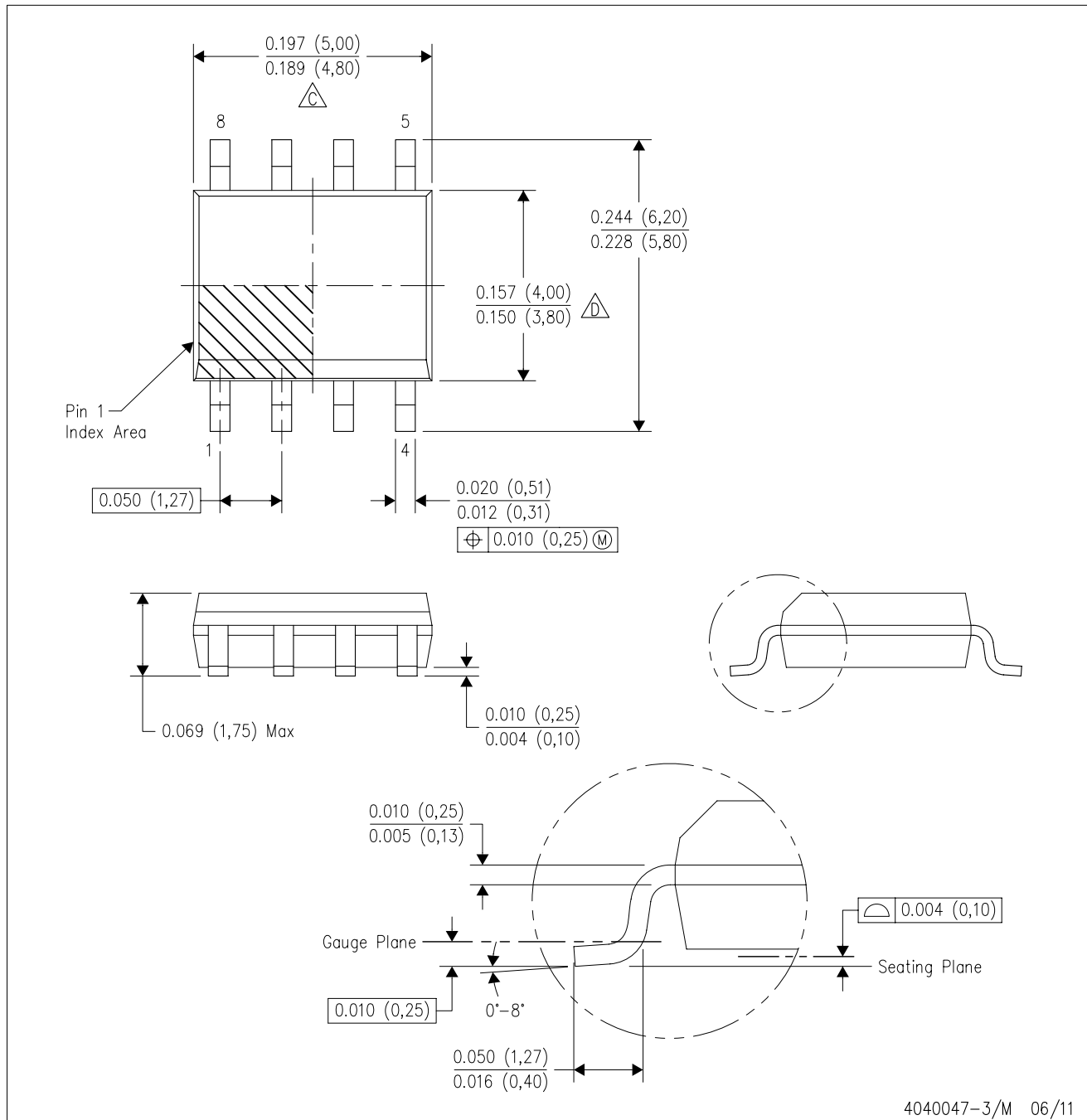


4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

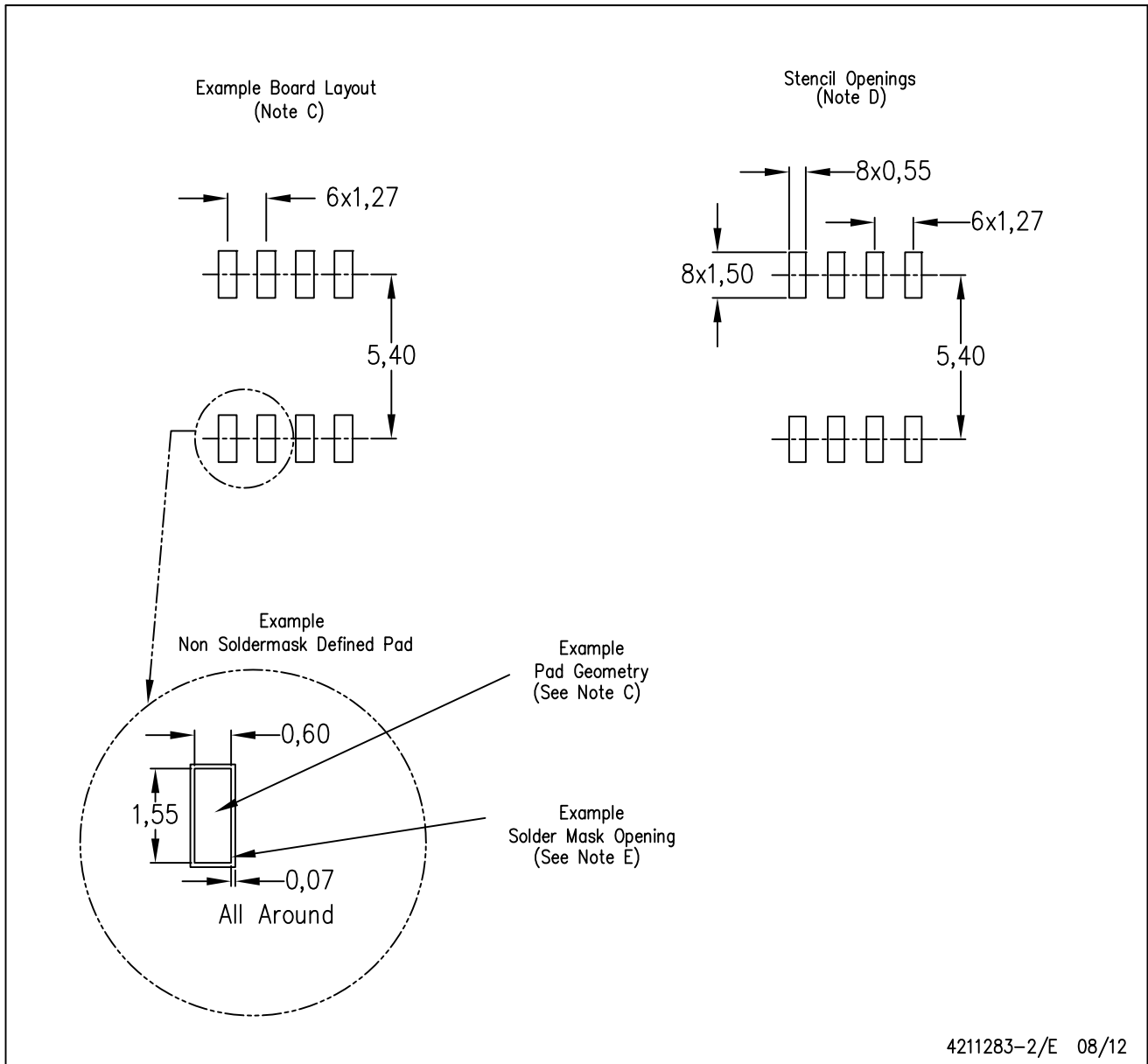
PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

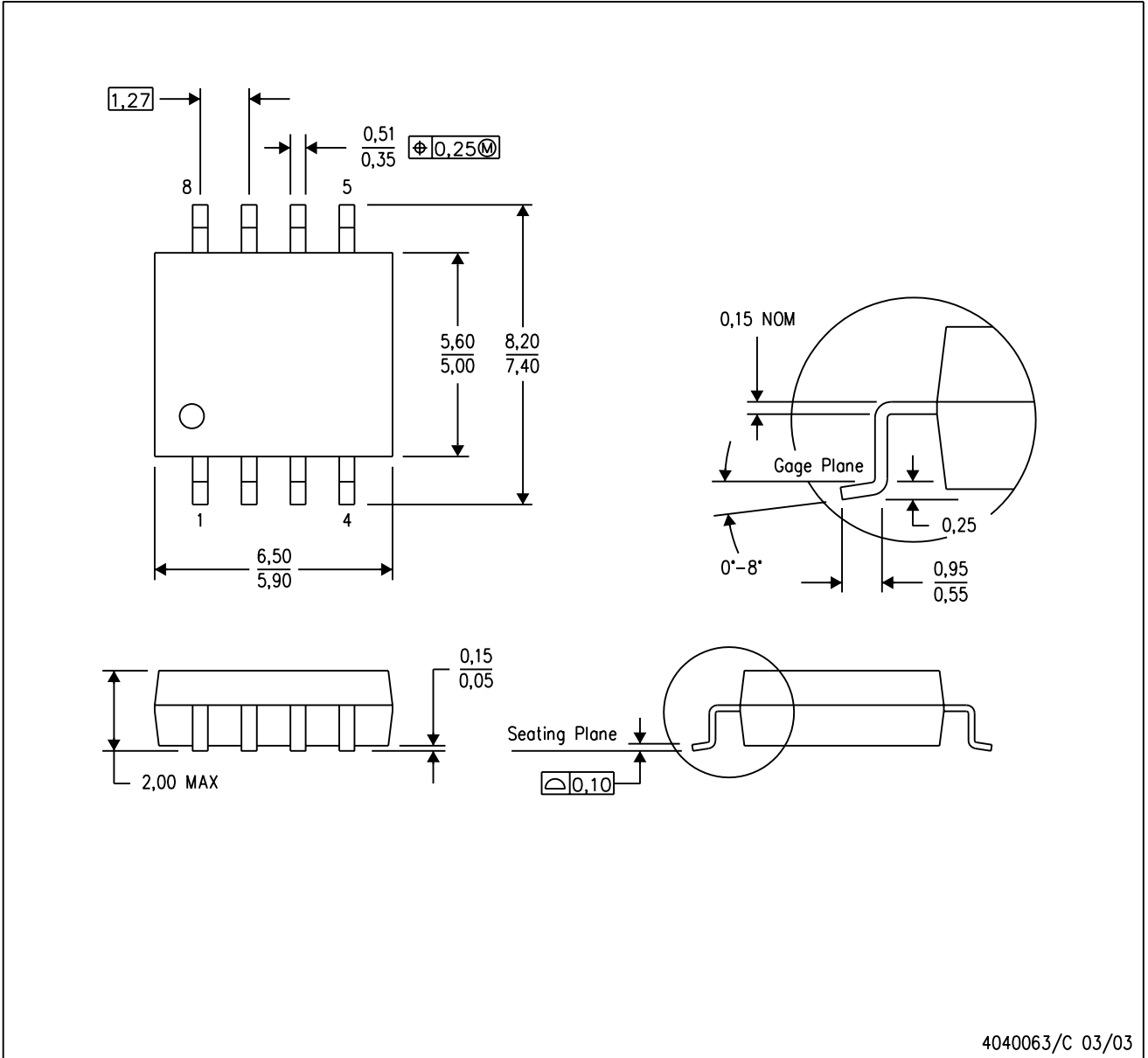


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8)

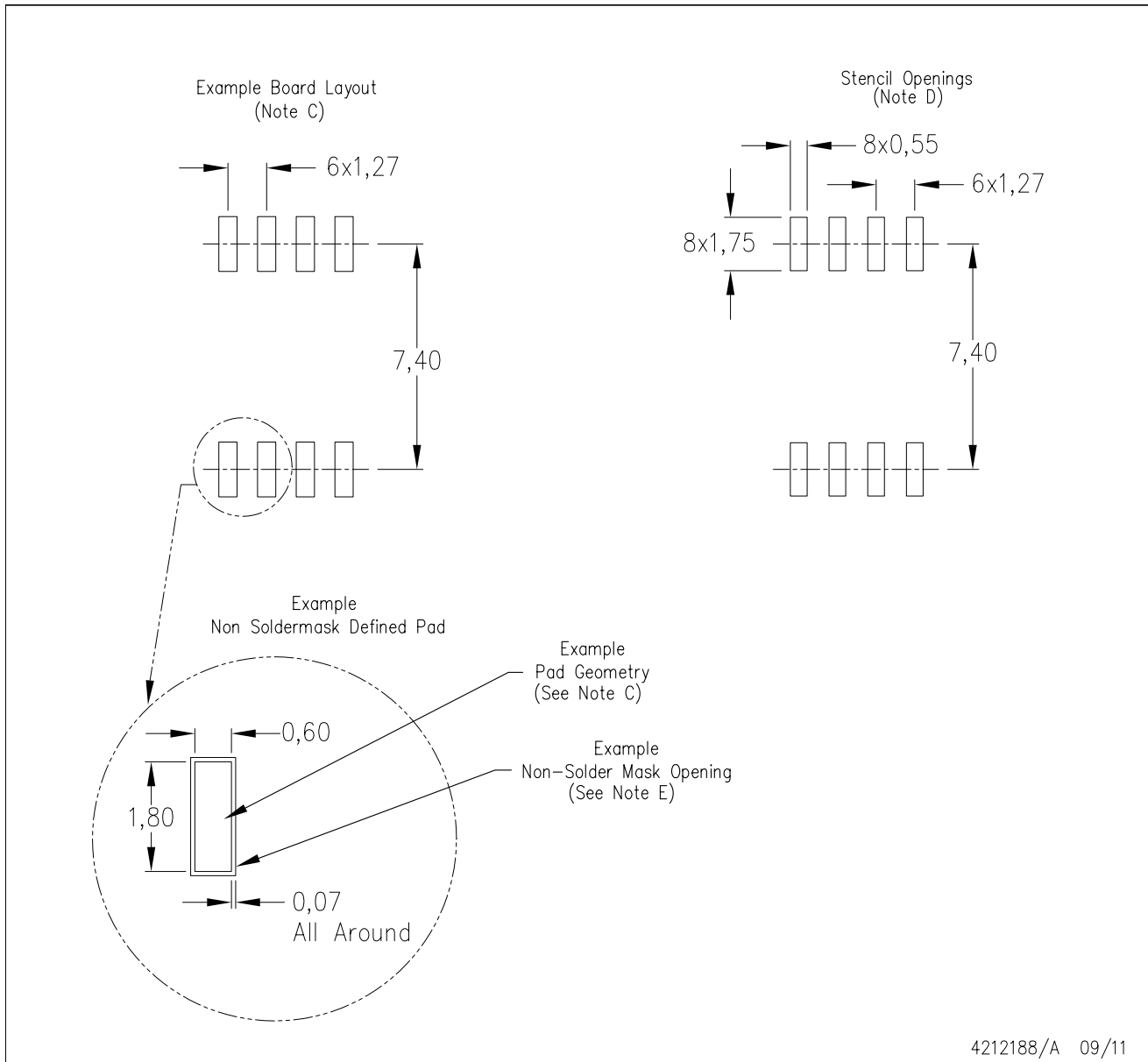
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

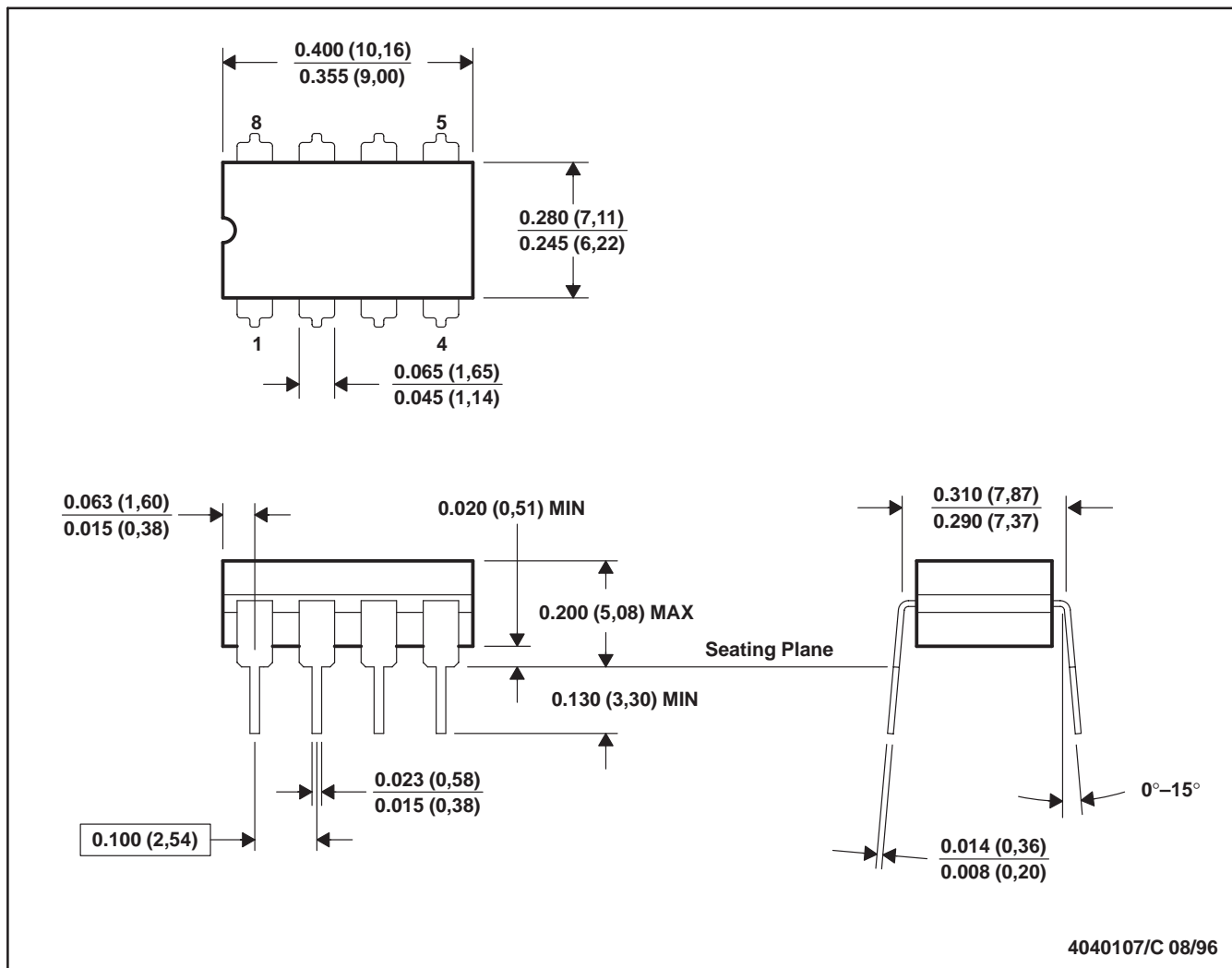
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

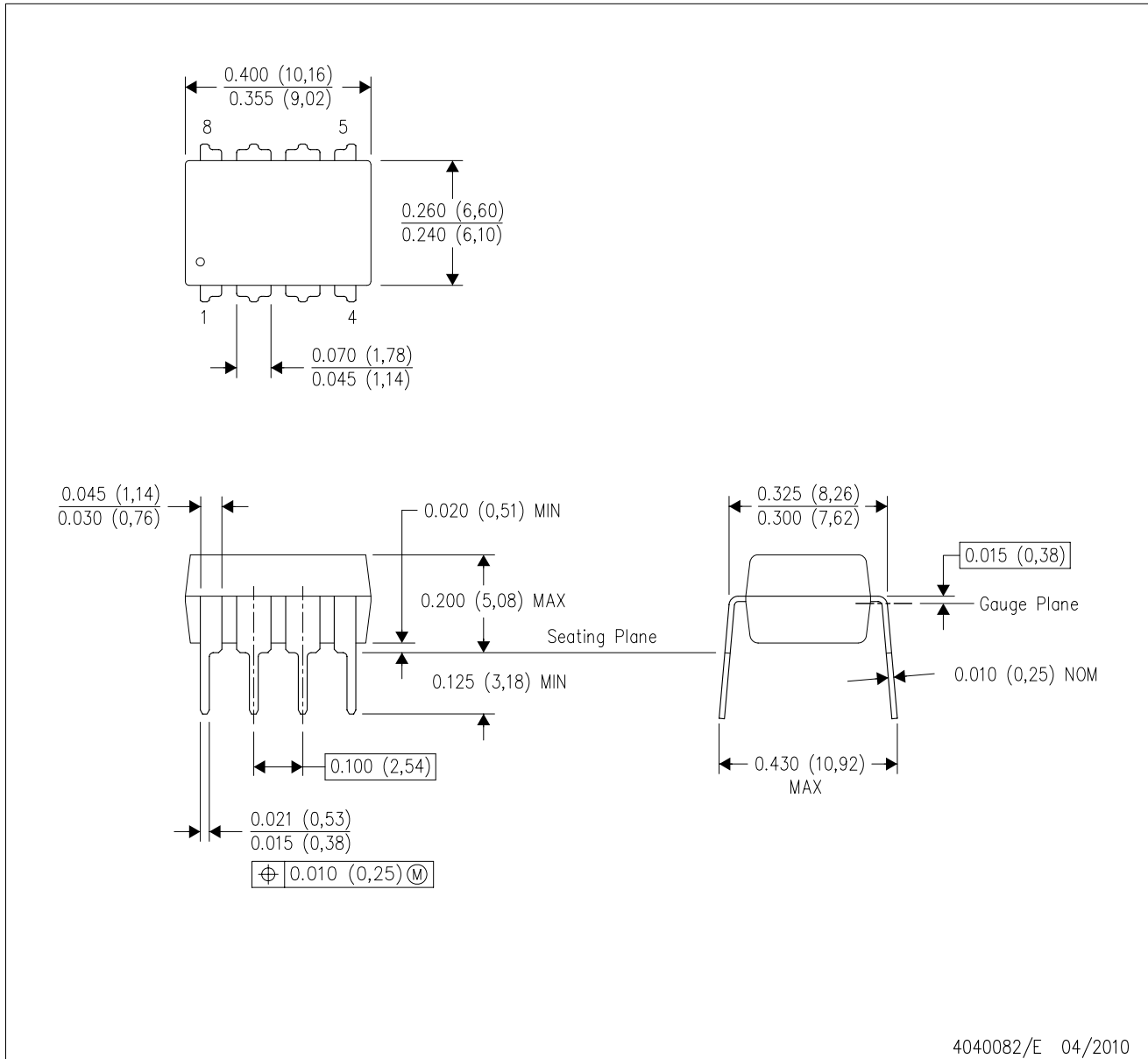


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



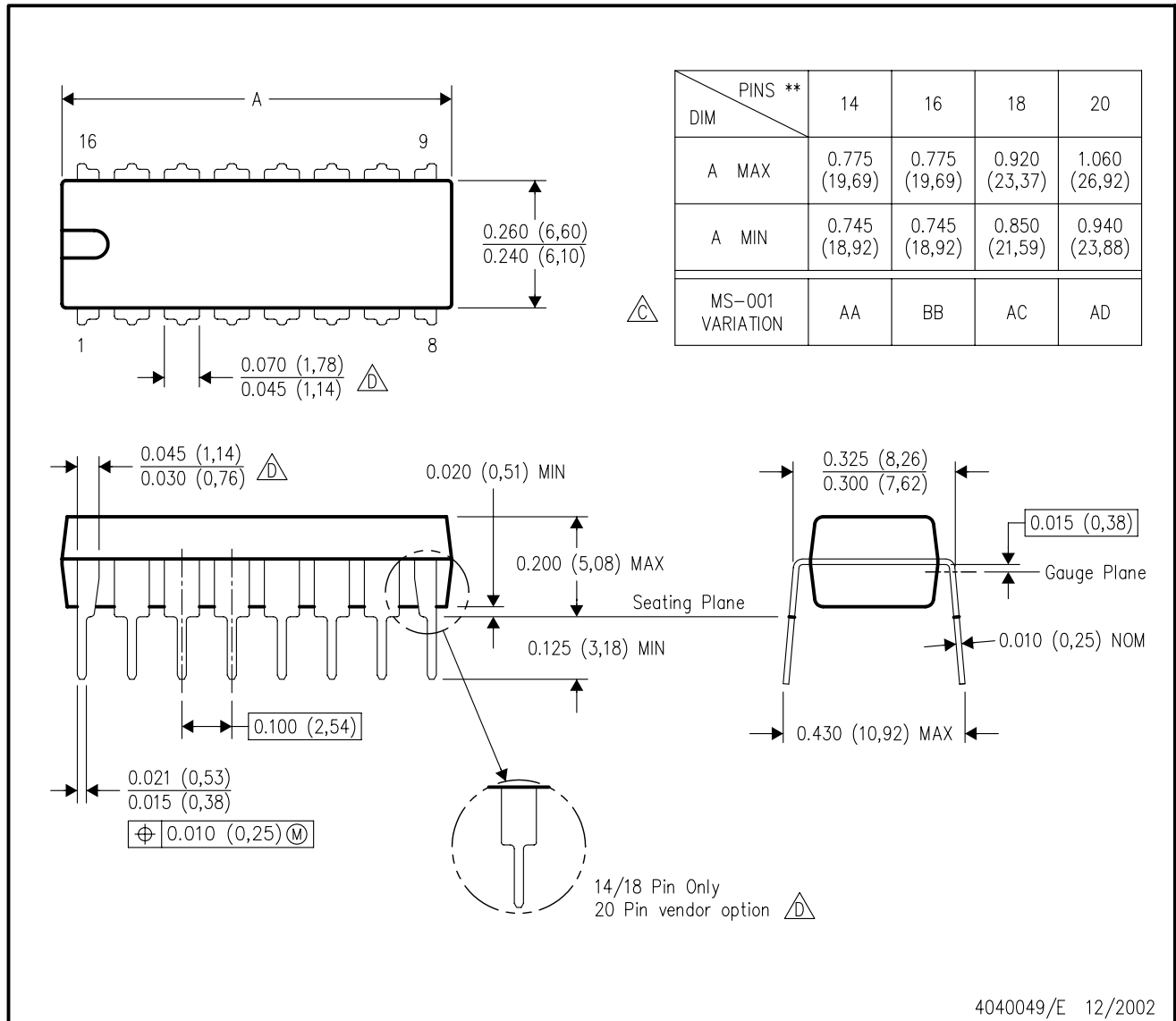
4040082/E 04/2010

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

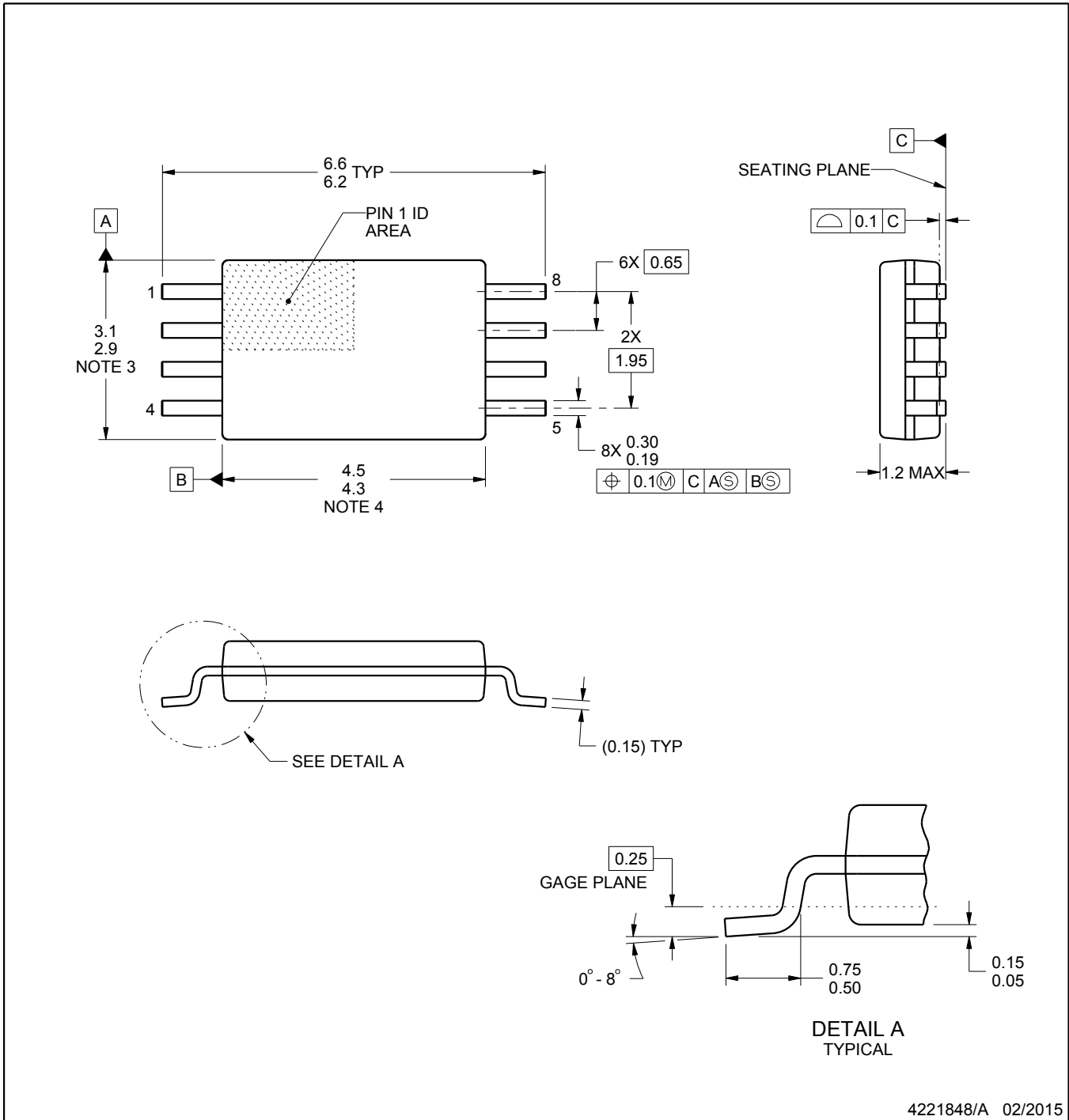
4040049/E 12/2002

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

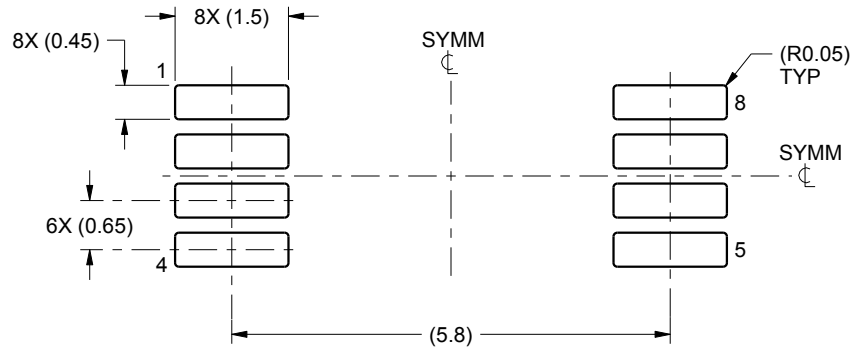
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

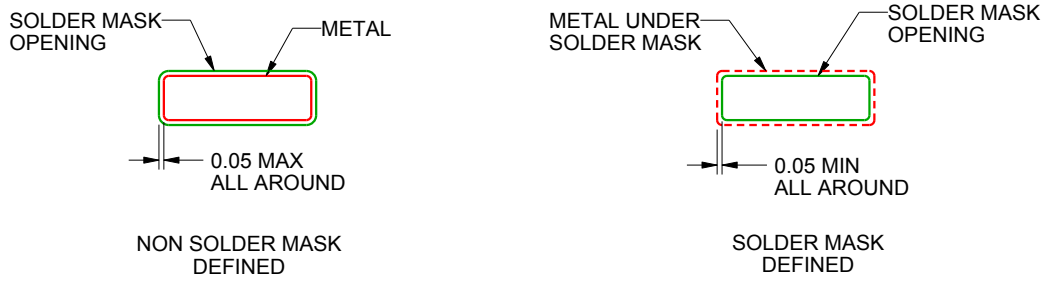
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

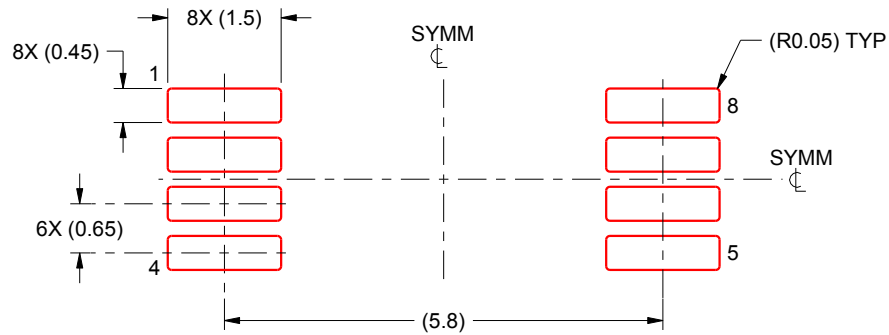
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

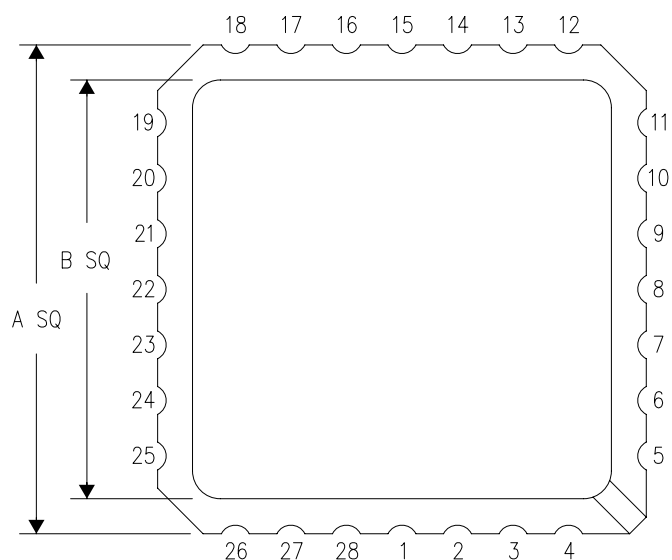
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

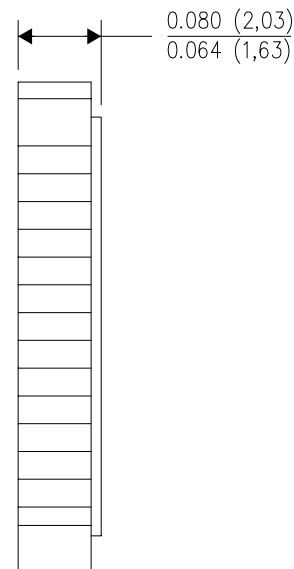
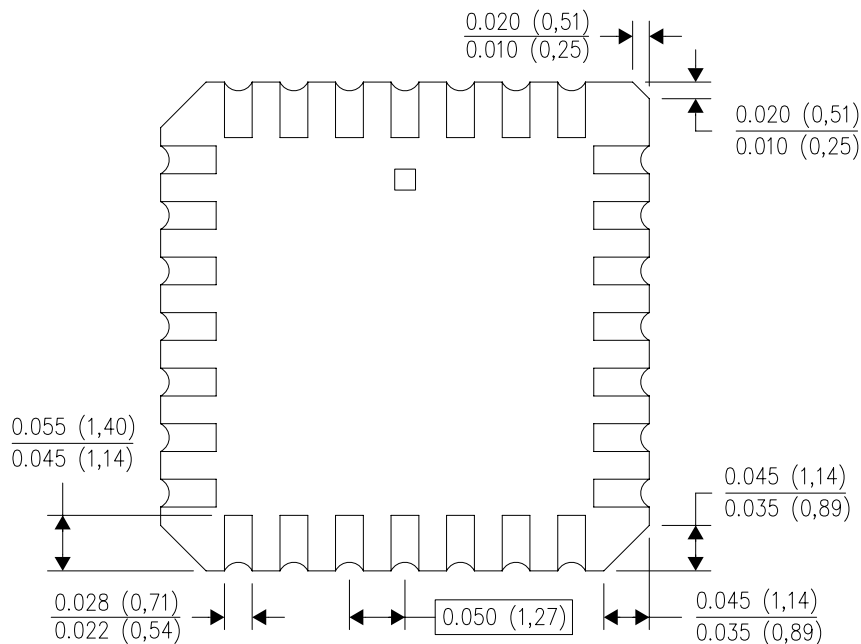
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

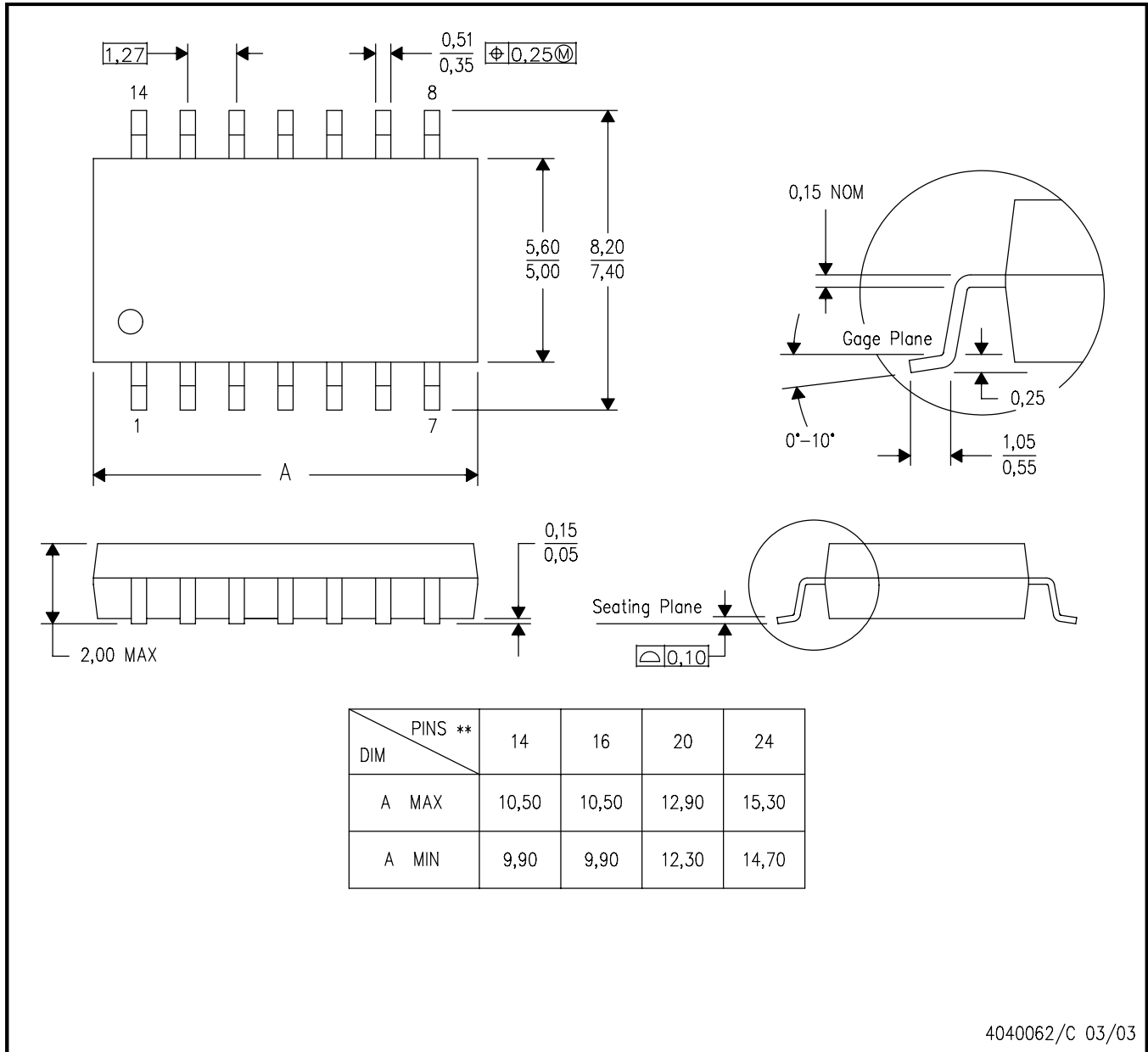
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.