TL07xx Low-Noise JFET-Input Operational Amplifiers

1 Features

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion: 0.003% Typical
- Low Noise
  V_n = 18 nV/$\sqrt{Hz}$ Typ at f = 1 kHz
- High-Input Impedance: JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate: 13 V/μs Typical
- Common-Mode Input Voltage Range Includes V_{CC+}

2 Applications

- Motor Integrated Systems: UPS
- Drives and Control Solutions: AC Inverter and VF Drives
- Renewables: Solar Inverters
- Pro Audio Mixers
- DLP Front Projection System
- Oscilloscopes

3 Description

The TL07xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low-input bias and offset currents, and low offset-voltage temperature coefficient. The low harmonic distortion and low noise make the TL07xseries ideally suited for high-fidelity and audio pre-amplifier applications. Offset adjustment and external compensation options are available within the TL07x family.

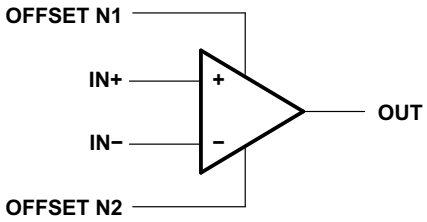
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL07xxD	SOIC (14)	8.65 mm × 3.91 mm
	SOIC (8)	4.90 mm x 3.90 mm
TL07xxFK	LCCC (20)	8.89 mm × 8.89 mm
TL07xxJG	PDIP (8)	9.59 mm x 6.67 mm
TL074xJ	CDIP (14)	19.56 mm × 6.92 mm
TL07xxP	PDIP (8)	9.59 mm x 6.35 mm
TL07xxPS	SO (8)	6.20 mm x 5.30 mm
TL074xN	PDIP (14)	19.3 mm × 6.35 mm
TL074xNS	SO (14)	10.30 mm × 5.30 mm
TL07xxPW	TSSOP (8)	4.40 mm x 3.00 mm
TL074xPW	TSSOP (14)	5.00 mm × 4.40 mm

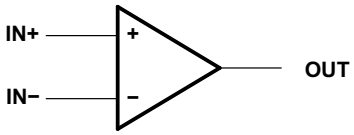
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Symbols

TL071

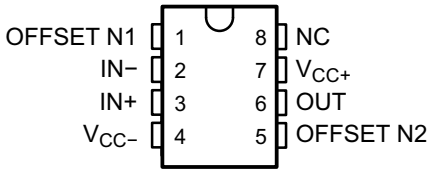


TL072 (each amplifier)
TL074 (each amplifier)

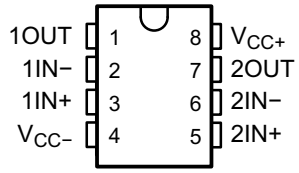


5 Pin Configuration and Functions

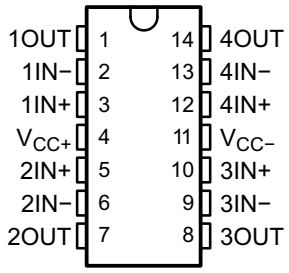
TL071x D, P, and PS Package
8-Pin SOIC, PDIP, SO
Top View



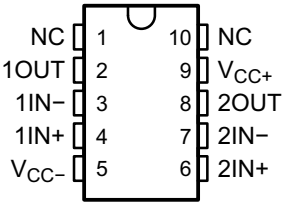
TL072x D, JG, P, PS and PW Package
8-Pin SOIC, CDIP, PDIP, SO
Top View



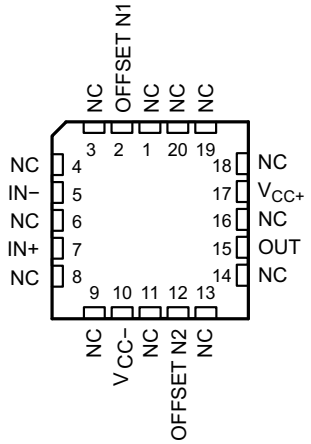
TL074x D, J, N , NS, PW, and W Package
14-Pin SOIC, CDIP, PDIP, SO and CFP
Top View



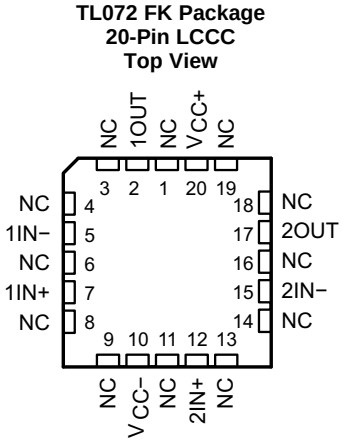
TL072 U Package
10-Pin CFP
Top View



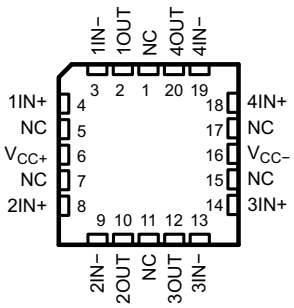
TL071 FK Package
20-Pin LCCC
Top View



TL072 FK Package
20-Pin LCCC
Top View



TL074 FK Package
20-Pin LCCC
Top View



Pin Functions

PIN								I/O	DESCRIPTION
NAME	TL071		TL072			TL074			
	SOIC, PDIP, SO	LCCC	SOIC, CDIP, PDIP, SO	CFP	LCCC	SOIC, CDIP, PDIP, SO, CFP	LCCC		
1IN–	—	—	2	3	5	2	3	I	Inverting input
1IN+	—	—	3	4	7	3	4	I	Non-Inverting input
1OUT	—	—	1	2	2	1	2	O	Output
2IN–	—	—	6	7	15	6	9	I	Inverting input
2IN+	—	—	5	6	12	5	8	I	Non-Inverting input
2OUT	—	—	7	8	17	7	10	O	Output
3IN–	—	—	—	—	—	9	13	I	Inverting input
3IN+	—	—	—	—	—	10	14	I	Non-Inverting input
3OUT	—	—	—	—	—	8	12	O	Output
4IN–	—	—	—	—	—	13	19	I	Inverting input
4IN+	—	—	—	—	—	12	18	I	Non-Inverting input
4OUT	—	—	—	—	—	14	20	O	Output
IN–	2	5	—	—	—	—	—	I	Inverting input
IN+	3	7	—	—	—	—	—	I	Non-Inverting input
NC(1)	8	1	—	1	1	—	1	—	Do not connect
		3			—				
		4			—				
		6			—				
		8			—				
		9			9				
		11		0	11		5		
		13			13		7		
		14			14		11		
		16			16		15		
		18			18		17		
		19			19				
		20							
OFFSET N1	1	2	—	—	—	—	—	—	Input offset adjustment
OFFSET N2	5	12	—	—	—	—	—	—	Input offset adjustment
OUT	6	15	—	—	—	—	—	O	Output
$V_{CC–}$	4	10	4	5	10	11	16	—	Power supply
V_{CC+}	7	17	8	9	20	4	6	—	Power supply

(1) NC – No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC+} - V_{CC-}	Supply voltage (2)	–18	18	V
V_{ID}	Differential input voltage (3)	–30	30	V
V_I	Input voltage (2) (4)	–15	15	V
	Duration of output short circuit (5)	Unlimited		
T_J	Operating Virtual Junction Temperature		150	°C
	Case temperature for 60 seconds - FK package		260	°C
	Lead temperature 1.8 mm (1/16 inch) from case for 10 seconds		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}	Supply voltage		–5	–15	V
V_{CM}	Common-mode voltage		V_{CC-} + 4	V_{CC+} – 4	V
T_A	Operating free-air temperature	TL07xM	–55	125	°C
		TL08xQ	–40	125	
		TL07xI	–40	85	
		TL07xA, TL07xB, TL07xC	0	70	

6.4 Thermal Information

THERMAL METRIC (1)		TL071/TL072/TL074											UNIT
		D (SOIC)		FK (LCCC)	J (CDIP)		N (PDIP)		NS (SO)		PW (TSSOP)		
		8 PINS	14 PINS	20 PINS	8 PINS	14 PINS	8 PINS	14 PINS	8 PINS	14 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	86	—	—	—	85	80	95	76	150	113	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	5.61	15.05	14.5	—	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics, TL07xC, TL07xAC, TL07xBC, TL07xI

V_{CC}± = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		T_A[2]	TL071C, TL072C, TL074C			TL071AC, TL072AC, TL074AC			TL071BC, TL072BC, TL074BC			TL071I, TL072I, TL074I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0,	R_S = 50 Ω	25°C		3	10		3	6		2	3		3	6	mV
				Full range			13			7.5			5			8	
αV_{IO}	Temperature coefficient of input offset voltage	V_O = 0,	R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current	V_O = 0		25°C		5	100		5	100		5	100		5	100	pA
				Full range			10			2			2			2	nA
I_{IB}	Input bias current[3]	V_O = 0		25°C		65	200		65	200		65	200		65	200	pA
				Full range			7			7			7			7	nA
V_{ICR}	Common-mode input voltage range			25°C	±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L= 10 kΩ		25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L≥ 10 kΩ		Full range	±12			±12			±12			±12			
		R_L≥ 2 kΩ			±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
				Full range	15			25			25			25			
B_1	Utility-gain bandwidth			25°C		3			3			3			3		MHz
r_i	Input resistance			25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0,	R_S = 50 Ω	25°C	70	100		75	100		75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0,	R_S = 50 Ω	25°C	70	100		80	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0,	No load	25°C		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{O1} /V_{O2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120			120			120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range is T_A = 0°C to 70°C for TL07_C,TL07_AC, TL07_BC and is T_A = –40°C to 85°C for TL07_I.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 1. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.6 Electrical Characteristics, TL07xM

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	T_A(2)	TL071M, TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		µV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100	pA
			Full range			20			20	nA
I_{IB}	Input bias current	V_O = 0	25°C		65	200		65	200	pA
						50			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	35	200		35	200		V/mV
				15			15			
B_1	Unity-gain bandwidth				3			3		MHz
r_i	Input resistance				10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

(1) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 1. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

(2) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is T_A = –55°C to 125°C.

6.7 Switching Characteristics

$V_{CC\pm}$ = ±15 V, T_A= 25°C

PARAMETER		TEST CONDITIONS		TL07xM			TL07xC, TL07xAC, TL07xBC, TL07xI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 20	5	13		8	13		V/µs
t_r	Rise-time overshoot factor	V_I = 20 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 20		0.1			0.1		µs
					20%			20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		µV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, R_L ≥ 2 kΩ, f = 1 kHz,	A_{VD} = 1, RS ≤ 1 kΩ,		0.003%			0.003%		

6.8 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

Table 1. Table of Graphs

			Figure
I_{IB}	Input bias current	versus Free-air temperature	Figure 1
V_{OM}	Maximum peak output voltage	versus Frequency versus Free-air temperature versus Load resistance versus Supply voltage	Figure 2, Figure 3, Figure 4 Figure 5 Figure 6 Figure 7
A_{VD}	Large signal differential voltage amplification	versus Free-air temperature versus Load resistance	Figure 8 Figure 9
	Phase shift	versus Frequency	Figure 9
	Normalized unity-gain bandwidth	versus Free-air temperature	Figure 10
	Normalized phase shift	versus Free-air temperature	Figure 10
CMRR	Common-mode rejection ratio	versus Free-air temperature	Figure 11
I_{CC}	Supply current	versus Free-air temperature versus Supply voltage	Figure 12 Figure 13
P_D	Total power dissipation	versus Free-air temperature	Figure 14
	Normalized slew rate	versus Free-air temperature	Figure 15
V_n	Equivalent input noise voltage	versus Frequency	Figure 16
THD	Total harmonic distortion	versus Frequency	Figure 17
	Large-signal pulse response	versus Time	Figure 18
V_O	Output voltage	versus Elapsed time	Figure 19

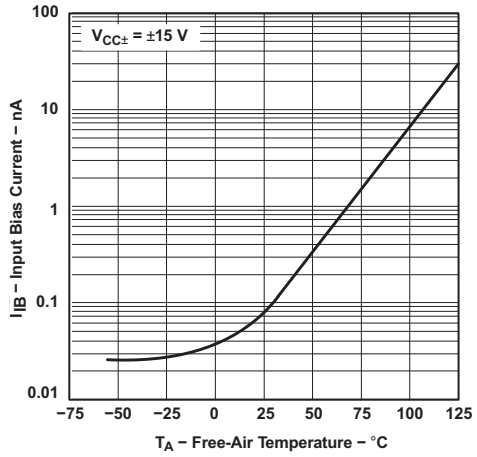


Figure 1. Input Bias Current vs Free-Air Temperature

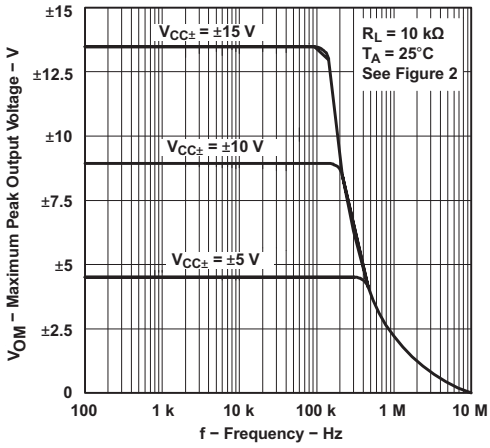


Figure 2. Maximum Peak Output Voltage vs Frequency

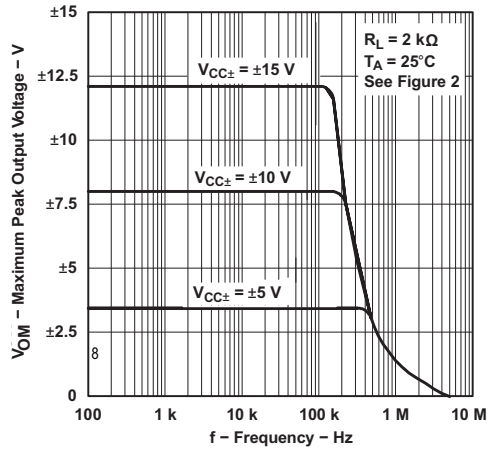


Figure 3. Maximum Peak Output Voltage vs Frequency

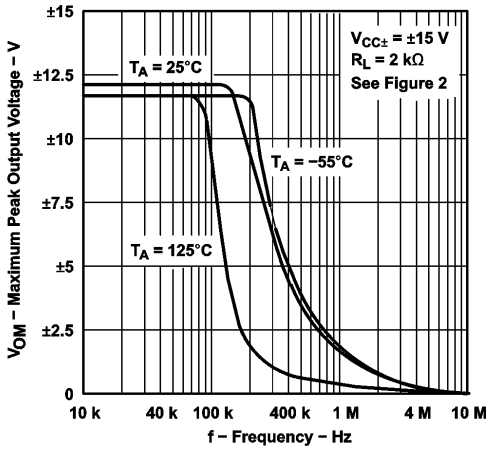


Figure 4. Maximum Peak Output Voltage vs Frequency

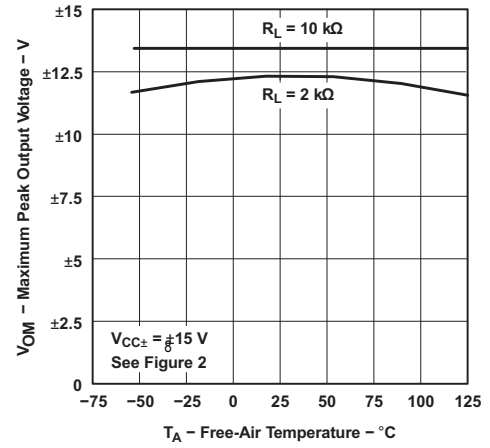


Figure 5. Maximum Peak Output Voltage vs Free-Air Temperature

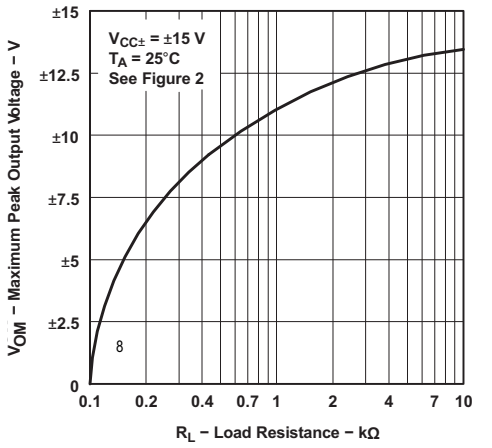


Figure 6. Maximum Peak Output Voltage vs Load Resistance

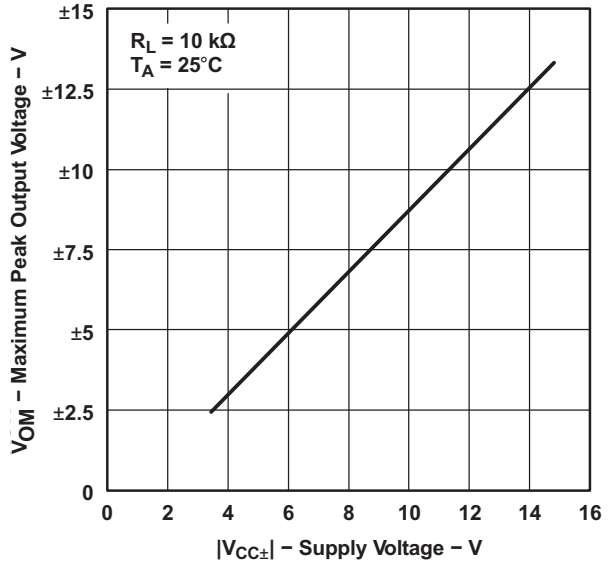


Figure 7. Maximum Peak Output Voltage vs Supply Voltage

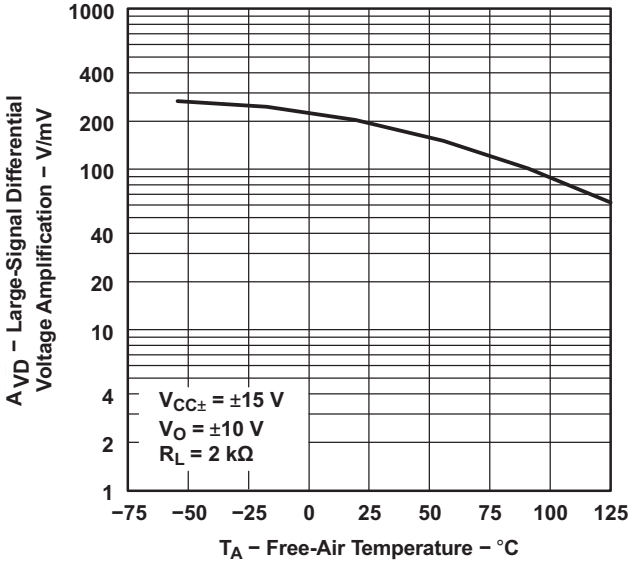


Figure 8. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

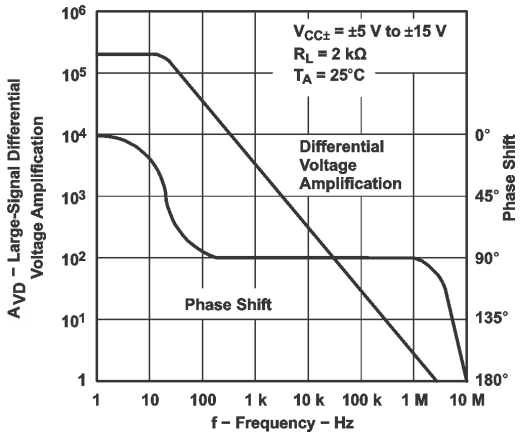


Figure 9. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

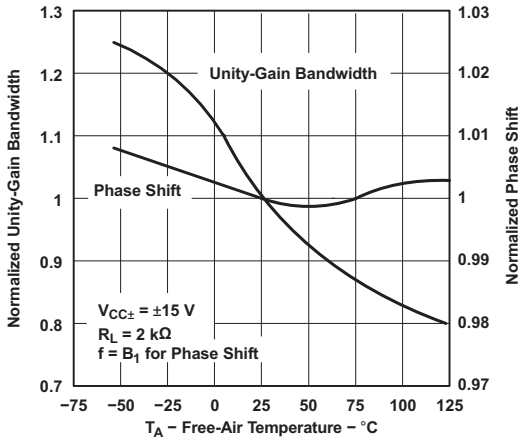


Figure 10. Normalized Unity-Gain Bandwidth and Phase Shift vs Free-Air Temperature

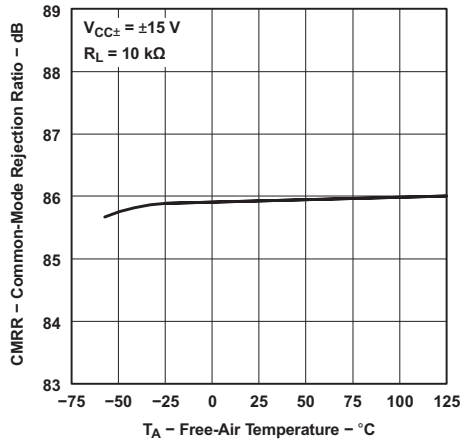


Figure 11. Common-Mode Rejection Ratio vs Free-Air Temperature

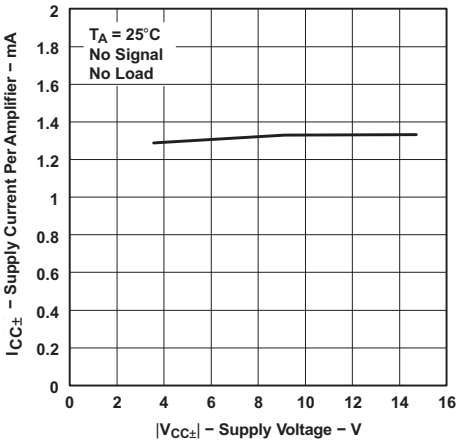


Figure 12. Supply Current Per Amplifier vs Supply Voltage

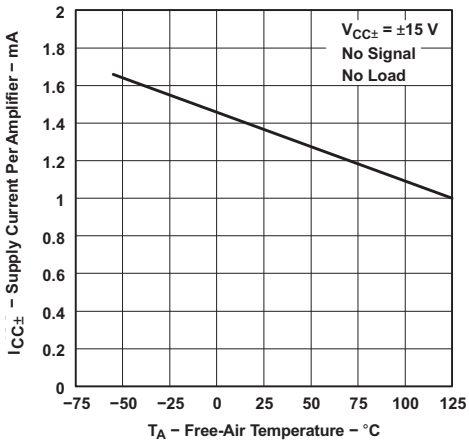


Figure 13. Supply Current Per Amplifier vs Free-Air Temperature

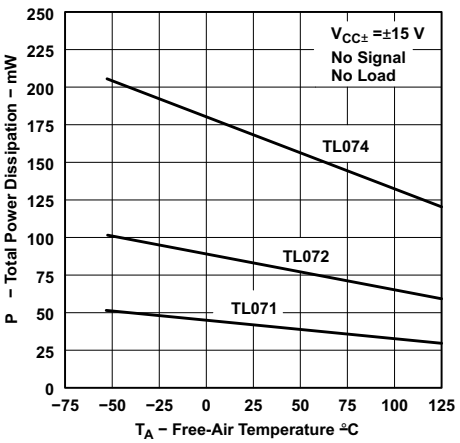


Figure 14. Total Power Dissipation vs Free-Air Temperature

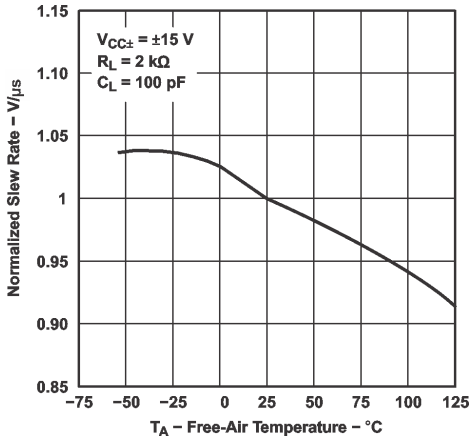


Figure 15. Normalized Slew Rate vs Free-Air Temperature

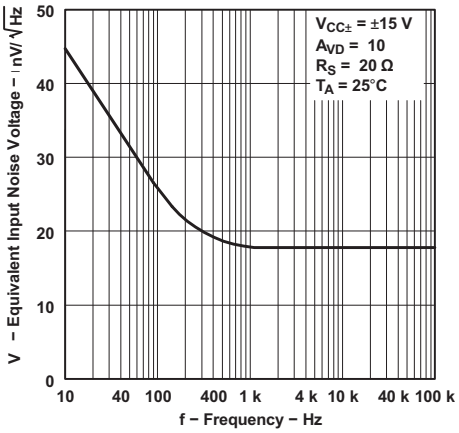


Figure 16. Equivalent Input Noise Voltage vs Frequency

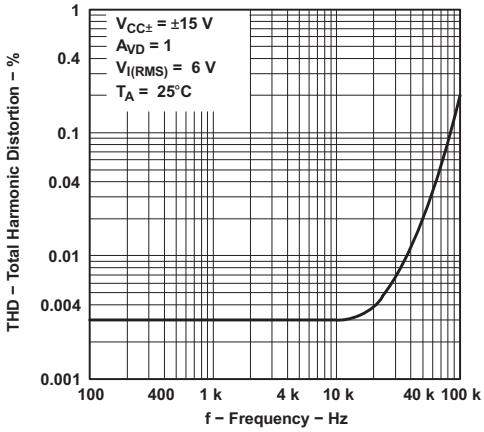


Figure 17. Total Harmonic Distortion vs Frequency

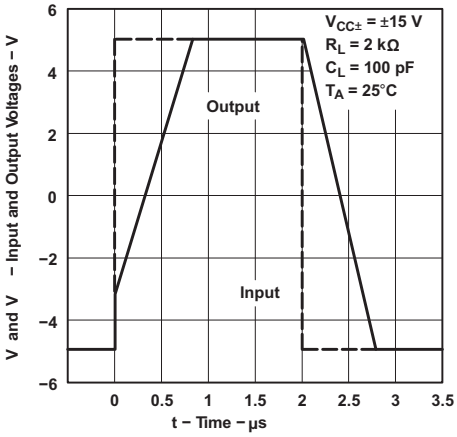


Figure 18. Voltage-Follower Large-Signal Pulse Response

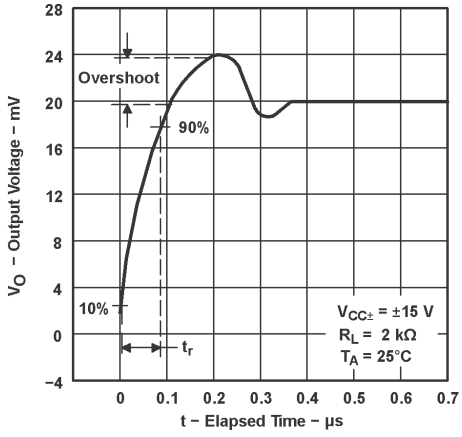


Figure 19. Output Voltage vs Elapsed Time

7 Parameter Measurement Information

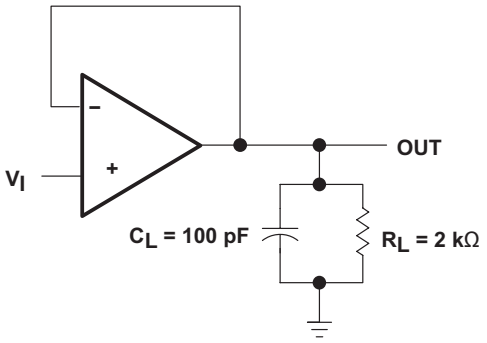


Figure 20. Unity-Gain Amplifier

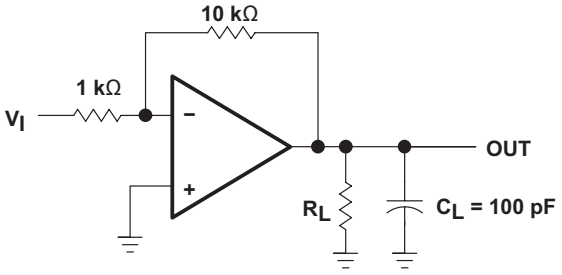


Figure 21. Gain-of-10 Inverting Amplifier

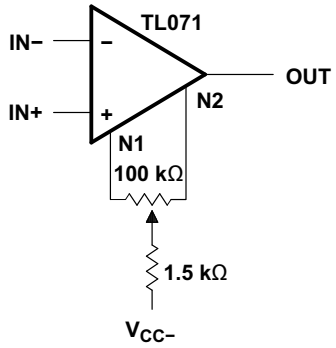


Figure 22. Input Offset-Voltage Null Circuit

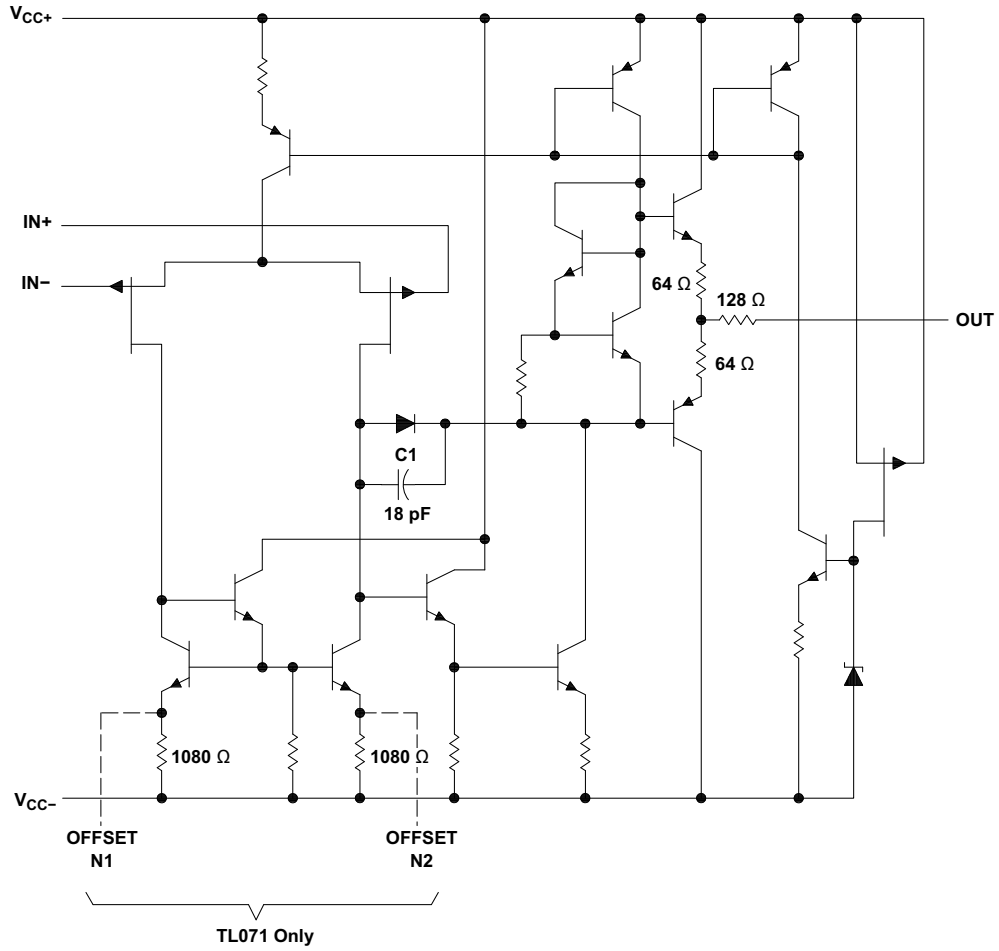
8 Detailed Description

8.1 Overview

The JFET-input operational amplifiers is in the TL07xx series are similar to the TL08x series, with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07xx series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

8.2 Functional Block Diagram



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

8.3 Feature Description

8.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL07x devices will add little harmonic distortion when used in audio signal applications.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 13-V/µs slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

9.2 Typical Application

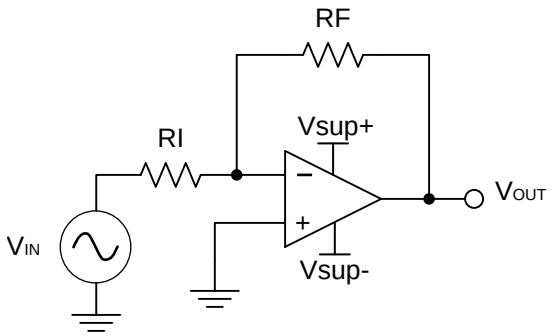


Figure 23. Inverting Amplifier

9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kilohm range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 kΩ for RI which means 36 kΩ will be used for RF. This was determined by Equation 3.

$$A_V = -\frac{RF}{RI} \quad (3)$$

Typical Application (continued)

9.2.3 Application Curve

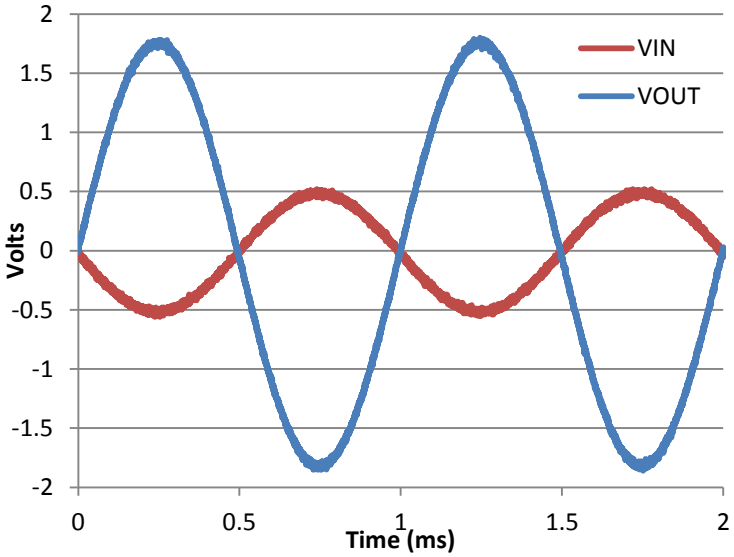


Figure 24. Input and Output Voltages of the Inverting Amplifier

9.3 System Examples

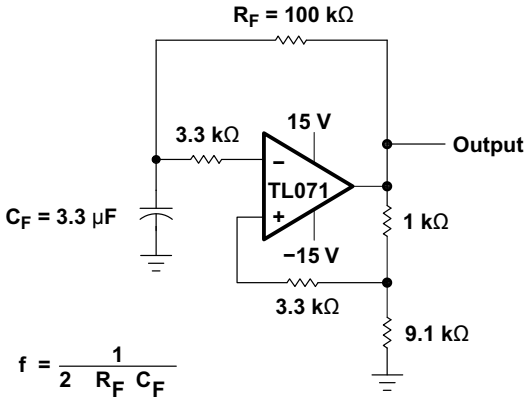


Figure 25. 0.5-Hz Square-Wave Oscillator

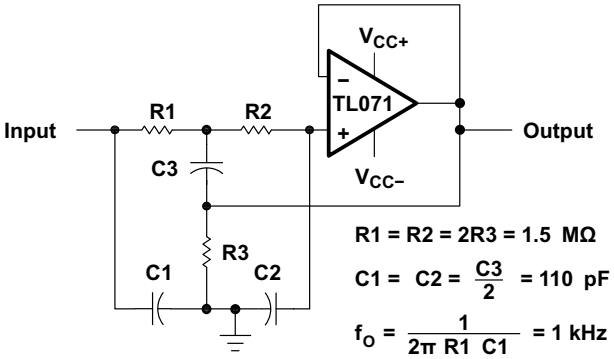


Figure 26. High-Q Notch Filter

System Examples (continued)

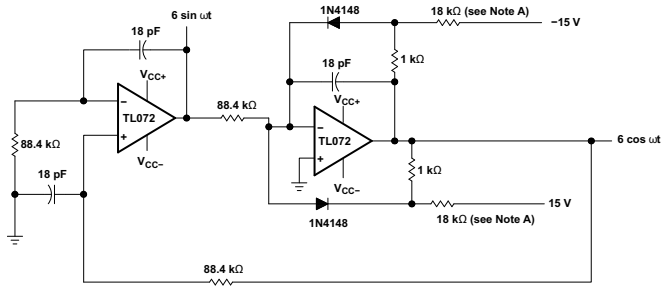


Figure 27. 100-kHz Quadrature Oscillator

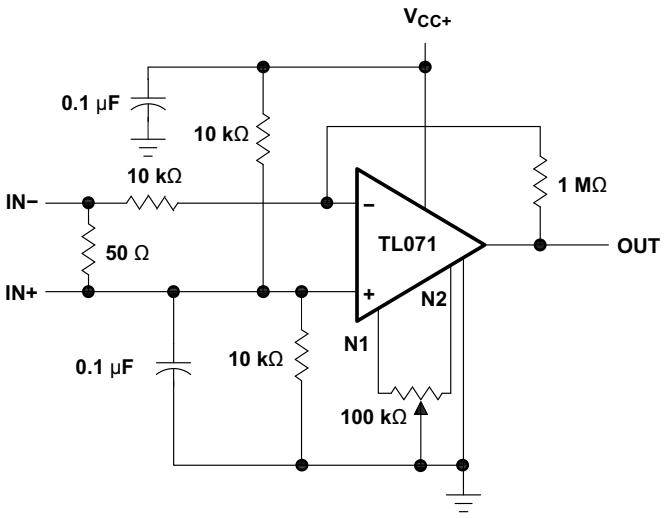


Figure 28. AC Amplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce

Layout Guidelines (continued)

leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

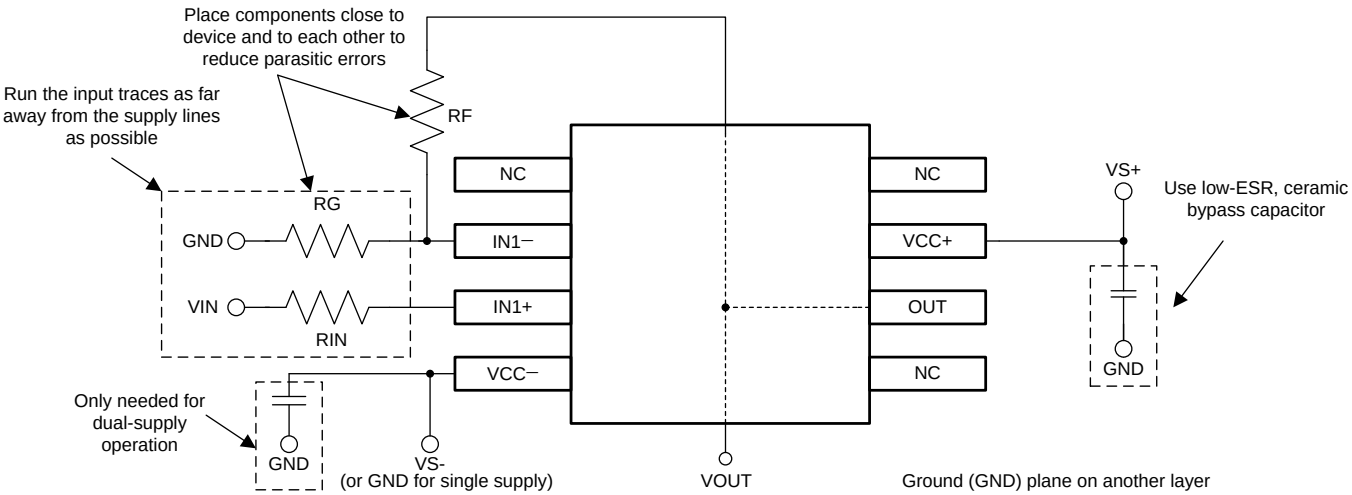


Figure 29. Operational Amplifier Board Layout for Noninverting Configuration

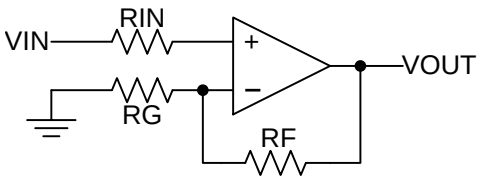
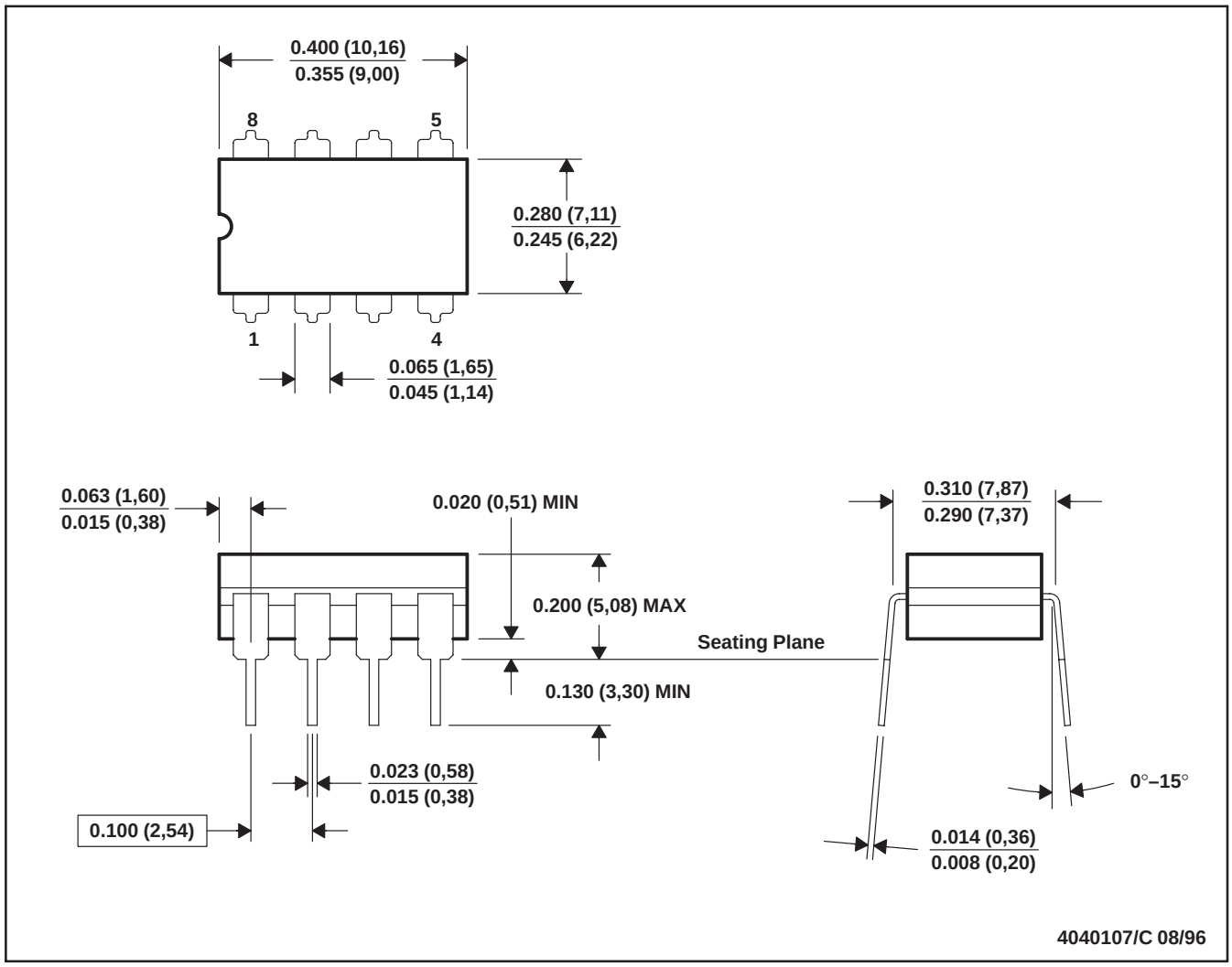


Figure 30. Operational Amplifier Schematic for Noninverting Configuration

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**

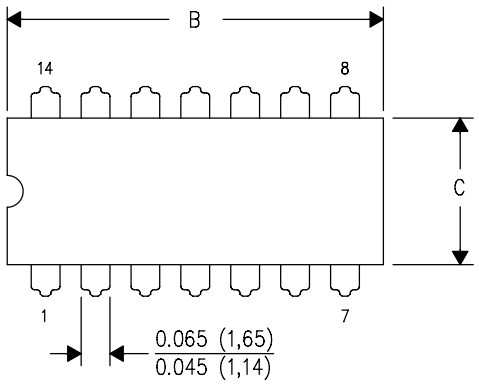


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

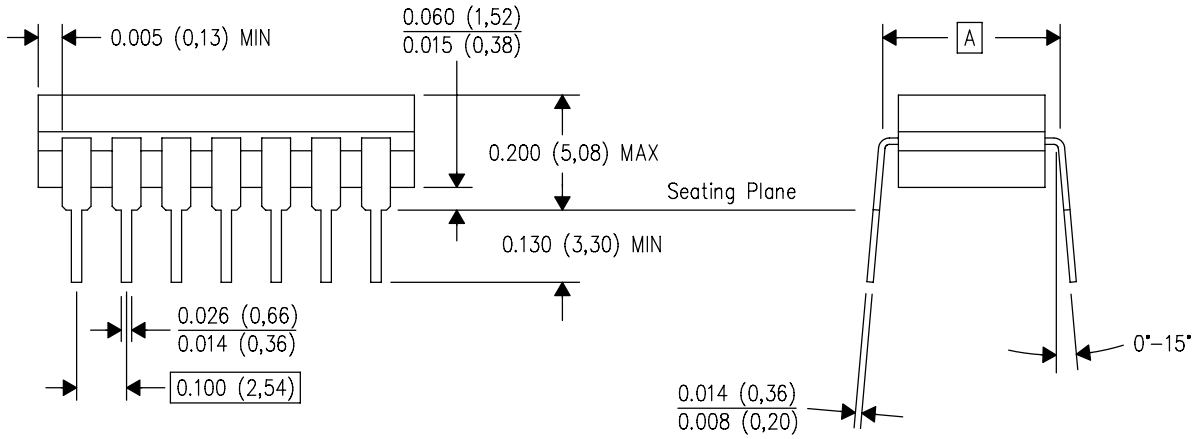
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



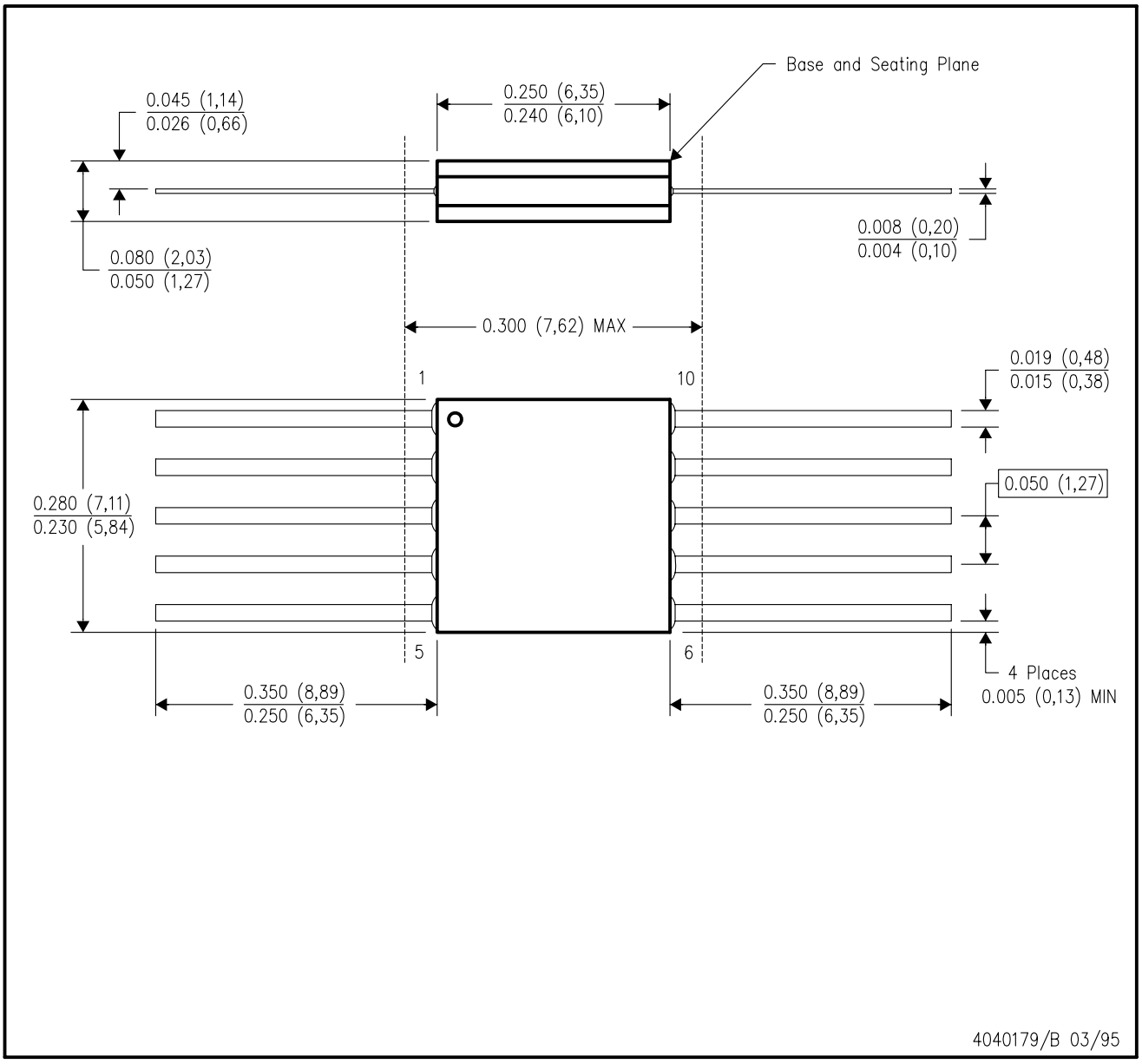
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

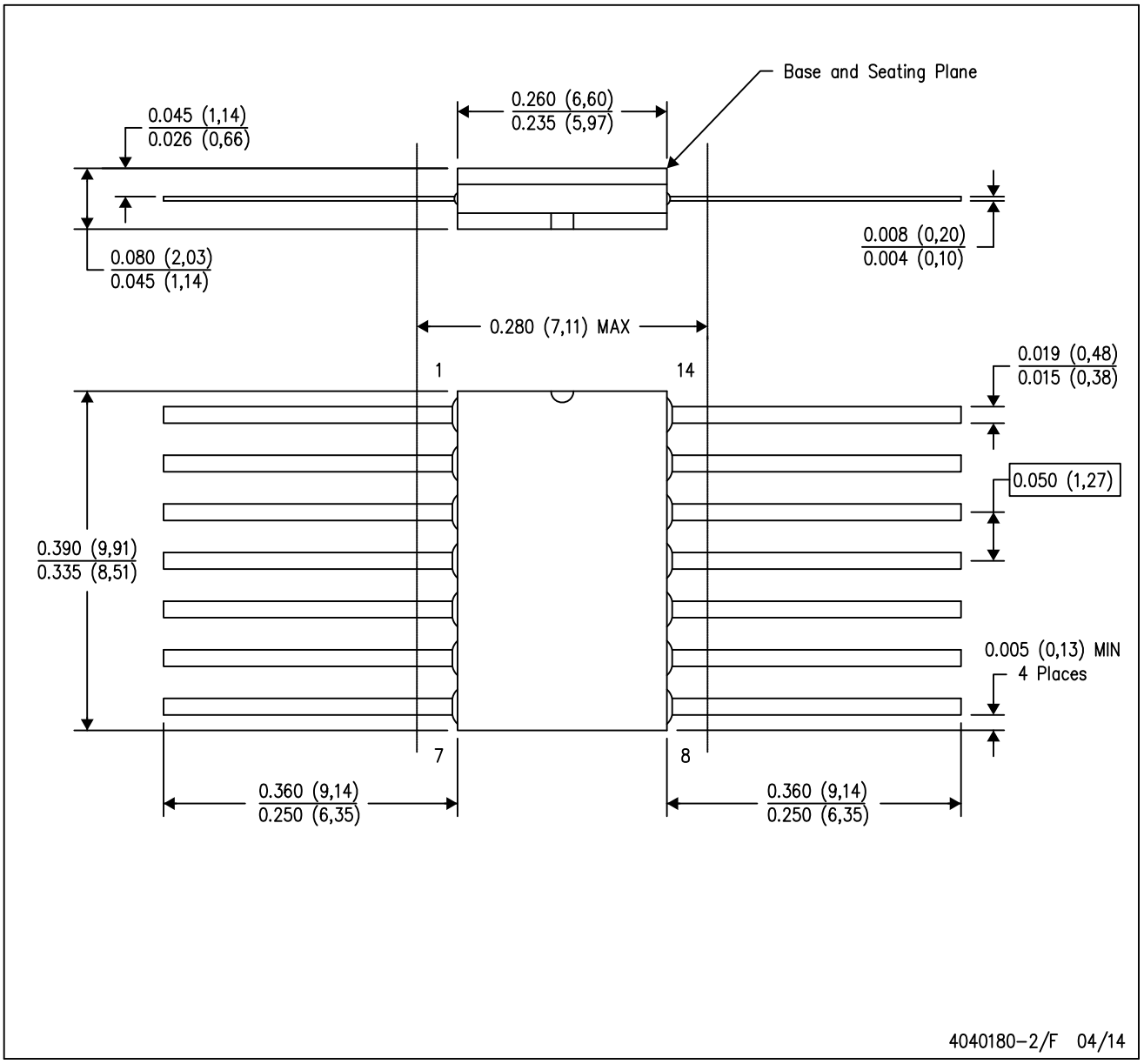
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

U (S–GDFP–F10) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

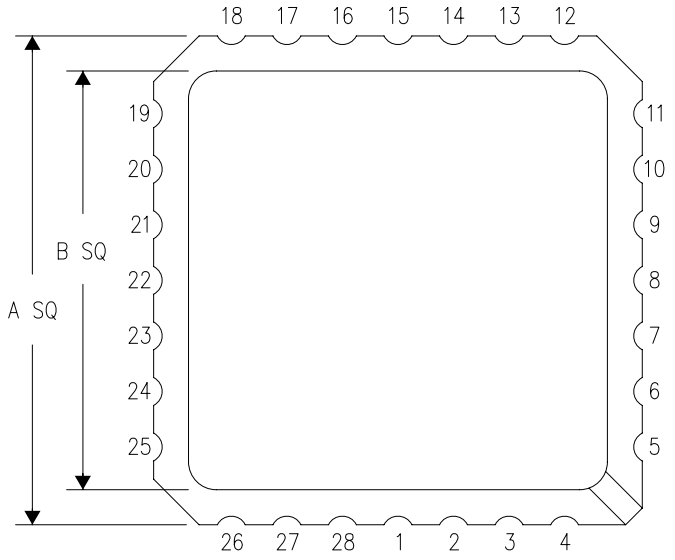
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



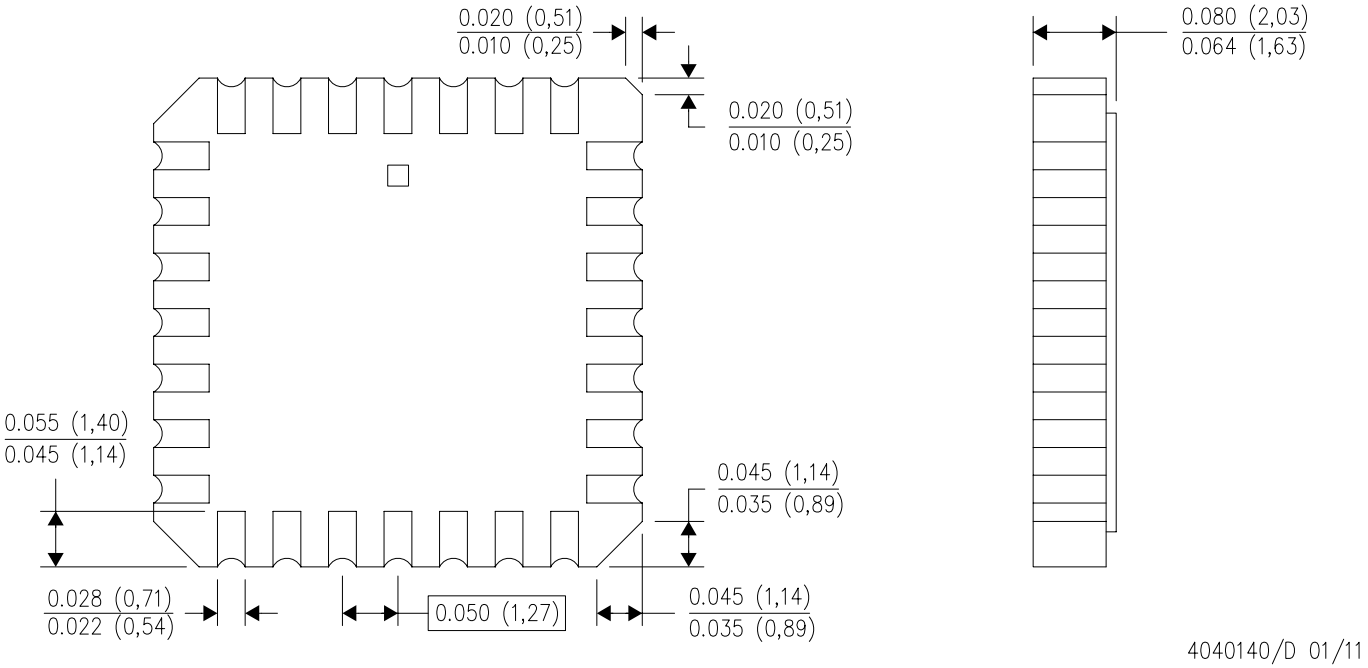
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



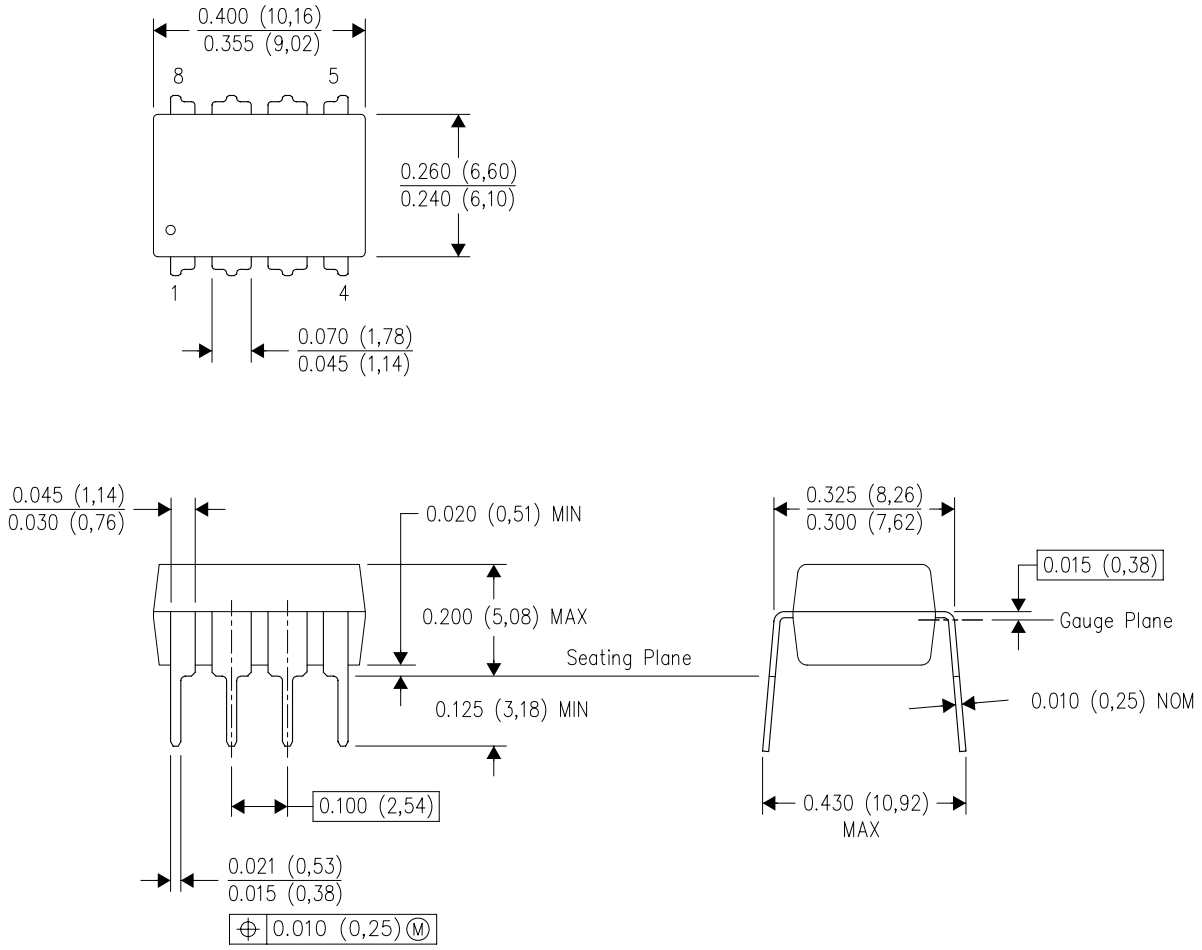
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



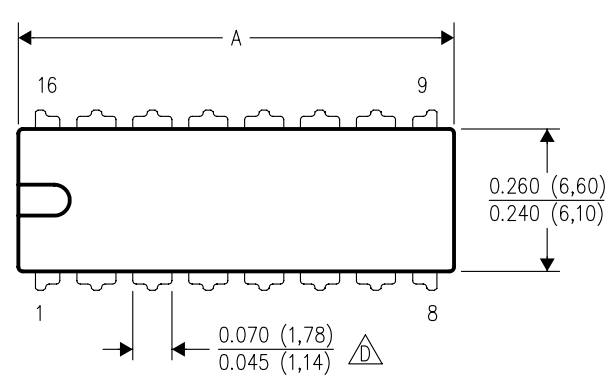
4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

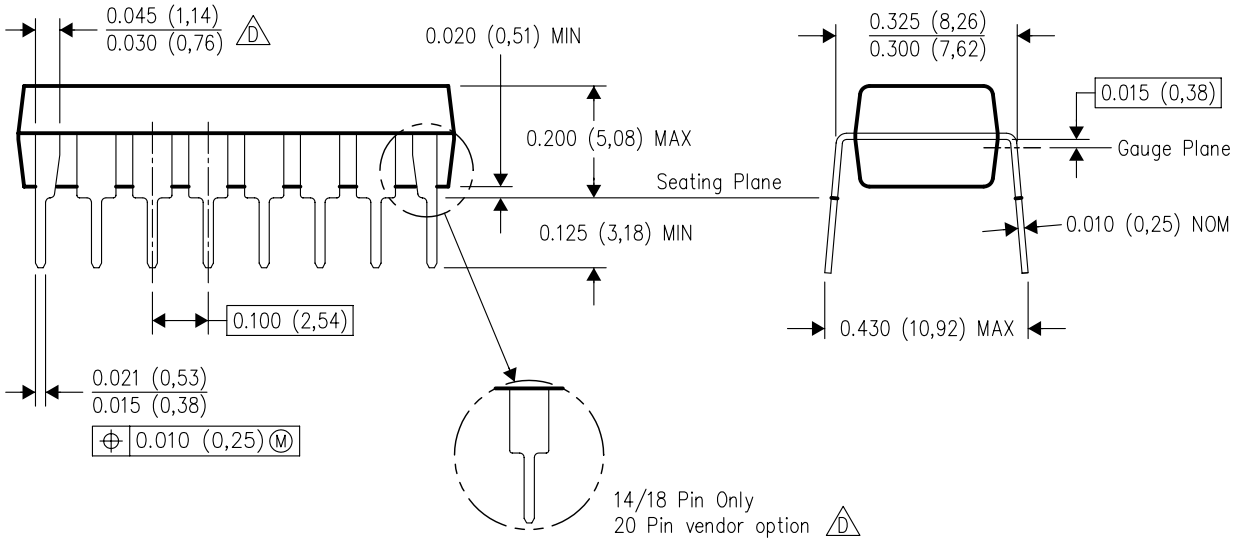
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



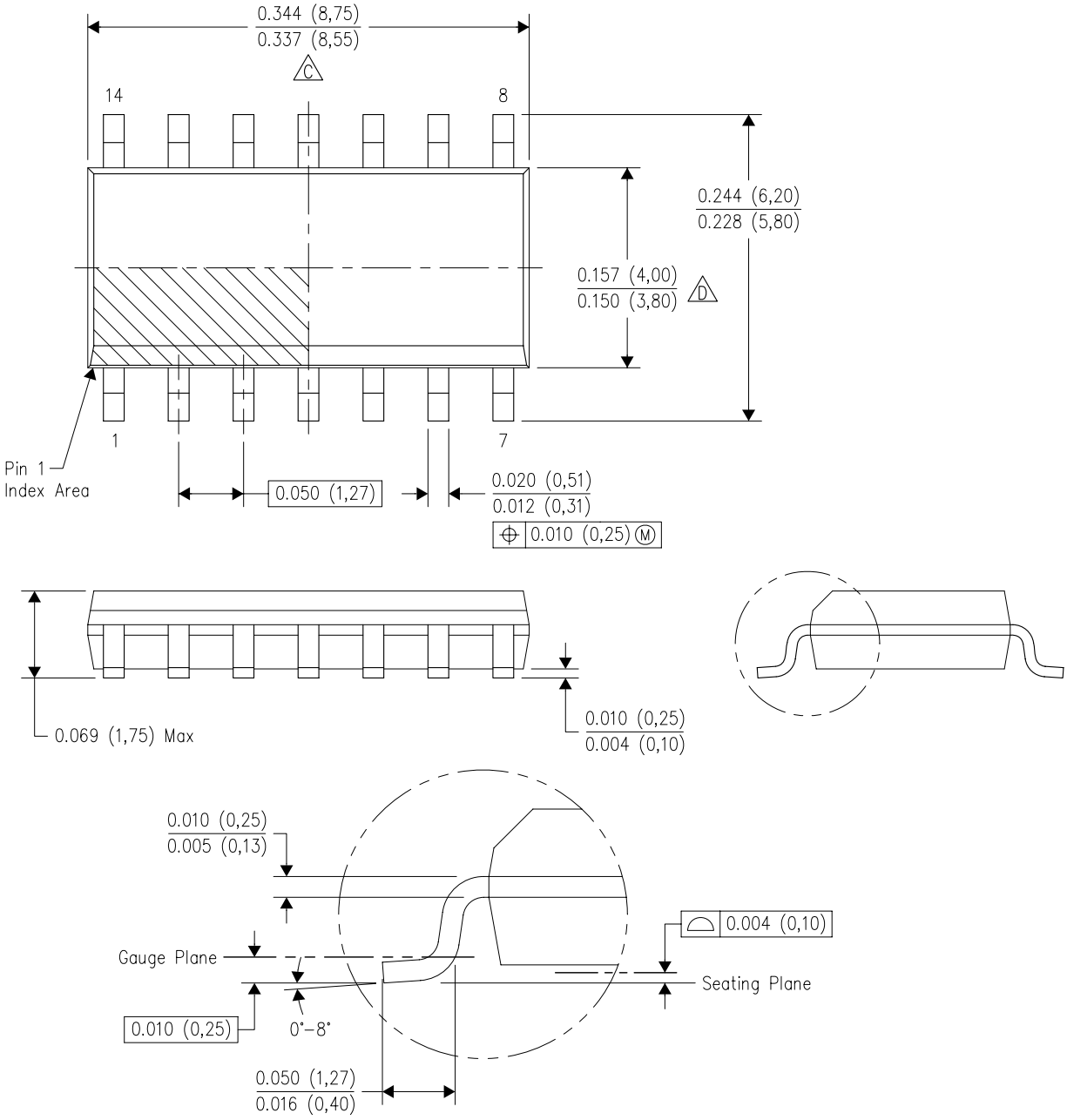
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

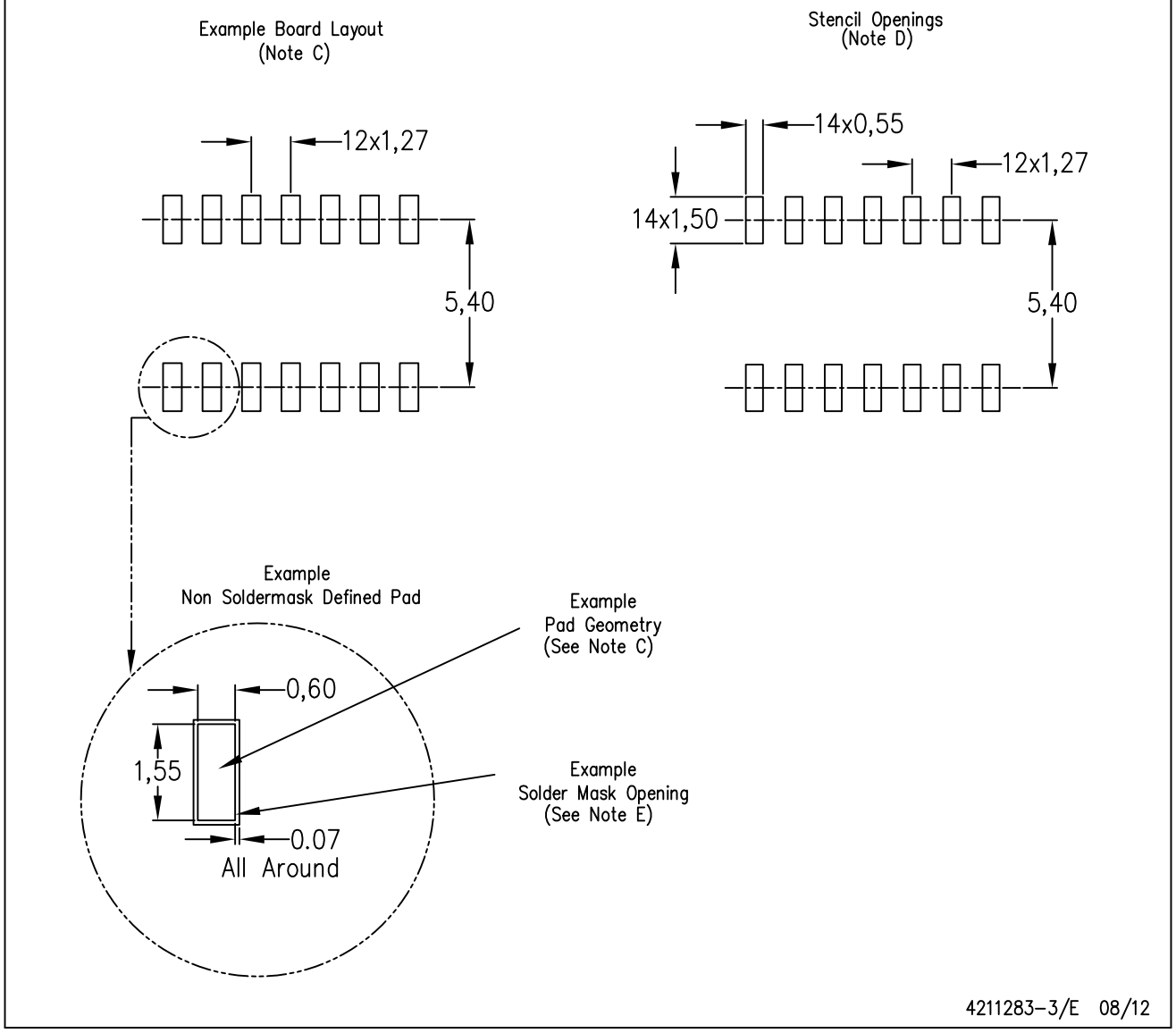
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



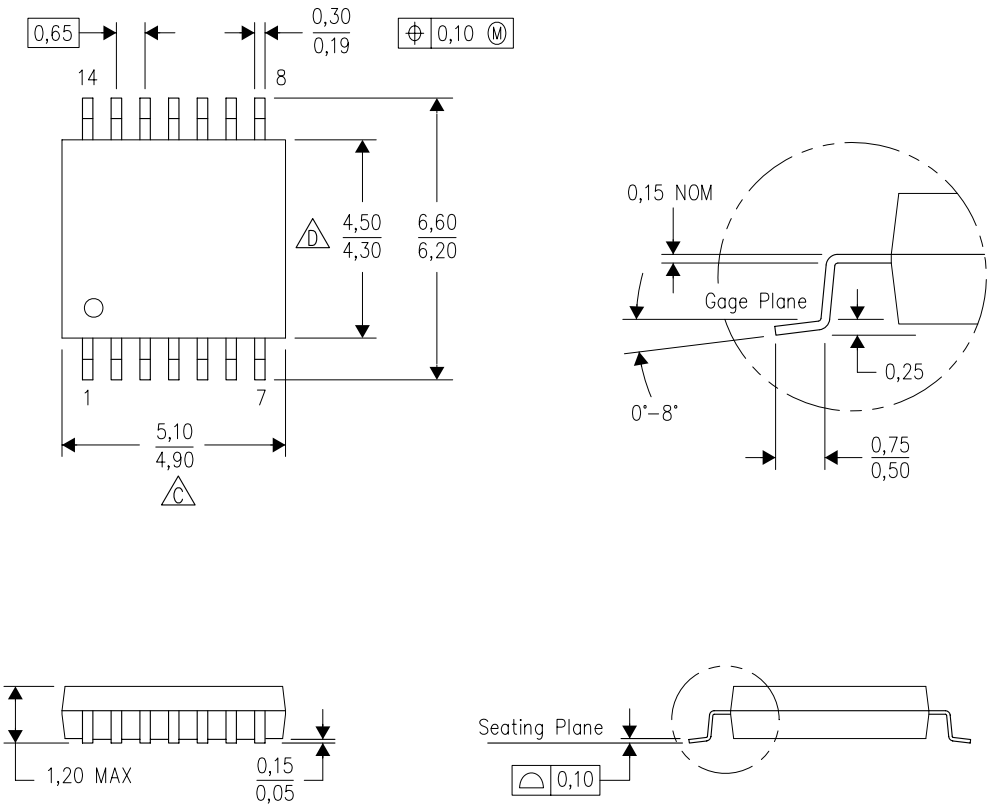
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

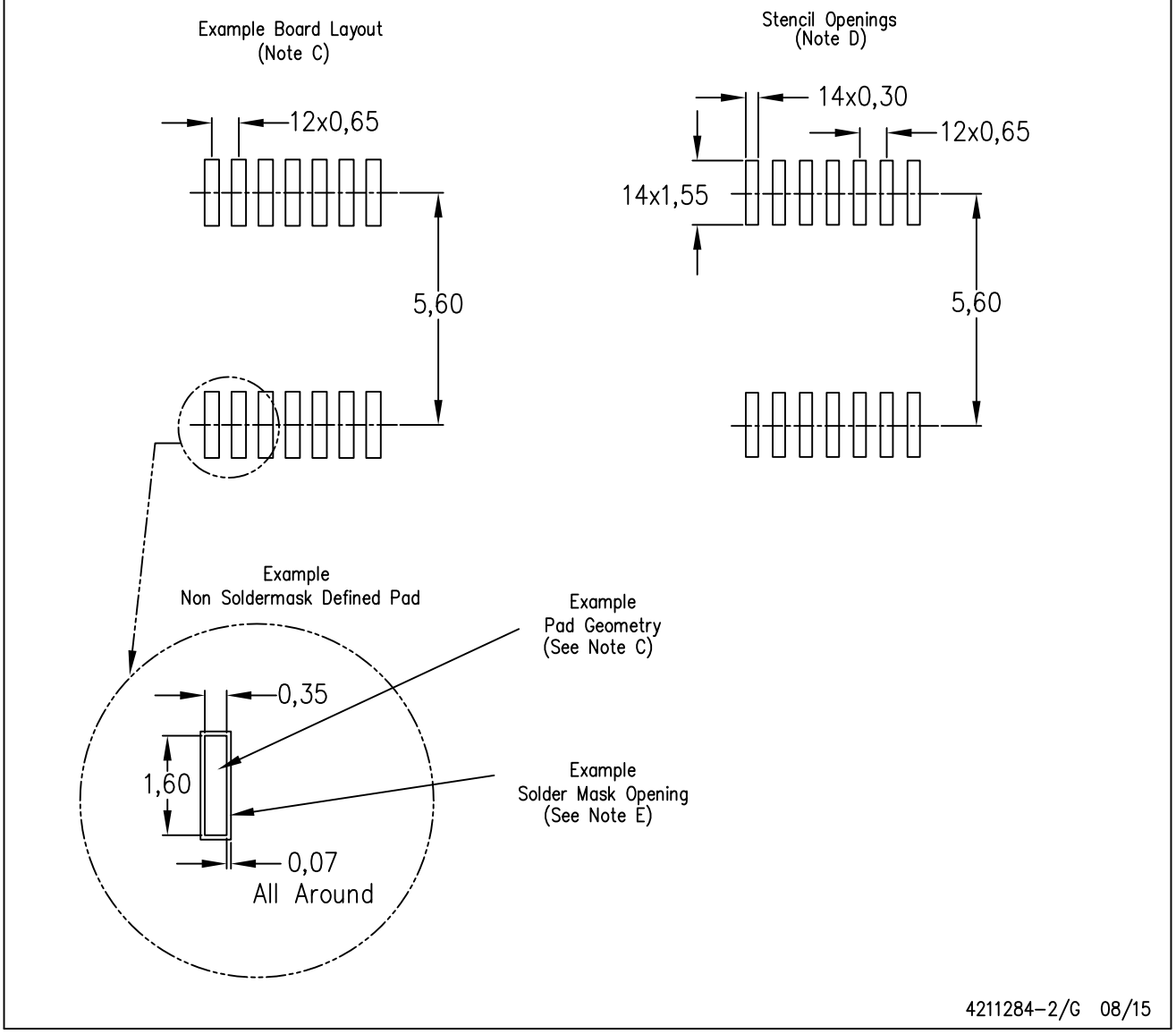
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



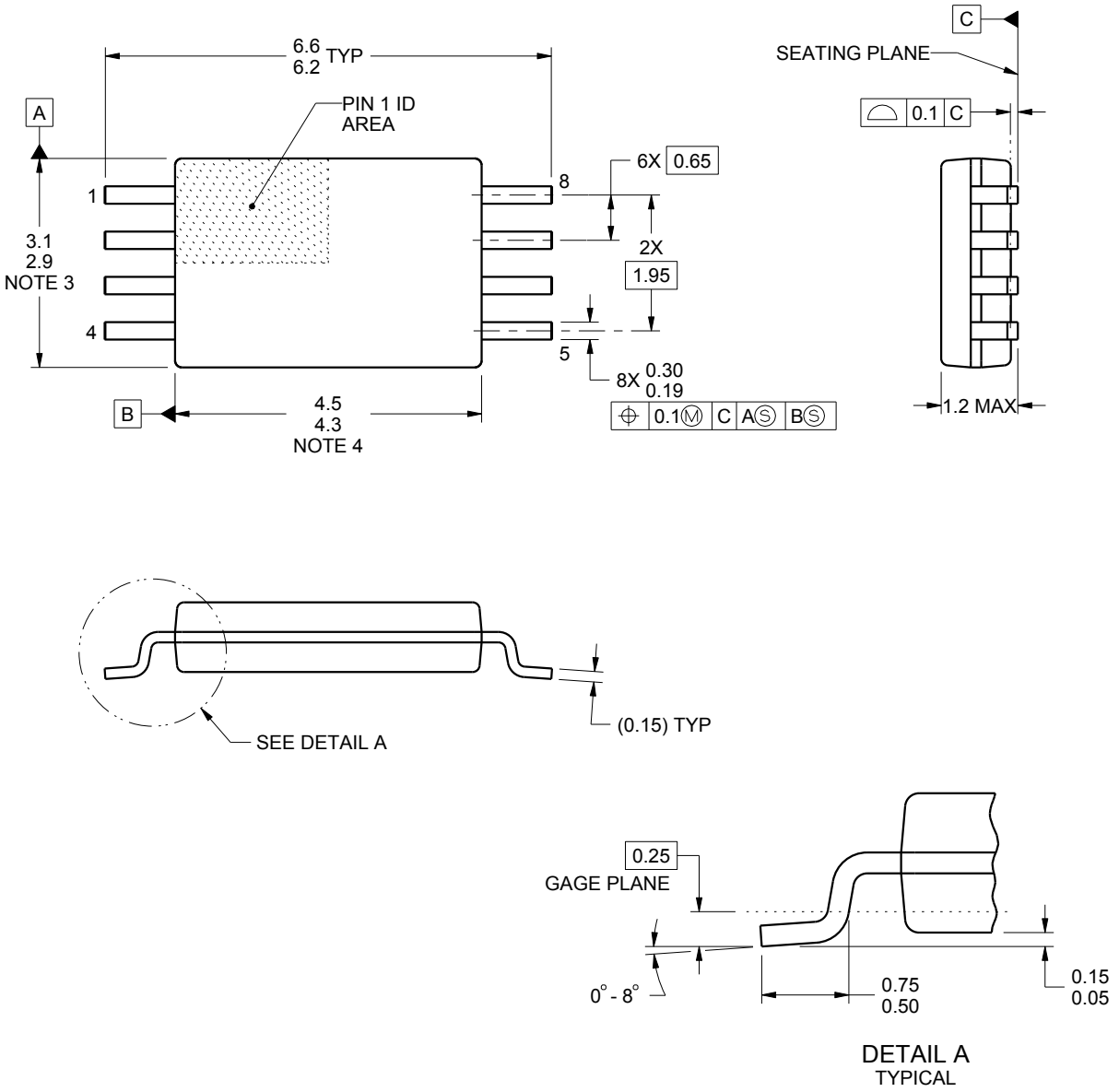
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

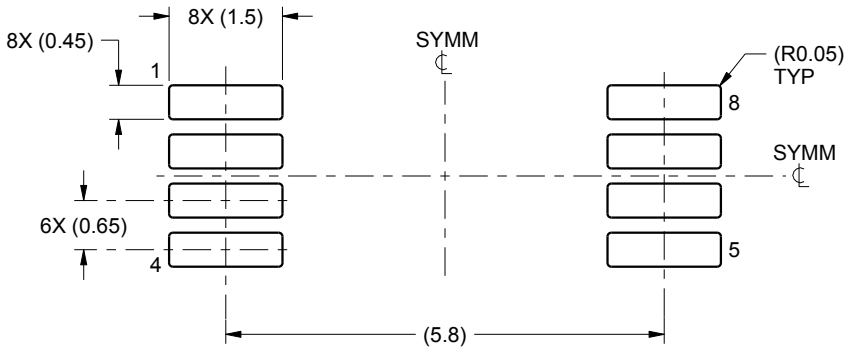
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

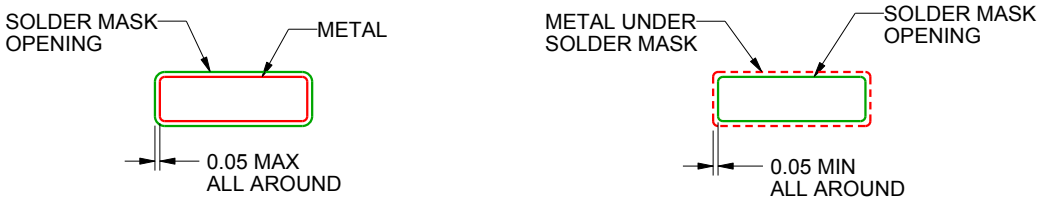


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

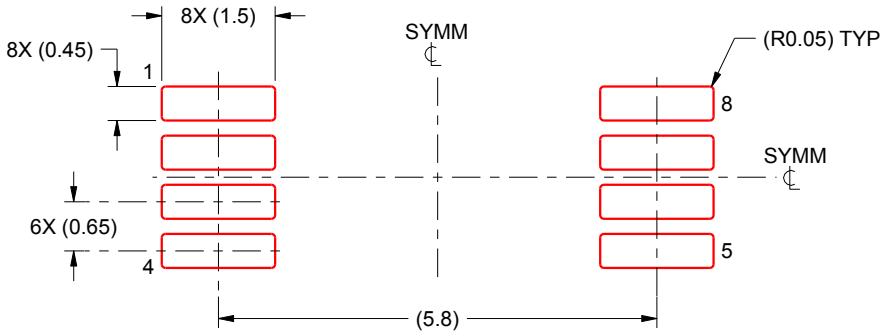
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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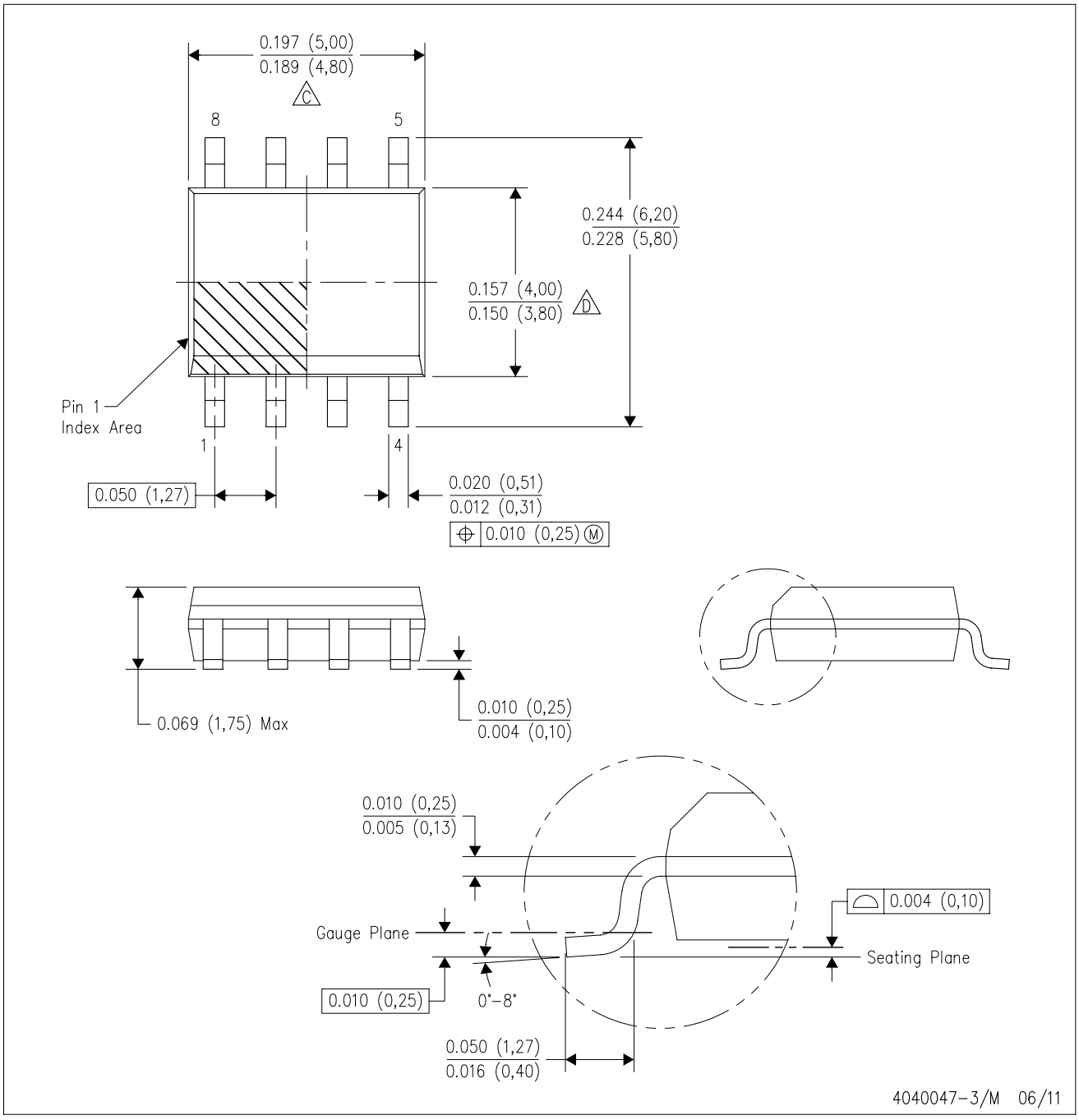
NOTES: (continued)

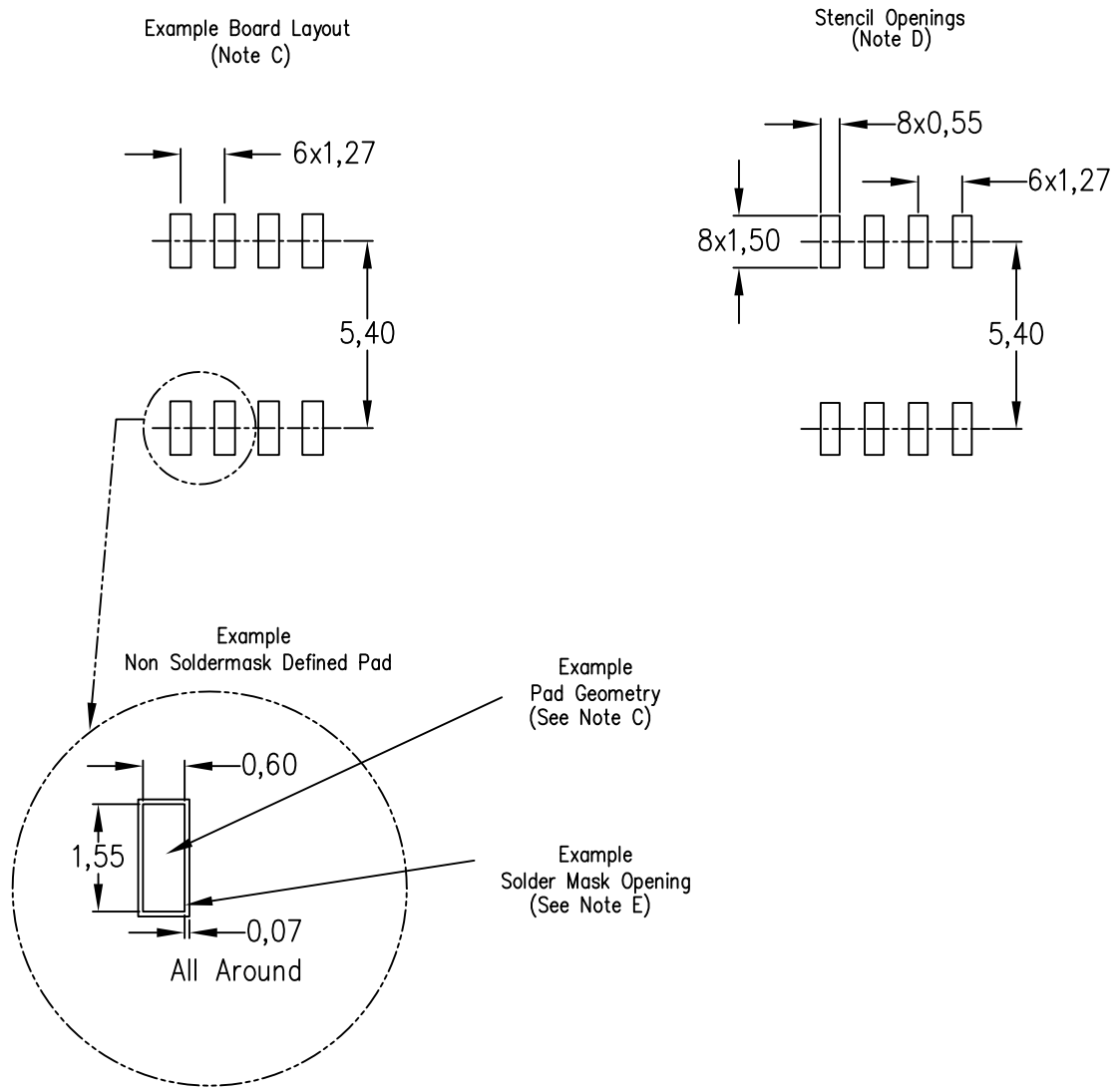
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

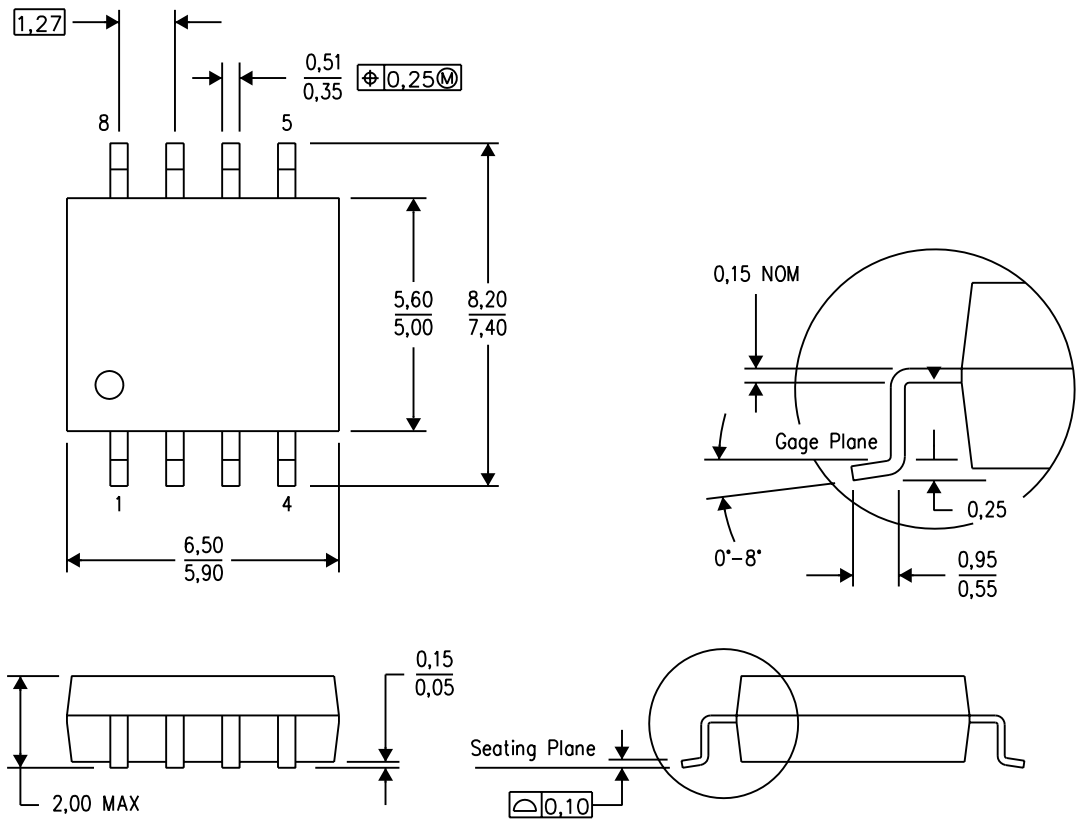
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

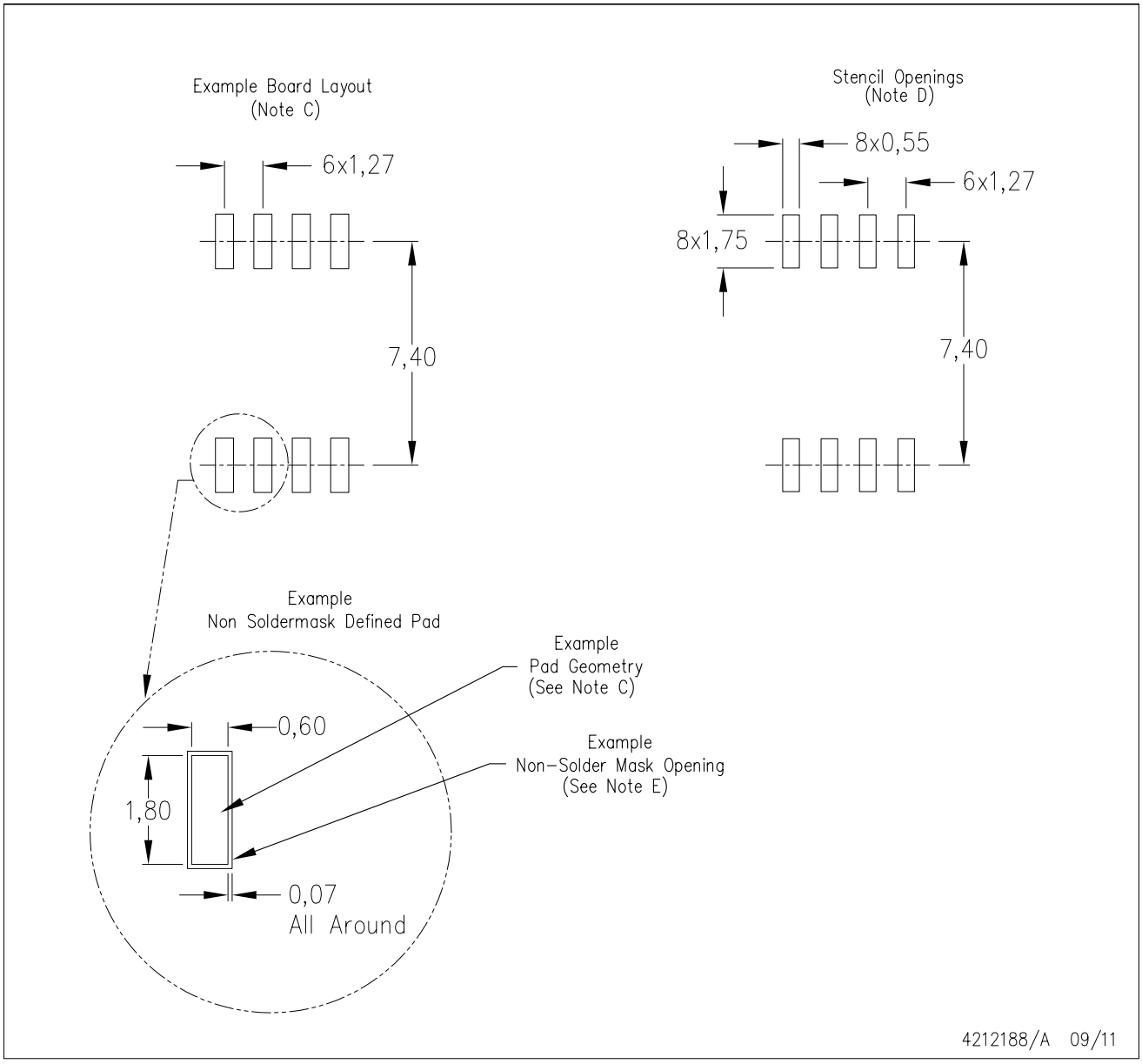
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8)

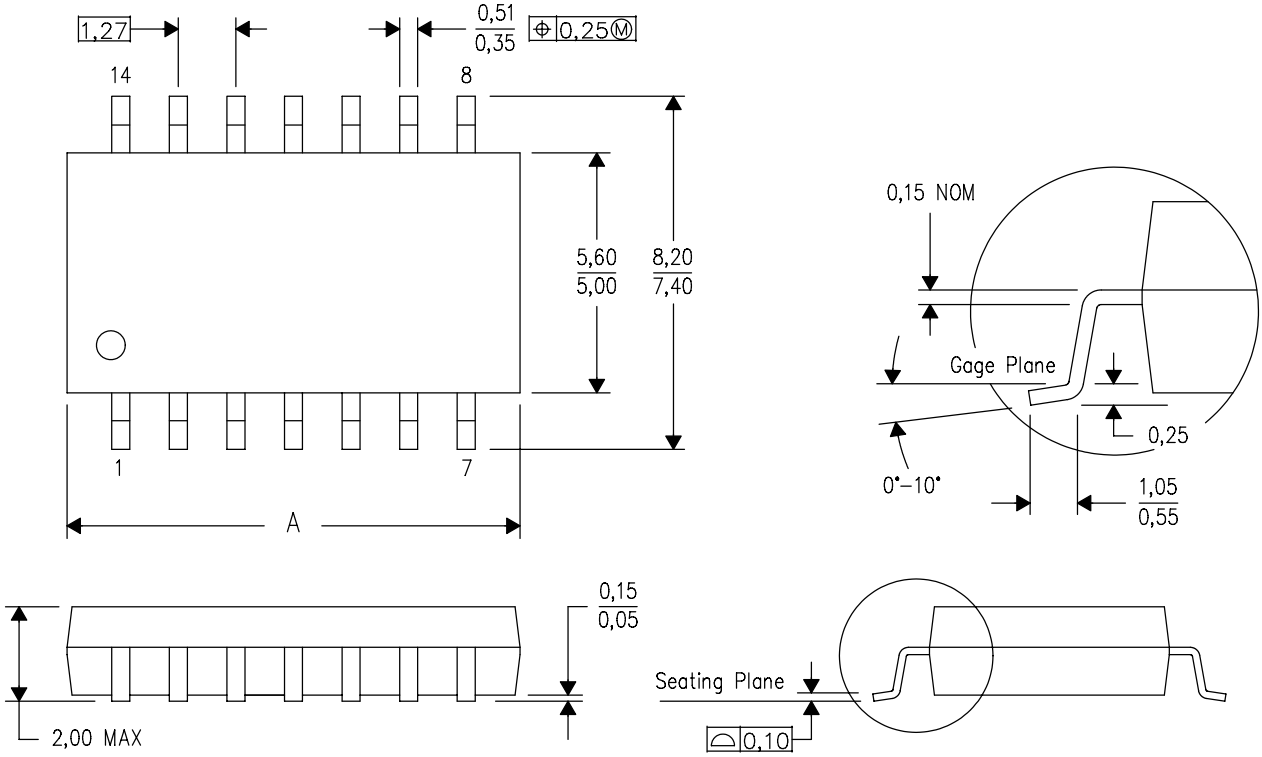


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.