TL77xxA Supply-Voltage Supervisors

1 Features

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Wide Supply-Voltage Range
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- Externally Adjustable Pulse Duration

2 Applications

- Computers
- Tablets
- Smart Phones
- Servers
- Music Players

3 Description

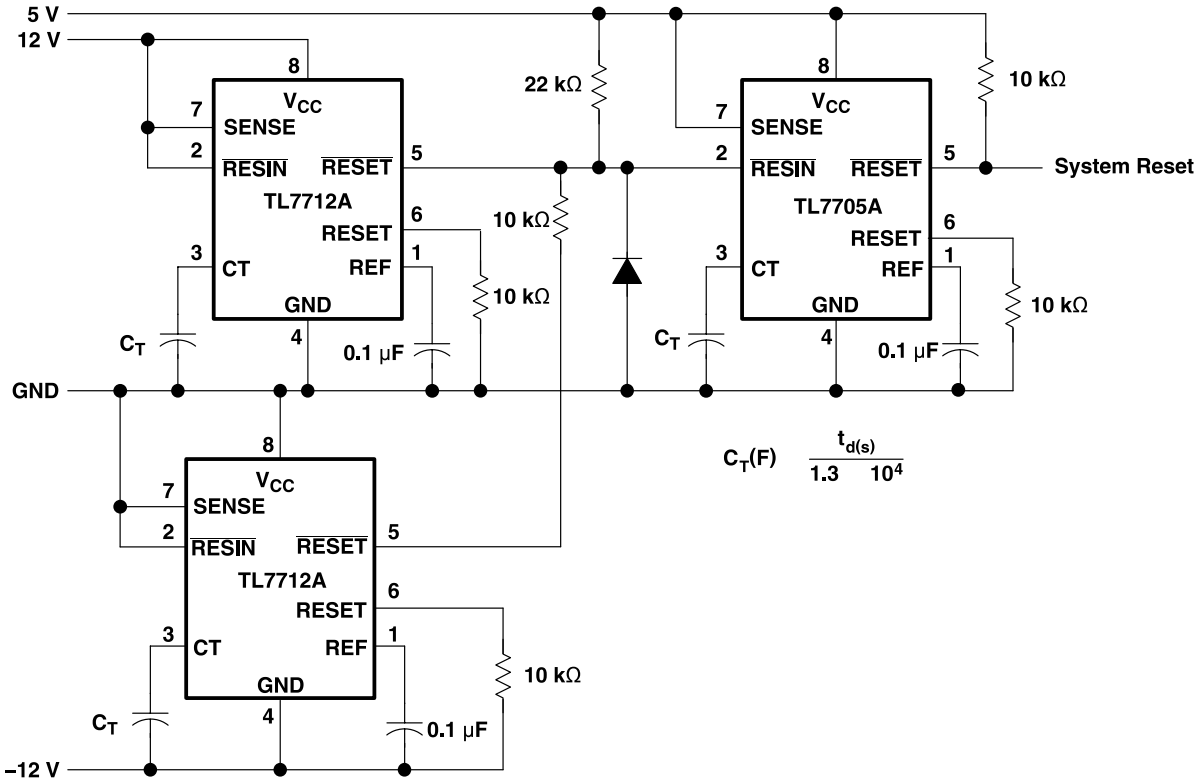
The TL77xxA family of integrated-circuit supply-voltage supervisors is designed specifically for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 3.6 V. At this point (assuming that SENSE is above V_{IT+}), the delay timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, $\overline{\text{RESET}}$ and RESET go active.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL77xxA	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm
TL7705A	SO (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Three-Supply Monitoring



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (January 2015) to Revision K — **Page**

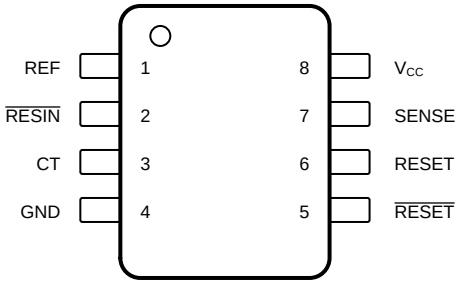
- Added SO (8) to *Device Information* table ... 1
- Changed RESET to $\overline{\text{RESET}}$ in *Timing Diagram* ... 6
- Added *Receiving Notification of Documentation Updates* section ... 15

Changes from Revision I (July 2009) to Revision J — **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1

5 Pin Configuration and Functions

TL7702A, TL7709A, TL77012A, TL7715A D or P Package
TL7705A D, P, or PS Package
8-Pin SOIC, PDIP, or SO
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CT	3	I/O	External timing-capacitor pin
GND	4	—	Device ground
REF	1	O	Voltage reference output
RESET	6	O	Supervisor reset signal output
$\overline{\text{RESET}}$	5	O	Supervisor reset signal output (inverted)
$\overline{\text{RESIN}}$	2	I	Reset input
SENSE	7	I	Sense input
V_{CC}	8	—	Power Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage (2)			20	V
V_I	Input voltage, $\overline{RESIN}$		–0.3	20	V
V_I	Input voltage range SENSE	TL7702A (3)	–0.3	6	V
		TL7705A	–0.3	20	V
		TL7709A	–0.3	20	V
		TL7712A, TL7715A	–0.3	20	V
I_{OH}	High-level output current, I_{OH}, RESET			–30	mA
I_{OL}	Low-level output current, I_{OL}, $\overline{RESET}$			30	mA
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply Voltage		3.5	18	V
V_{IH}	High-level input voltage at $\overline{RESIN}$		2		V
V_{IL}	Low-level input voltage at $\overline{RESIN}$			0.6	V
V_I	Input voltage, SENSE	TL7702A	0	See (1)	V
		TL7705A	0	10	
		TL7709A	0	15	
		TL7712A	0	20	
		TL7715A	0	20	
I_{OH}	High-level output current, RESET			–16	mA
I_{OL}	Low-level output current, $\overline{RESET}$			16	mA
T_A	Operating free-air temperature	TL77xxAC	0	70	°C
		TL77xxAI	–40	85	

(1) For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_{CC} − 1 V or 6 V, whichever is less.

6.4 Thermal Information

THERMAL METRIC[1]		TL77xxA			UNIT
		D	P	PS	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	85	95	°C/W

report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS[1]	TL77xxAC TL77xxAI			UNIT
					MIN	TYP	MAX	
V_{OH}	High-level output voltage, RESET			I_{OH} = –16 mA	V_{CC} – 1.5			V
V_{OL}	Low-level output voltage, $\overline{\text{RESET}}$			I_{OL} = 16 mA			0.4	V
V_{ref}	Reference Voltage			T_A = 25°C	2.48	2.53	2.58	V
V_{IT-}	Negative-going input threshold voltage, SENSE	TL7702A		T_A = 25°C	2.48	2.53	2.58	V
		TL7705A			4.5	4.55	4.6	
		TL7709A			7.5	7.6	7.7	
		TL7712A			10.6	10.8	11	
		TL7715A			13.2	13.5	13.8	
V_{hys}	Hysteresis, SENS (V_{IT+} – V_{IT-})	TL7702A		T_A = 25°C		10		mV
		TL7705A				15		
		TL7709A				20		
		TL7712A				35		
		TL7715A				45		
I_I	Input current	$\overline{\text{RESIN}}$		V_I = 2.4 V to V_{CC}			20	µA
				V_I = 0.4 V			–100	
		SENSE	TL7702A	$V_{ref} < V_I < V_{CC}$ – 1.5 V		0.5	2	
I_{OH}	High-level output current, $\overline{\text{RESET}}$			V_O = 18 V			50	µA
I_{OL}	Low-level output current, RESET			V_O = 0			–50	µA
I_{CC}	Supply current			All inputs and outputs open		1.8	3	mA

(1) All electrical characteristics are measured with 0.1-µF capacitors connected at REF, CT, and V_{CC} to GND.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS[1]	TL77xxAC TL77xxAI			UNIT
				MIN	TYP	MAX	
	Output pulse duration		CT = 0.1 µF	0.65	1.2	2.6	msec
	Input pulse duration at $\overline{\text{RESIN}}$			0.4			µs
$t_{w(S)}$	Pulse duration at sense input to switch outputs		$V_{IH} = V_{IT-}$ + 200 mV, $V_{IL} = V_{IT-}$ − 200 mV	2			µs
t_{pd}	propagation delay time, $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$		V_{CC} = 5V			1	µs
t_r	Rise time	RESET	V_{CC} = 5 V[2]			0.2	µs
		$\overline{\text{RESET}}$				3.5	
t_f	Fall time	RESET	V_{CC} = 5 V[2]			3.5	µs
		$\overline{\text{RESET}}$				0.2	

(1) All switching characteristics are measured with 0.1-µF capacitors connected at REF and V_{CC} to GND.
(2) The rise and fall times are measured with a 4.7-kΩ load resistor at RESET and $\overline{\text{RESET}}$.

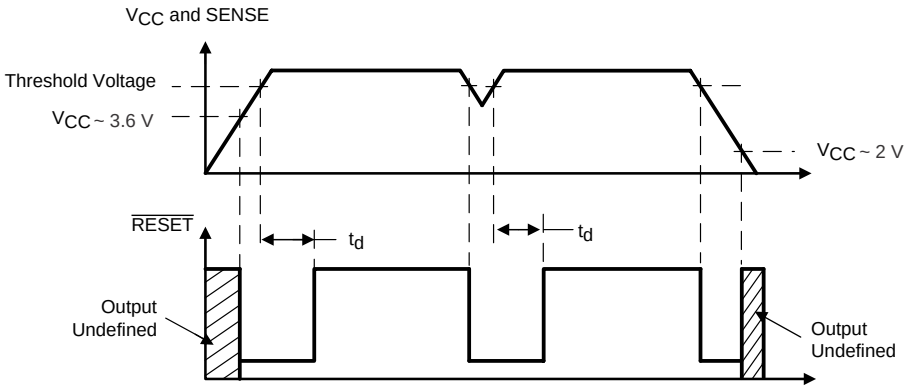


Figure 1. Timing Diagram

6.7 Typical Characteristics

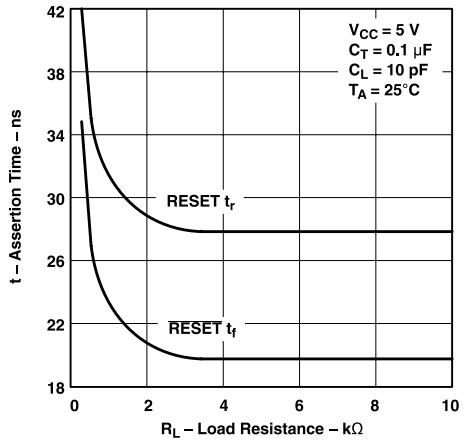


Figure 2. Assertion Time vs Load Resistance

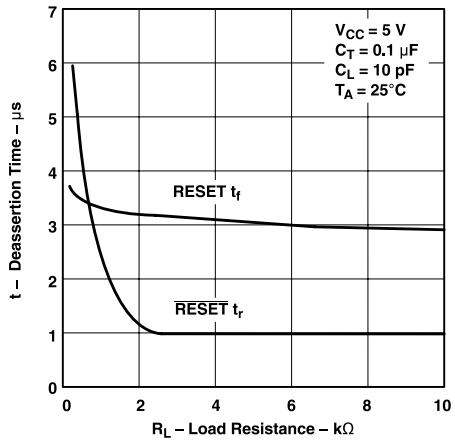


Figure 3. Deassertion Time vs Load Resistance

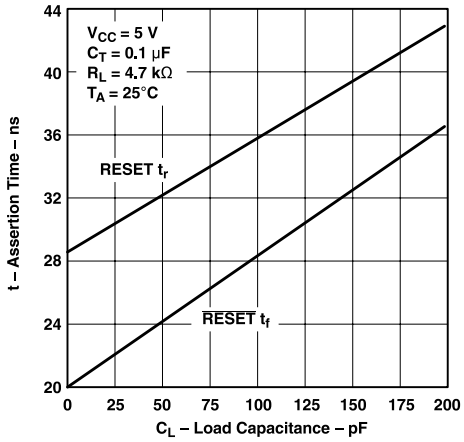


Figure 4. Assertion Time vs Load Capacitance

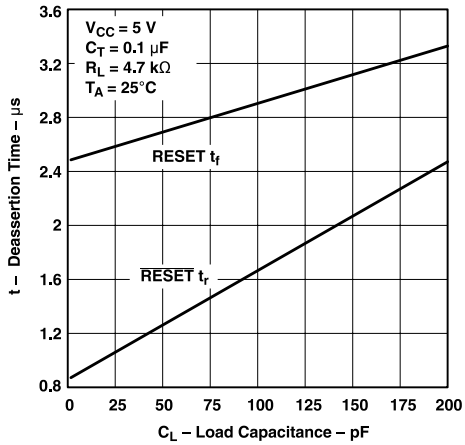


Figure 5. De-assertion Time vs Load Capacitance

7 Parameter Measurement Information

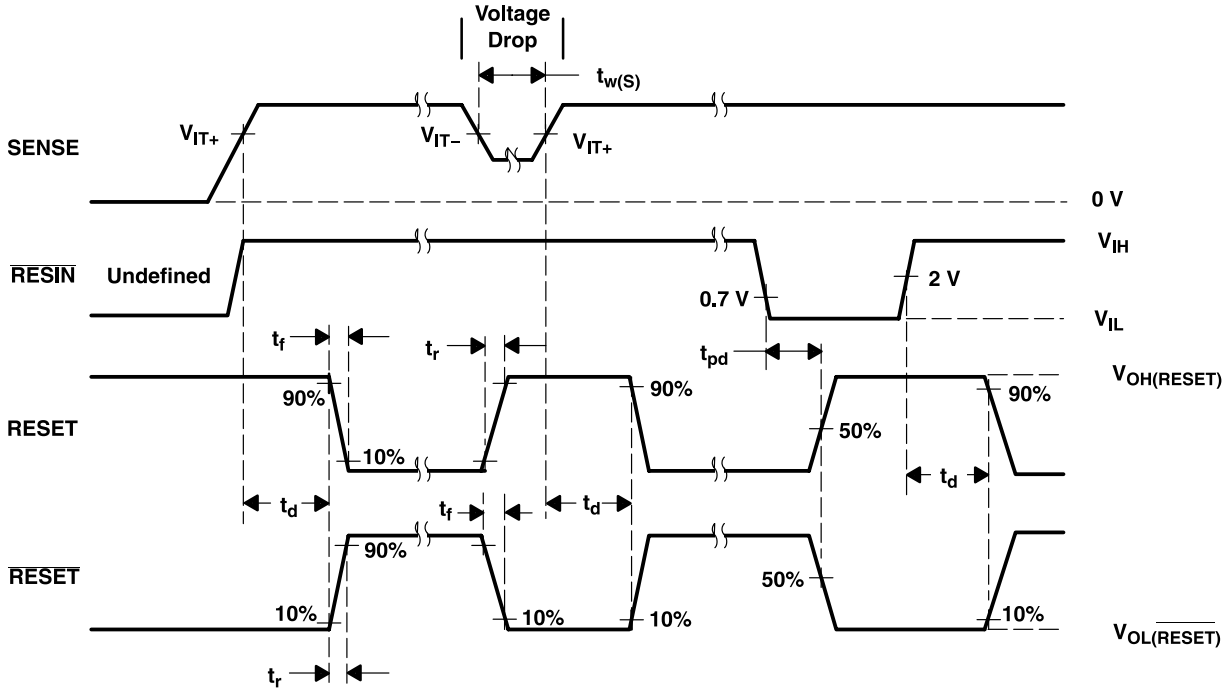


Figure 6. Voltage Waveform

8 Detailed Description

8.1 Overview

The TL77xxA family of integrated-circuit supply-voltage supervisors is designed specifically for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the $\overline{\text{RESET}}$ output becomes active (low) when V_{CC} attains a value approaching 3.6 V. At this point (assuming that SENSE is above V_{IT+}), the delay timer function activates a time delay, after which outputs $\overline{\text{RESET}}$ and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation, $\overline{\text{RESET}}$ and RESET go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value.

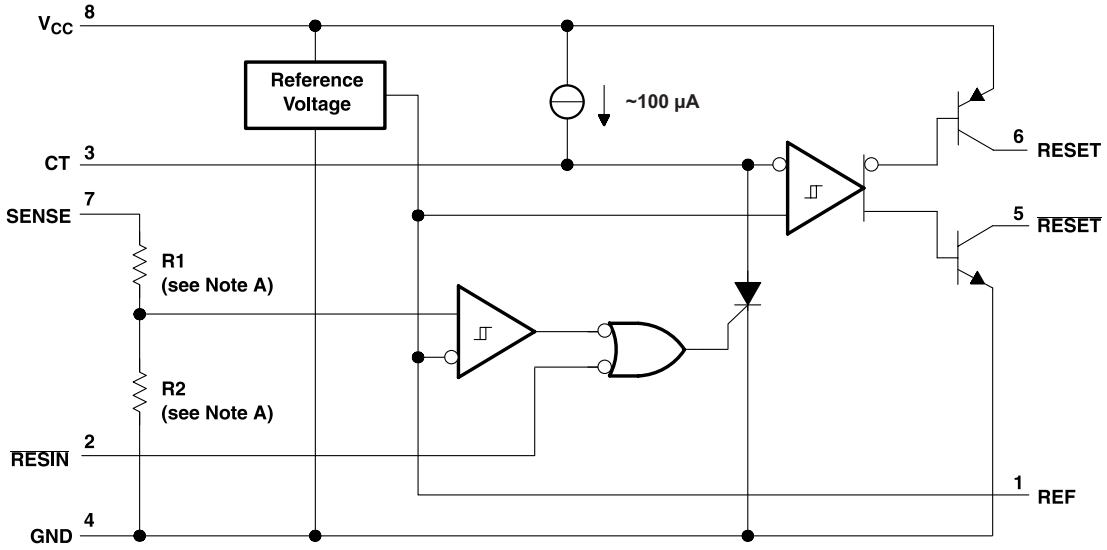
During power down and when SENSE is below V_{IT-}, the outputs remain active until V_{CC} falls below 2 V. After this, the outputs are undefined. An external capacitor (typically 0.1 μF) must be connected to REF to reduce the influence of fast transients in the supply voltage.

Five versions of this circuit are available:

- TL7705A (Vt = 4.55 V): Application in TTL-systems and microcomputer systems which require a 5 volt supply (for example, TMS7000)
- TL7709A (Vt = 7.6 V): Application in microcomputer systems using the TMS1XXXNLL
- TL7712A (Vt = 10.8 V): Application in CMOS, microprocessor, and memory circuits with a 12 volt supply.
- TL7715A (Vt = 13.5 V): Application in circuits which operate with a supply voltage of 15 V, as is found often in analog circuits.
- TL7702A (Vt = 2.5 V): Application in systems where other supply voltages are used. The required trigger level my be adjusted with an external resistor divider at the SENSE input.

8.2 Functional Block Diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



A. TL7702A: R1 = 0 Ω, R2 = open
TL7705A: R1 = 7.8 kΩ, R2 = 10 kΩ
TL7709A: R1 = 19.7 kΩ, R2 = 10 kΩ
TL7712A: R1 = 32.7 kΩ, R2 = 10 kΩ
TL7715A: R1 = 43.4 kΩ, R2 = 10 kΩ

B. Resistor values shown are nominal.

8.3 Feature Description

8.3.1 Wide Supply-Voltage Range

Th TL77xxA family operates of a wide supply voltage range of 3.5 V to 18 V.

8.3.2 Externally Adjustable Pulse Duration

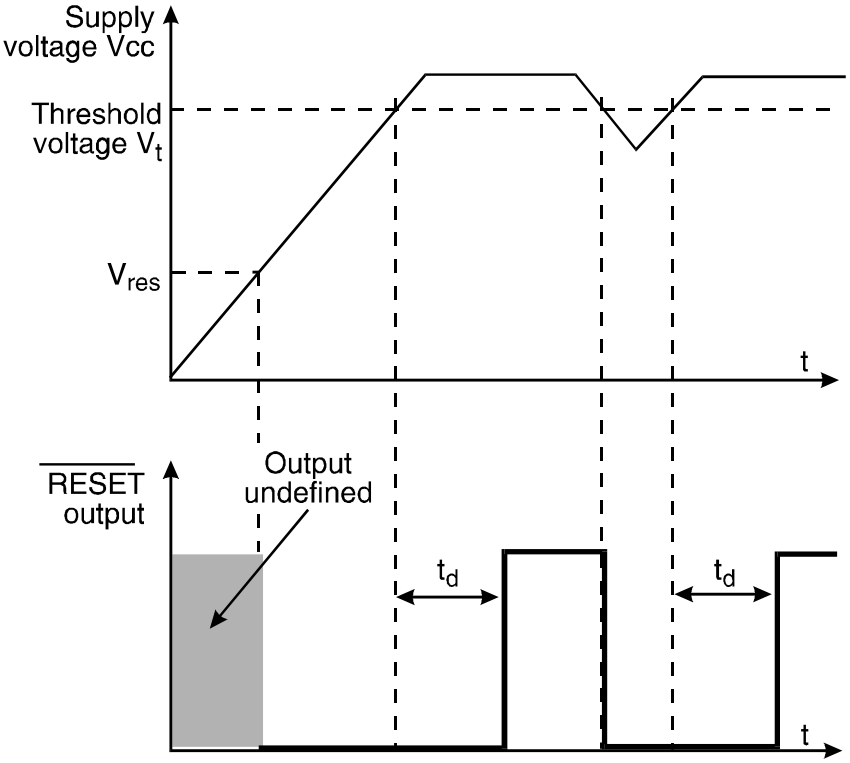
The time delay is determined by the value of the external capacitor C_T: $t_d = 1.3 \times 10^4 \times C_T$, where C_T is in farads (F) and t_d is in seconds (s).

8.3.3 Temperature-Compensated Voltage Reference

The series TL77xxA incorporates an extremely stable reference voltage source. This voltage source can also be used in applications where a constant voltage source is required. The reference voltage varies less than 10 mV over the supply voltage range of 3.5 V to 18 V. The same stability of the reference voltage is maintained, when the ambient temperature is changed. The reference's voltage varies only 16 mV when the ambient temperature is changed from –40°C to +85°C.

8.4 Device Functional Modes

Figure 7 shows the timing of the various signals. In this example the SENSE input is connected to the supply voltage V_{CC} as in typical applications of this device. The minimum supply voltage for which the function of this device is guaranteed is 3.6 V. After power-on, the outputs are undefined until the minimum supply voltage V_{res} is reached. For the TL77xxA the minimum supply voltage is V_{res} = 3 V (typical 2.5 V). Beyond the voltage V_{res} the capacitor C_T is first kept discharged, and the outputs stay in the active state (RESET = High, $\overline{\text{RESET}}$ = Low). When the input voltage becomes higher than the threshold voltage V_t, the thyristor is turned off and the capacitor is charged. After a delay, t_d, the voltage at the capacitor passes the trigger level of the output comparator and the outputs become inactive. The circuit to be initialized is now set to a defined state and starts the correct operation.



A. Note: SENSE Input connected to V_{CC}

Figure 7. Timing Diagram

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This application shows the initialization circuit diagrams for a microprocessor system with supply voltage Vcc = 5 V. The external components required are the decoupling capacitor C_{ref} for the reference voltage and the timing capacitor C_T. The outputs of the TL77xxA are open collector outputs. In Figure 8 therefore a pull-up resistor is shown at the $\overline{\text{RESET}}$ output to ensure the correct HIGH level.

9.2 Typical Application

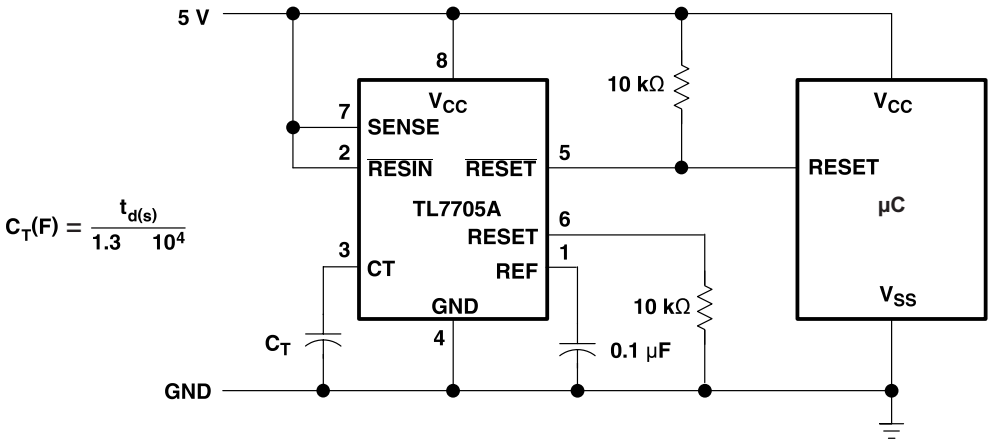


Figure 8. Reset Controller Schematic for a Microprocessor

9.2.1 Design Requirements

- 5-V microprocessor supply voltage
- t_d = 1.3 ms

9.2.2 Detailed Design Procedure

- Select reasonable values for pull-up/pull-down resistors for RESET and $\overline{\text{RESET}}$. This design uses 10 kΩ.
- Choose C_T = 0.1 µF to achieve t_d = 1.3 ms
- This design uses only the active-low reset output ($\overline{\text{RESET}}$) because the example microcontroller resets when the input is Low.

Typical Application (continued)

9.2.3 Application Curves

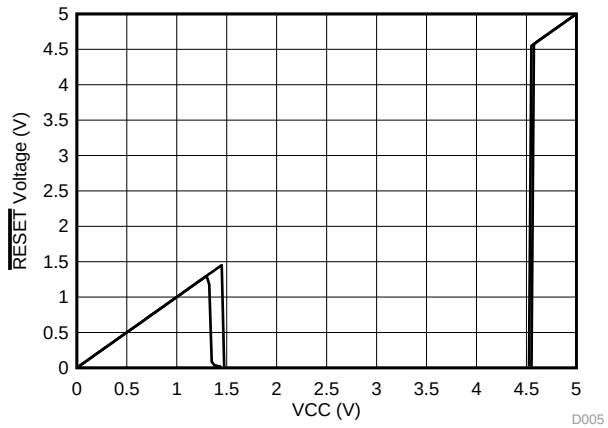


Figure 9. Supervisor $\overline{\text{RESET}}$ Output Voltage vs V_{CC}

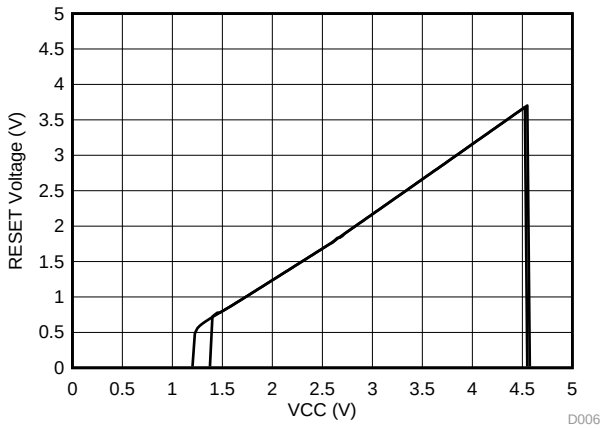


Figure 10. Supervisor RESET Output Voltage vs V_{CC}

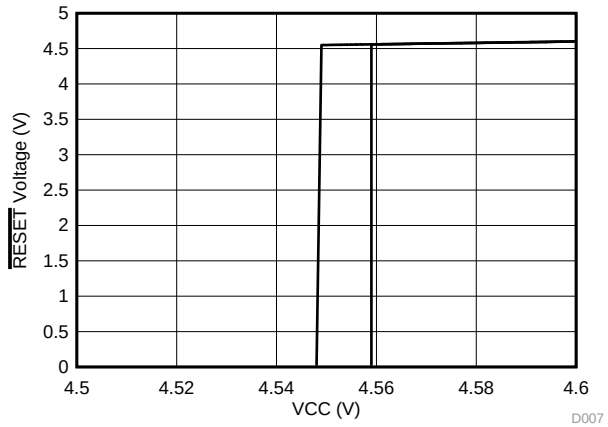


Figure 11. Supervisor $\overline{\text{RESET}}$ Output Voltage vs V_{CC} at Transition

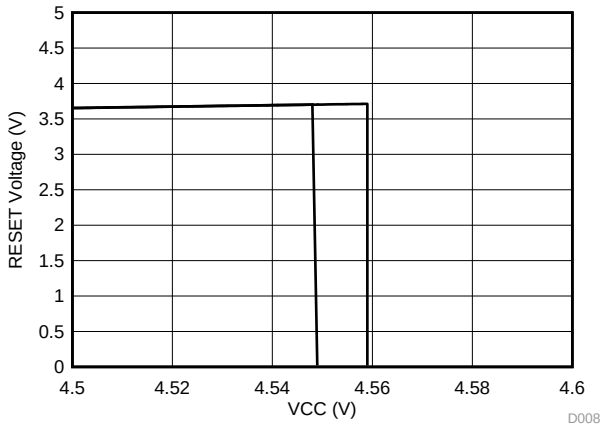


Figure 12. Supervisor RESET Output Voltage vs V_{CC} at Transition

9.3 System Examples

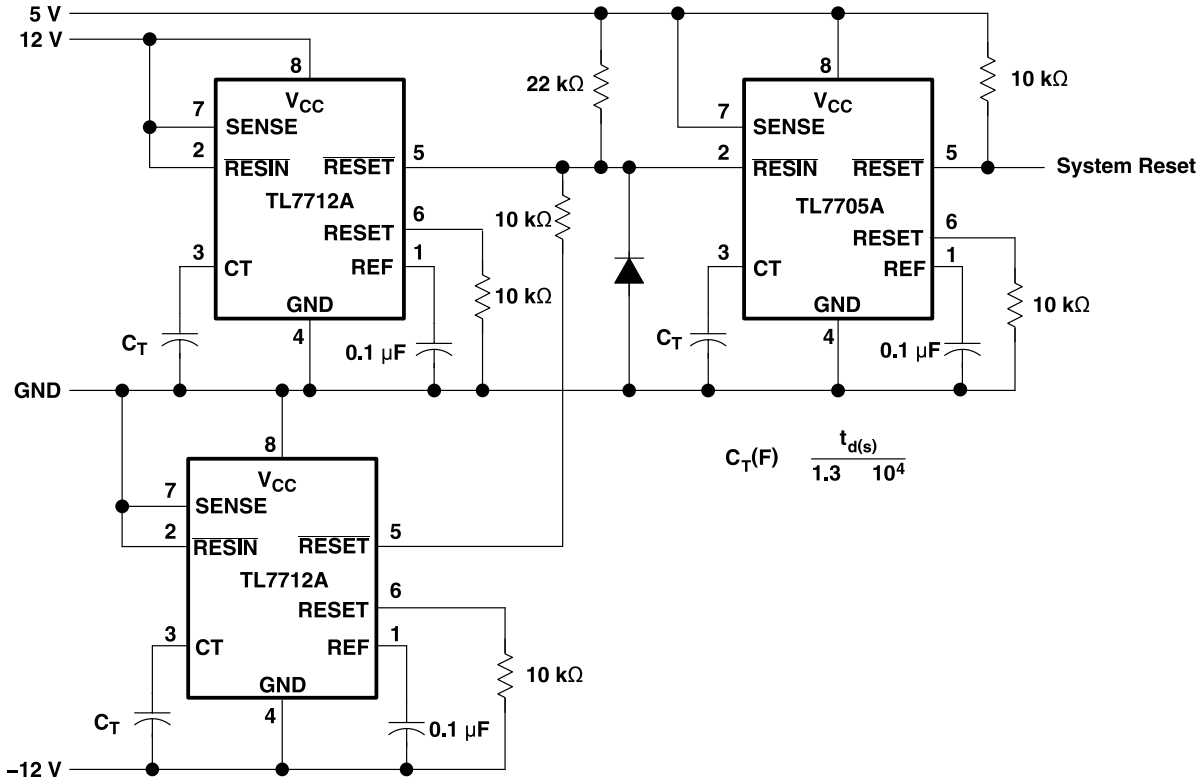


Figure 13. Multi Power-Supply System Reset Generation Schematic

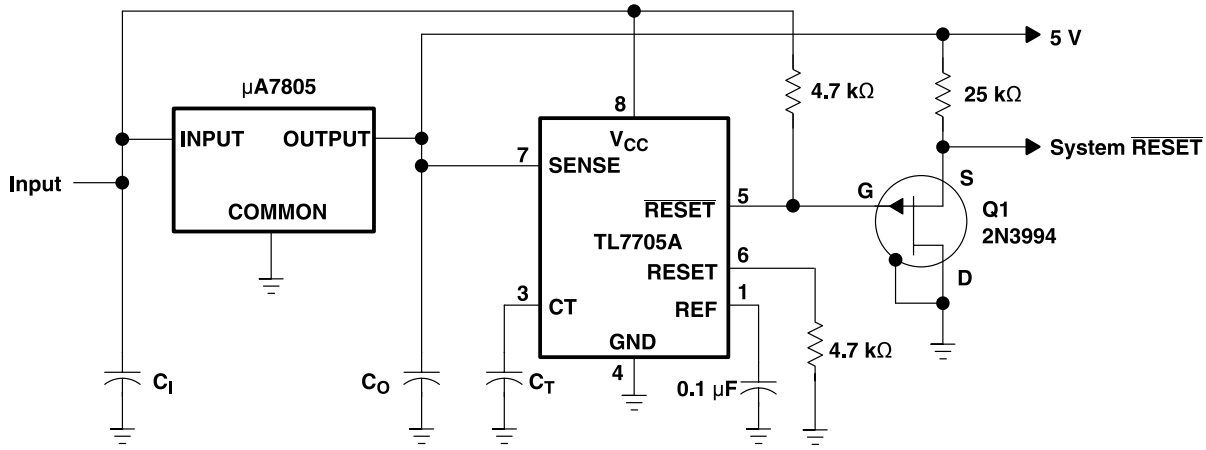


Figure 14. Eliminating Undefined States Using a P-Channel JFET Schematic

System Examples (continued)

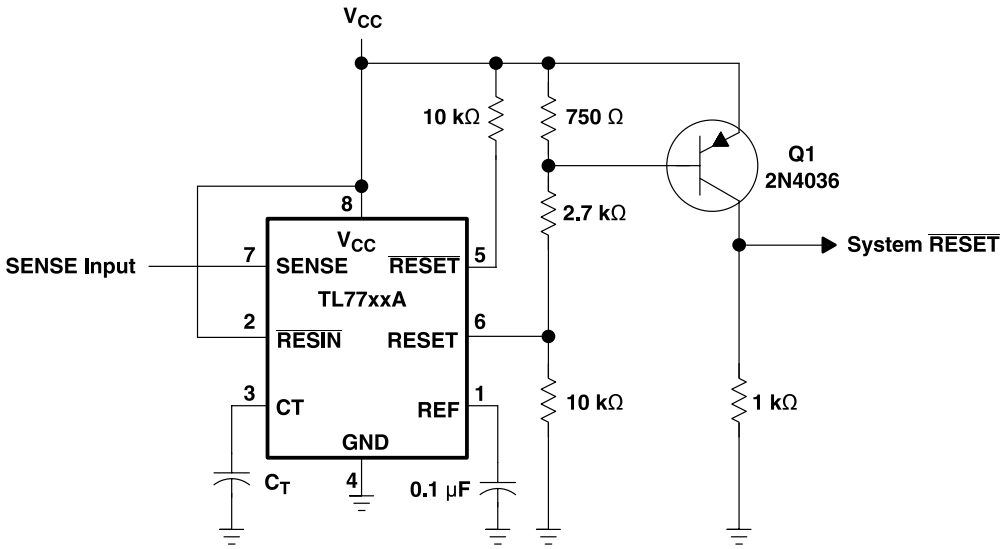


Figure 15. Eliminating Undefined States Using PNP Transistor Schematic

10 Power Supply Recommendations

The TL77xxA devices operate within the specifications from the *Recommended Operating Conditions* between 3.5 V and 18 V.

CAUTION

These devices risk being damaged when powered by more than 20 V.

11 Layout

11.1 Layout Guidelines

The voltage monitor should be placed on the printed circuit board, where there are no neighboring circuits in the which switch high currents (like bus interface circuits and power switches). When laying out the layout of the printed circuit board, take special care with the interconnects which carry analog signals. Beside the SENSE input these are the C_T and V_{ref} terminals. Noise coupled into the C_T input will lead to a reduction of the output pulse width. Noise coupled into the V_{ref} input or into the filter capacitor at this input may lead to undesired triggering of the circuit and by this to an undesired RESET pulse. Practice shows, that this malfunction when high currents flow over the interconnects of these capacitors to the GND terminal of the voltage monitor. To avoid these effects, the GND terminals of these capacitors must be connected by the shortest way to the GND terminal of the voltage monitor in so that no currents caused by other circuits flow over these wires. Figure 16 show a layout proposal for the printed circuit board. Furthermore the resistors of the voltage divider at the SENSE input of the TL7702 (R2 and R3 in Figure 16) have to be placed in so, that no noise may be coupled into this circuit.

11.2 Layout Example

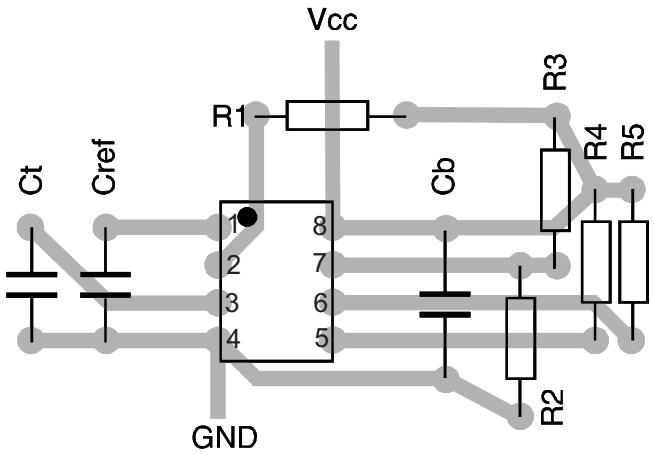
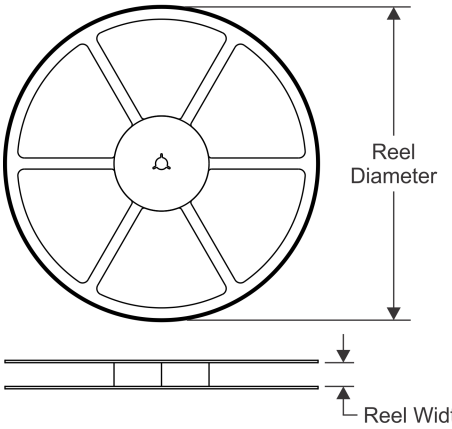


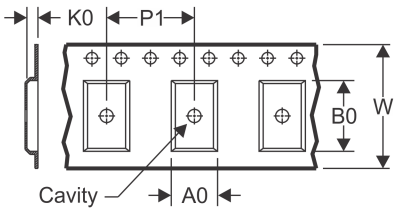
Figure 16. Printed Circuit Layout for the Supply Voltage Supervisor

TAPE AND REEL INFORMATION

REEL DIMENSIONS

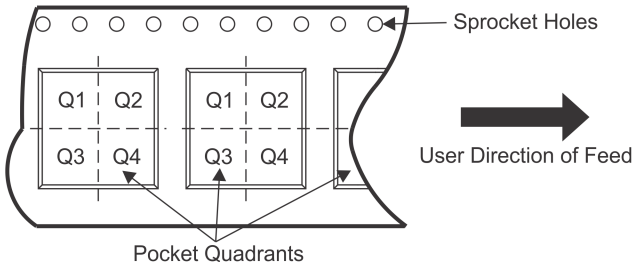


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

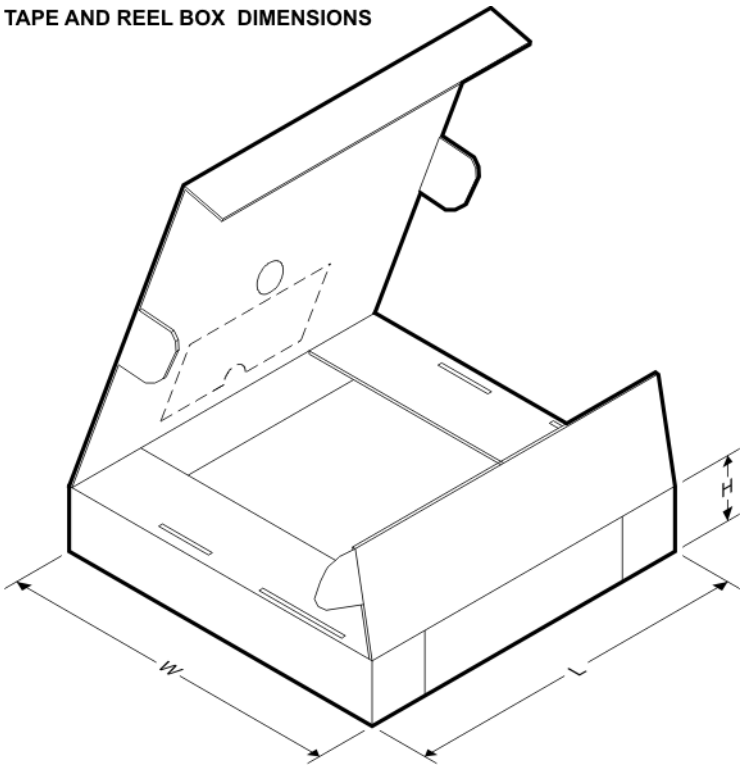
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7702ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7702ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7702AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL7705AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7709ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7712ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7712AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

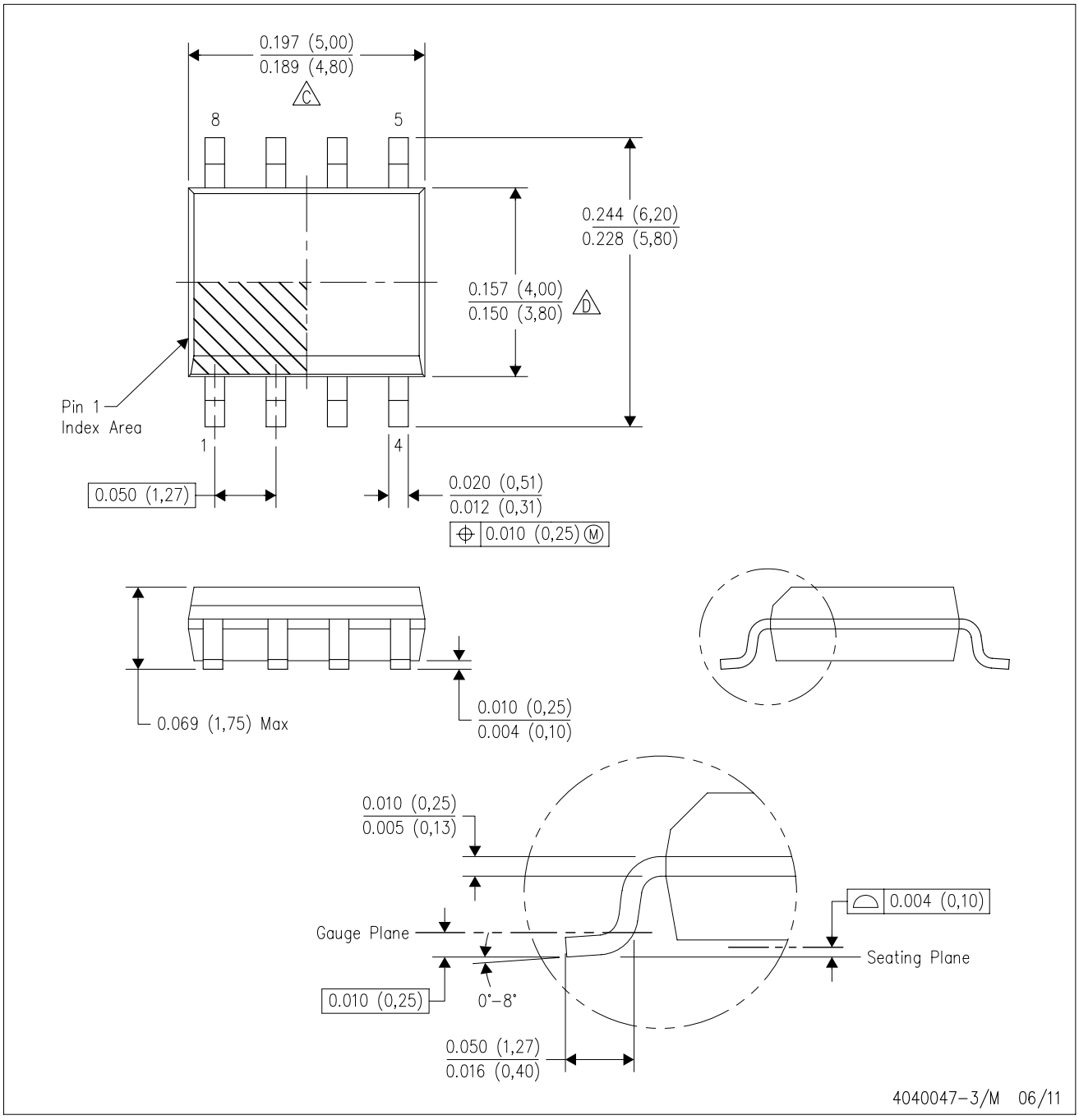
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

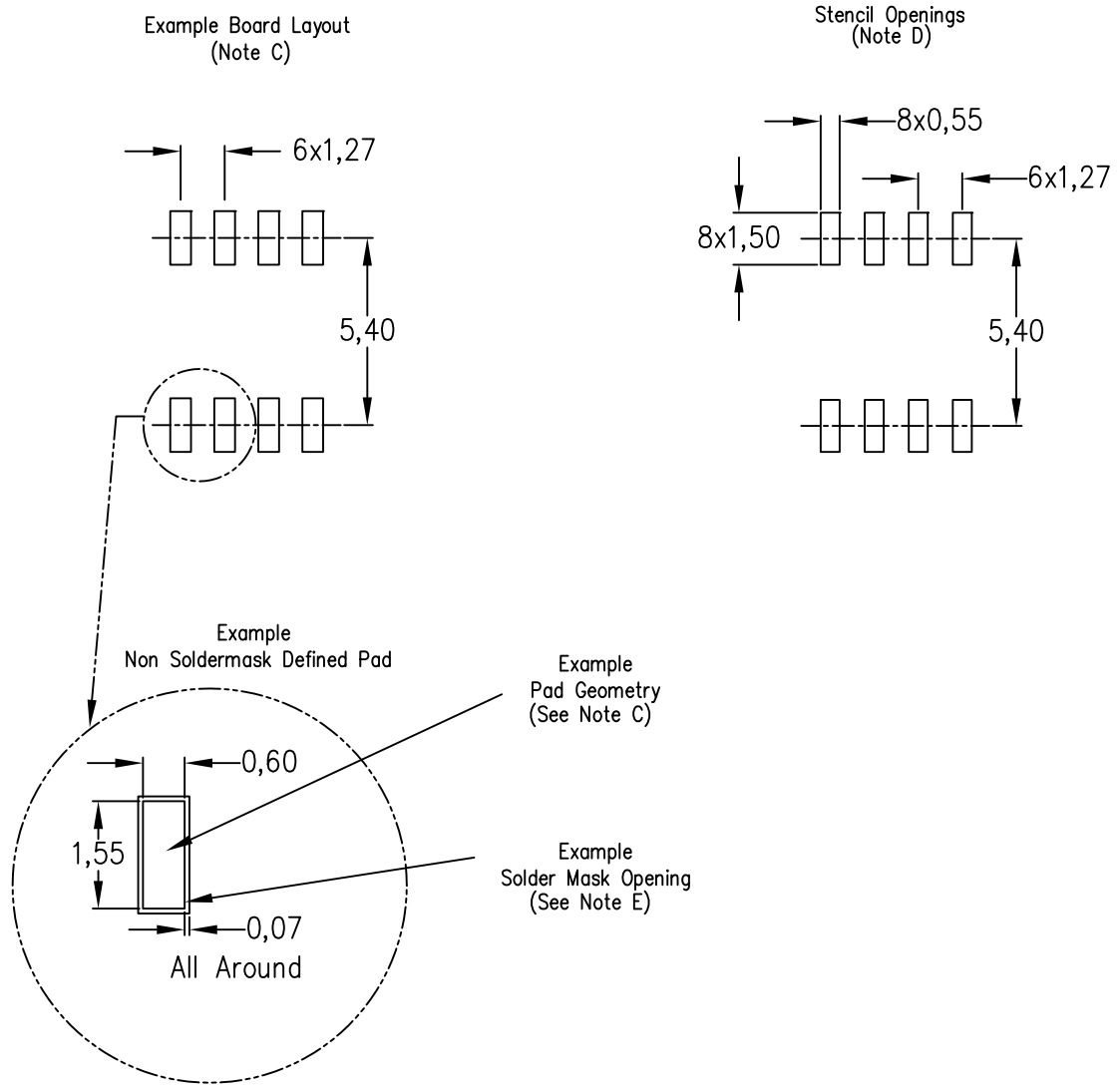
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7702ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7702ACDR	SOIC	D	8	2500	367.0	367.0	35.0
TL7702AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705ACPSR	SO	PS	8	2000	367.0	367.0	38.0
TL7705AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7709ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7712ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7712AIDR	SOIC	D	8	2500	340.5	338.1	20.6

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

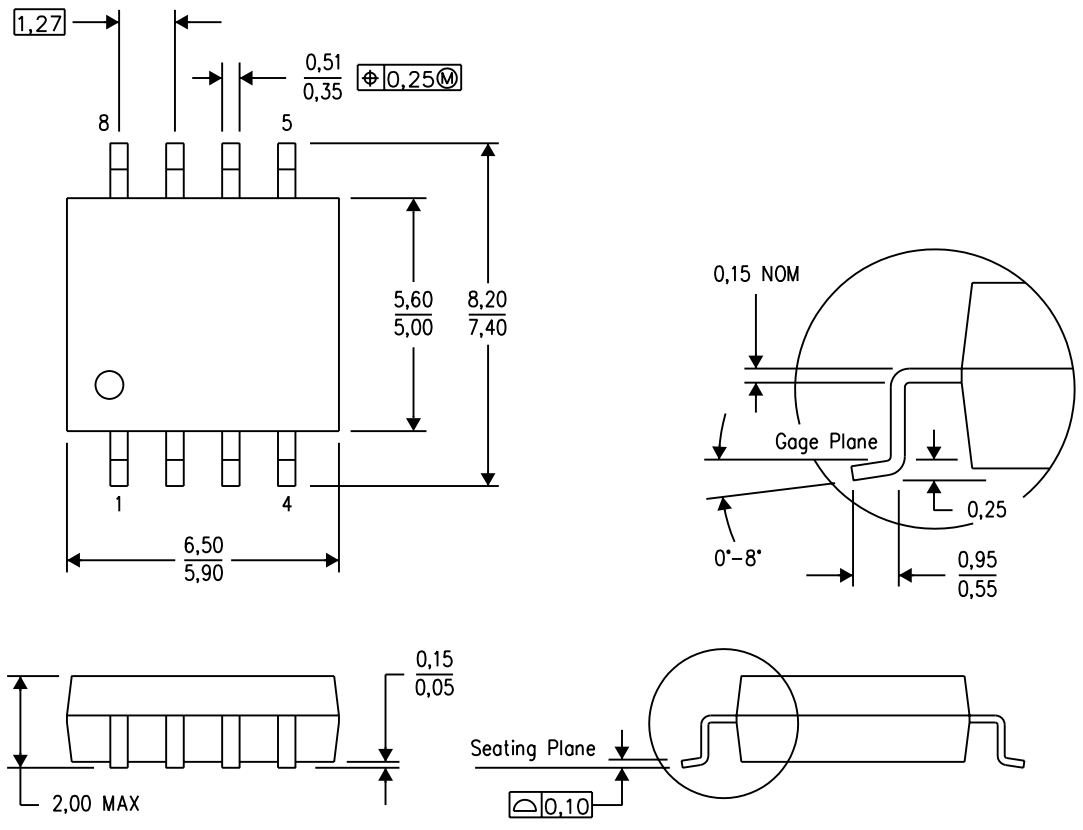
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



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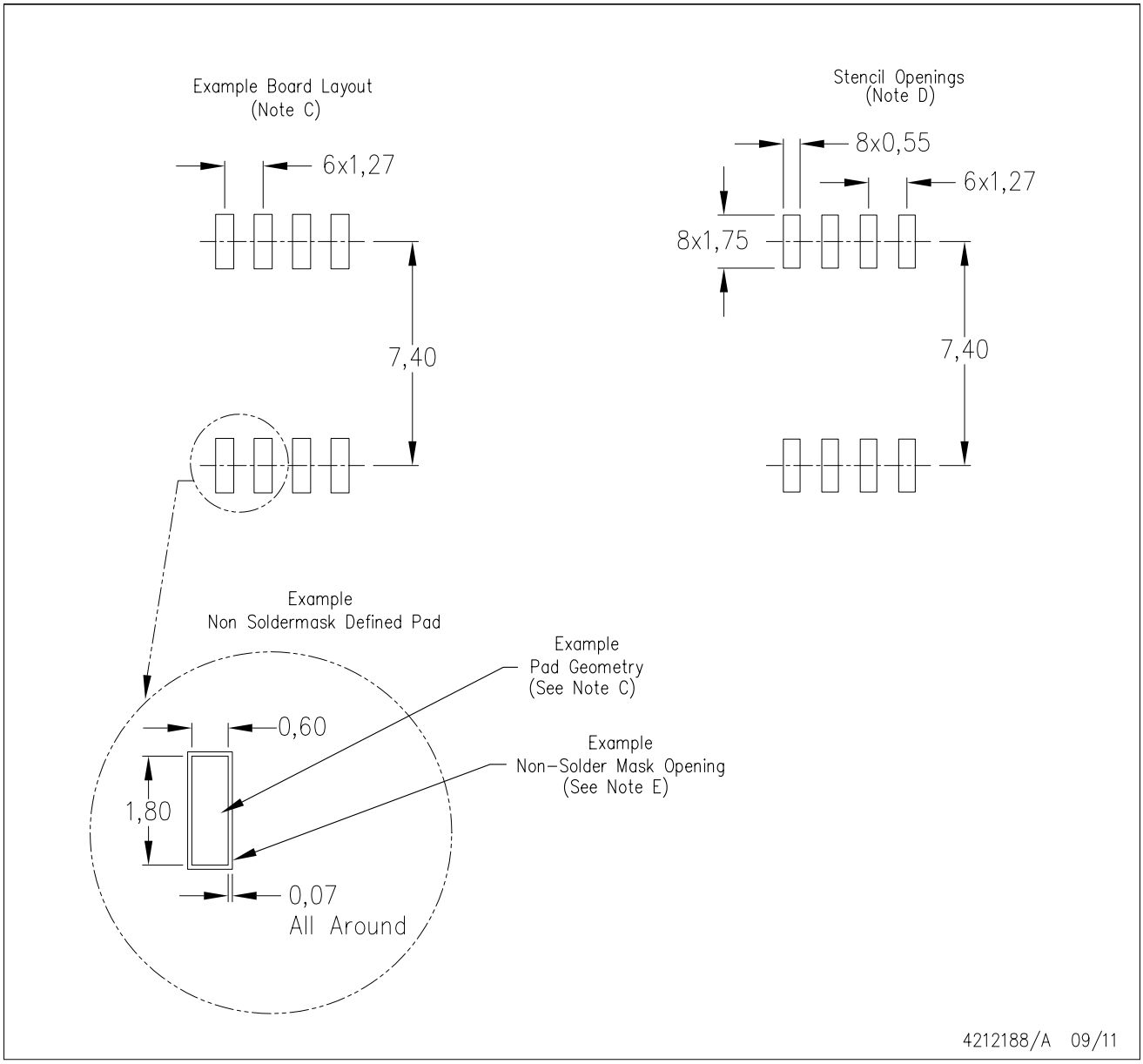
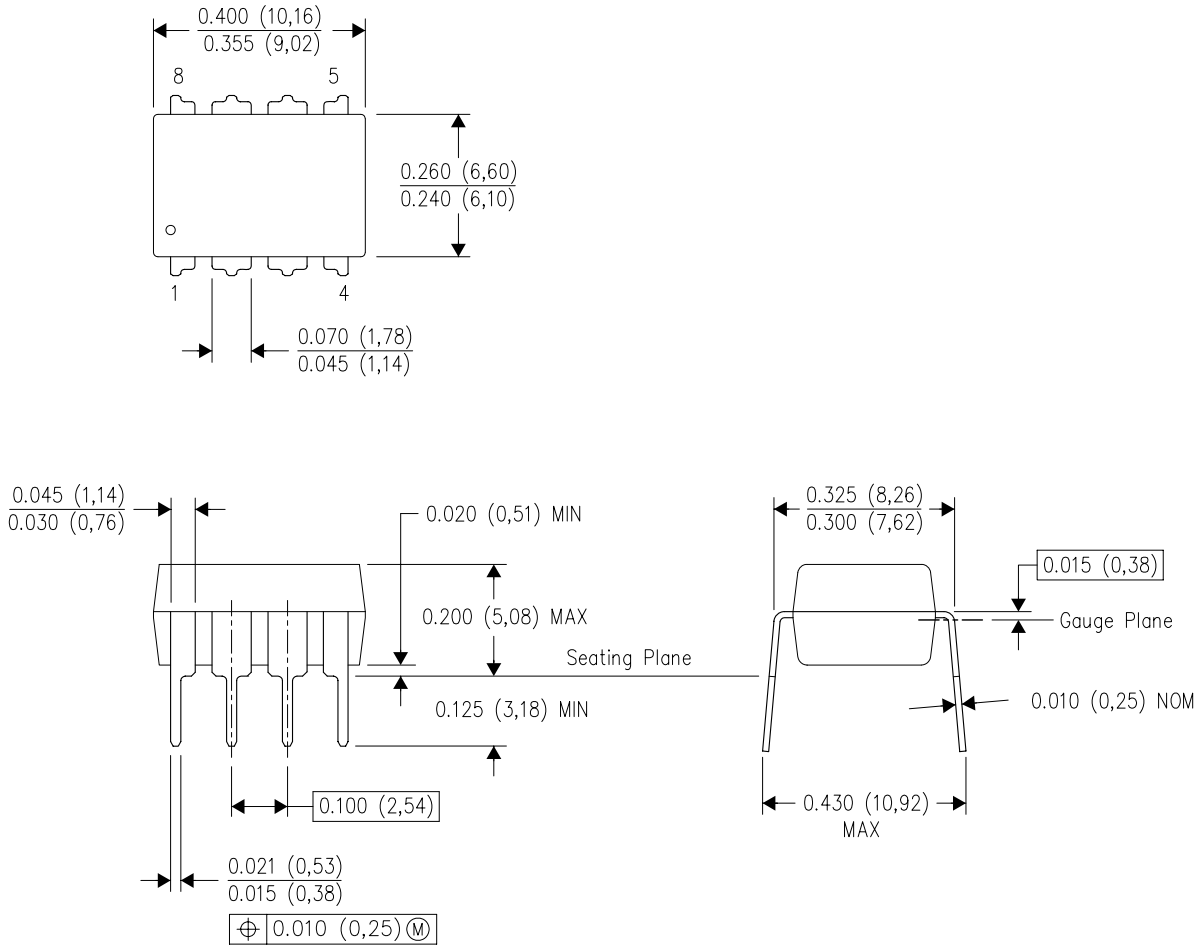
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.