

TLC227x, TLC227xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

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- Output Swing Includes Both Supply Rails
- Low Noise . . . 9 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Common-Mode Input Voltage Range Includes Negative Rail
- High-Gain Bandwidth . . . 2.2 MHz Typ
- High Slew Rate . . . 3.6 V/μs Typ
- Low Input Offset Voltage
950 μV Max at T_A = 25°C
- Macromodel Included
- Performance Upgrades for the TS272, TS274, TLC272, and TLC274
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

description

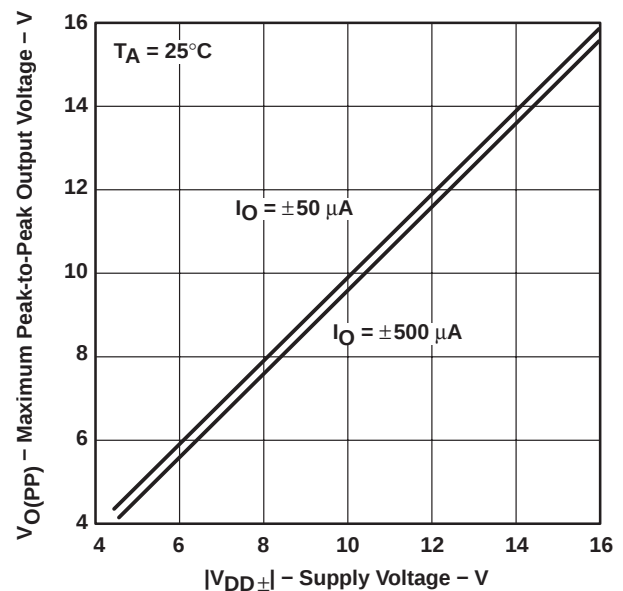
The TLC2272 and TLC2274 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC227x family offers 2 MHz of bandwidth and 3 V/μs of slew rate for higher speed applications. These devices offer comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC227x has a noise voltage of 9 nV/√Hz, two times lower than competitive solutions.

The TLC227x, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC227xA family is available with a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2272/4 also makes great upgrades to the TLC272/4 or TS272/4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices.

If the design requires single amplifiers, see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
VS
SUPPLY VOLTAGE



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TLC2272 AVAILABLE OPTIONS

T _A	V _{IO} max At 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CERAMIC LCC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP‡ (PW)	CERAMIC FLAT PACK (U)
0°C to 70°C	950 µV 2.5 mV	TLC2272ACD TLC2272CD	— —	— —	TLC2272ACP TLC2272CP	TLC2272ACPW TLC2272CPW	— —
–40°C to 125°C	950 µV 2.5 mV	TLC2272AID TLC2272ID	— —	— —	TLC2272AIP TLC2272IP	— TLC2272IPW	— —
	950 µV 2.5 mV	TLC2272AQD TLC2272QD	— —	— —	—	TLC2272AQPW TLC2272QPW	— —
–55°C to 125°C	950 µV 2.5 mV	TLC2272AMD TLC2272MD	TLC2272AMFK TLC2272MFK	TLC2272AMJG TLC2272MJG	TLC2272AMP TLC2272MP	—	TLC2272AMU TLC2272MU

† The D packages are available taped and reeled. Add R suffix to the device type (e.g., TLC2272CDR).

‡ The PW package is available taped and reeled. Add R suffix to the device type (e.g., TLC2272PWR).

§ Chips are tested at 25°C.

TLC2274 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CERAMIC LCC (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP‡ (PW)	CERAMIC FLAT PACK (W)
0°C to 70°C	950 µV 2.5 mV	TLC2274ACD TLC2274CD	—	—	TLC2274ACN TLC2274CN	TLC2274ACPW TLC2274CPW	—
–40°C to 125°C	950 µV 2.5 mV	TLC2274AID TLC2274ID	—	—	TLC2274AIN TLC2274IN	TLC2274AIPW TLC2274IPW	—
	950 µV 2.5 mV	TLC2274AQD TLC2274QD	—	—	—	—	—
–55°C to 125°C	950 µV 2.5 mV	TLC2274AMD TLC2274MD	TLC2274AMFK TLC2274MFK	TLC2274AMJ TLC2274MJ	TLC2274AMN TLC2274MN	—	TLC2274AMW TLC2274MW

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2274CDR).

‡ The PW package is available taped and reeled.

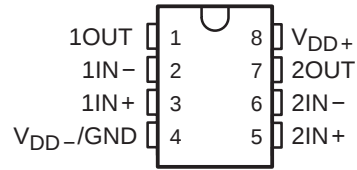
§ Chips are tested at 25°C.

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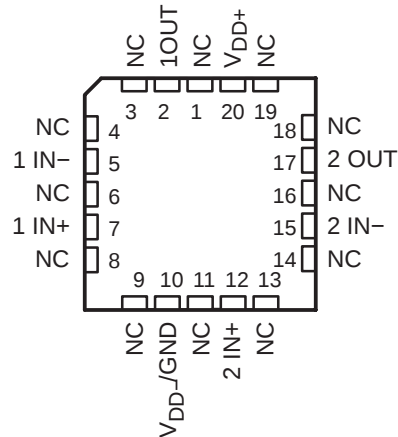
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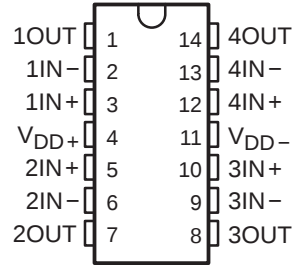
TLC2272
D, JG, P, OR PW PACKAGE
(TOP VIEW)



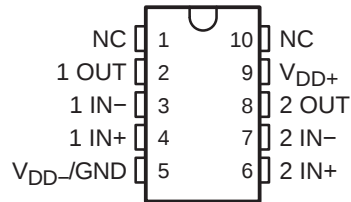
TLC2272
FK PACKAGE
(TOP VIEW)



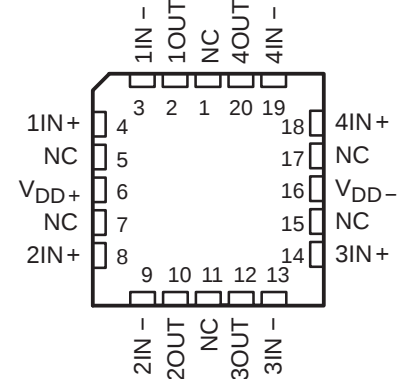
TLC2274
D, J, N, PW, OR W PACKAGE
(TOP VIEW)



TLC2272
U PACKAGE
(TOP VIEW)



TLC2274
FK PACKAGE
(TOP VIEW)

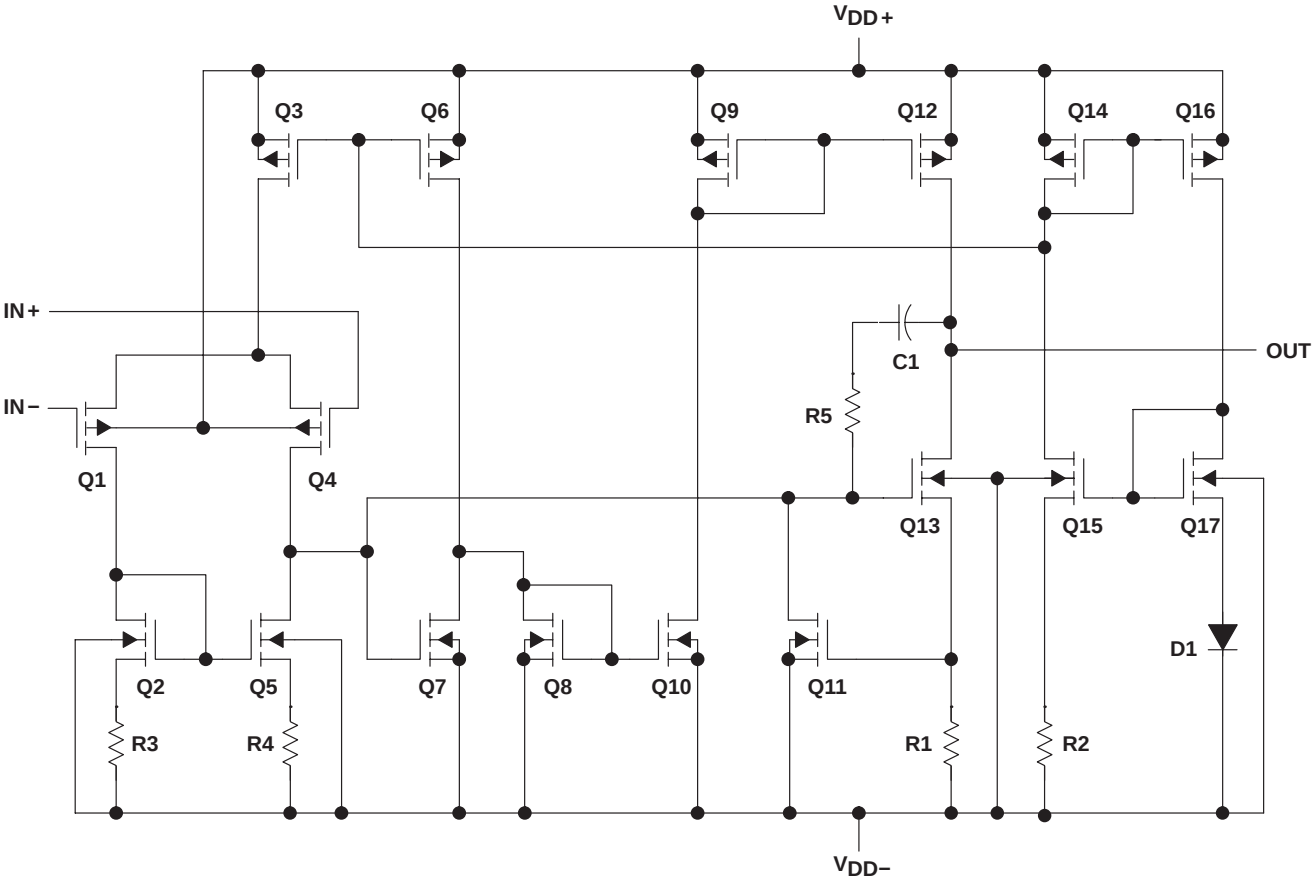


NC – No internal connection

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equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLC2272	TLC2274
Transistors	38	76
Resistors	26	52
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage range, V_I (any input, see Note 1)	$V_{DD-} - 0.3 \text{ V}$ to V_{DD+}
Input current, I_I (any input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5):	
D package (8 pin)	97.1°C/W
D package (14 pin)	86.2°C/W
N package	79.7°C/W
P package	84.6°C/W
PW package (8 pin)	149°C/W
PW package (14 pin)	113°C/W
Package thermal impedance, θ_{JC} (see Notes 4 and 5):	
FK package	5.6°C/W
J package	15.1°C/W
U package	14.7°C/W
Operating free-air temperature range, T_A :	
C suffix	0°C to 70°C
I, Q suffix	–40°C to 125°C
M suffix	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P or PW package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or U package	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current will flow if input is brought below $V_{DD-} - 0.3 \text{ V}$.
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
 4. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 5. The package thermal impedance is calculated in accordance with JESD 51-7 (plastic) or MIL-STD-883 Method 1012 (ceramic).

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage, V_I	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Operating free-air temperature, T_A	0	70	–40	125	–40	125	–55	125	°C

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TLC2272C electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2272C			TLC2272AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0\text{ V}$, $V_{DD} \pm \pm 2.5\text{ V}$, $V_O = 0\text{ V}$, $R_S = 50\ \Omega$	25°C	300	2500		300	950		μV
		Full range		3000			1500		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 70°C	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.002			0.002			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		Full range		100			100		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		Full range		100			100		
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.99			4.99		V
	$I_{OH} = -200\ \mu\text{A}$	25°C	4.85	4.93		4.85	4.93		
		Full range	4.85			4.85			
	$I_{OH} = -1\text{ mA}$	25°C	4.25	4.65		4.25	4.65		
		Full range	4.25			4.25			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01		V
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 5\text{ mA}$	25°C	0.9	1.5		0.9	1.5		
		Full range		1.5			1.5		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega^\ddagger$	25°C	15	35		15	35	V/mV
			Full range	15			15		
		$R_L = 1\text{ m}\Omega^\ddagger$	25°C	175			175		
r_{id} Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i Common-mode input capacitance	$f = 10\text{ kHz}$, P package	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 1\text{ MHz}$, $A_V = 10$	25°C		140			140		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ V to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	75		70	75		dB
		Full range	70			70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C	2.2	3		2.2	3		mA
		Full range		3			3		

† Full range is 0°C to 70°C.

‡ Referenced to 0 V

NOTE 6: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLC2272C operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2272C			TLC2272AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.5\text{ V to }2.5\text{ V}$, $R_L = 10\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C	2.3	3.6		2.3	3.6		V/ μs
		Full range	1.7			1.7			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		50			50		nV/ $\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		9			9		
V_{NPP} Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		1			1		μV
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.4			1.4		
I_n Equivalent input noise current		25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 10\text{ k}\Omega^\ddagger$	$A_V = 1$		0.0013%			0.0013%		
		$A_V = 10$		0.004%			0.004%		
		$A_V = 100$		0.03%			0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		2.18		2.18		MHz
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $A_V = 1$, $R_L = 10\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		1			1		MHz
t_s Settling time	$A_V = -1$, Step = $0.5\text{ V to }2.5\text{ V}$, $R_L = 10\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	To 0.1%	25°C	1.5		1.5			μs
		To 0.01%		2.6		2.6			
ϕ_m Phase margin at unity gain	$R_L = 10\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		50°			50°		
Gain margin		25°C		10			10		dB

† Full range is 0°C to 70°C.

‡ Referenced to 0 V

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TLC2272C electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2272C			TLC2272AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω		25°C	300	2500		300	950	μV	
	Full range			3000			1500				
αV _{IO}	Temperature coefficient of input offset voltage			25°C to 70°C	2			2			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.002			0.002			μV/mo
I _{IO}	Input offset current			25°C	0.5	60		0.5	60	pA	
				Full range	100			100			
I _{IB}	Input bias current			25°C	1	60		1	60	pA	
				Full range	100			100			
V _{ICR}	Common-mode input voltage	R _S = 50 Ω, V _{IO} ≤ 5 mV		25°C	–5 to 4	–5.3 to 4.2		–5 to 4	–5.3 to 4.2	V	
				Full range	–5 to 3.5			–5 to 3.5			
V _{OM+}	Maximum positive peak output voltage	I _O = –20 μA		25°C	4.99			4.99			V
		I _O = –200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I _O = –1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V _{OM–}	Maximum negative peak output voltage	V _{IC} = 0 V, I _O = 50 μA		25°C	–4.99			–4.99			V
		V _{IC} = 0 V, I _O = 500 μA		25°C	–4.85	–4.91		–4.85	–4.91		
				Full range	–4.85			–4.85			
		V _{IC} = 0 V, I _O = 5 mA		25°C	–3.5	–4.1		–3.5	–4.1		
				Full range	–3.5			–3.5			
A _{VD}	Large-signal differential voltage amplification	V _O = ±4 V	R _L = 10 kΩ	25°C	25	50		25	50	V/mV	
			R _L = 1 mΩ	Full range	25			25			
					25°C	300			300		
r _{id}	Differential input resistance			25°C	10 ¹²			10 ¹²			Ω
r _i	Common-mode input resistance			25°C	10 ¹²			10 ¹²			Ω
c _i	Common-mode input capacitance	f = 10 kHz,	P package	25°C	8			8			pF
z _o	Closed-loop output impedance	f = 1 MHz,	A _V = 10	25°C	130			130			Ω
CMRR	Common-mode rejection ratio	V _{IC} = –5 V to 2.7 V, V _O = 0 V, R _S = 50 Ω		25°C	75	80		75	80	dB	
				Full range	75			75			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD±} = 2.2 V to ±8 V, V _{IC} = 0 V, No load		25°C	80	95		80	95	dB	
				Full range	80			80			
I _{DD}	Supply current	V _O = 0 V No load		25°C	2.4	3		2.4	3	mA	
				Full range	3			3			

[†] Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLC2272C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLC2272C			TLC2272AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3\text{ V}$, $C_L = 100\text{ pF}$	$R_L = 10\text{ k}\Omega$	25°C	2.3	3.6		2.3	3.6		V/ μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C		50			50		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C		1			1		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion pulse duration	$V_O = \pm 2.3\text{ V}$, $f = 20\text{ kHz}$, $R_L = 10\text{ k}\Omega$	$A_V = 1$	25°C		0.0011%			0.0011%		
			$A_V = 10$			0.004%			0.004%		
			$A_V = 100$			0.03%			0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 10\text{ k}\Omega$	25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 10\text{ k}\Omega$	$A_V = 1$, $C_L = 100\text{ pF}$	25°C		0.54			0.54		MHz
t_s	Settling time	$A_V = -1$, Step = $-2.3\text{ V to }2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is 0°C to 70°C.

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SLOS190G – FEBRUARY 1997 – REVISED MAY 2004

TLC2274C electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2274C			TLC2274AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD} ± = ±2.5 V, V _O = 0 V, V _{IC} = 0 V, R _S = 50 Ω		25°C	300	2500		300	950	μV	
	Full range			3000			1500				
α _{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C	2			2			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.002			0.002			μV/mo
I _{IO}	Input offset current			25°C	0.5	60		0.5	60	pA	
				Full range	100			100			
I _{IB}	Input bias current			25°C	1	60		1	60	pA	
				Full range	100			100			
V _{ICR}	Common-mode input voltage	R _S = 50 Ω, V _{IO} ≤ 5 mV,		25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2	V	
				Full range	0 to 3.5			0 to 3.5			
V _{OH}	High-level output voltage	I _{OH} = –20 μA		25°C	4.99			4.99			V
		I _{OH} = –200 μA		25°C	4.85	4.93		4.85	4.93		
		I _{OH} = –1 mA		Full range	4.85			4.85			
				25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA		25°C	0.01			0.01			V
		V _{IC} = 2.5 V, I _{OL} = 500 μA		25°C	0.09	0.15		0.09	0.15		
				Full range	0.15			0.15			
		V _{IC} = 2.5 V, I _{OL} = 5 mA		25°C	0.9	1.5		0.9	1.5		
				Full range	1.5			1.5			
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 10 kΩ [‡]	25°C	15	35		15	35	V/mV	
				Full range	15			15			
			R _L = 1 mΩ [‡]	25°C	175			175			
r _{id}	Differential input resistance			25°C	10 ¹²			10 ¹²			Ω
r _i	Common-mode input resistance			25°C	10 ¹²			10 ¹²			Ω
c _i	Common-mode input capacitance	f = 10 kHz,	N package	25°C	8			8			pF
z _o	Closed-loop output impedance	f = 1 MHz,	A _V = 10	25°C	140			140			Ω
CMRR	Common-mode rejection ratio	V _{IC} = 0 V to 2.7 V, V _O = 2.5 V, R _S = 50 Ω		25°C	70	75		70	75	dB	
				Full range	70			70			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} /2, No load		25°C	80	95		80	95	dB	
				Full range	80			80			
I _{DD}	Supply current	V _O = 2.5 V, No load		25°C	4.4	6		4.4	6	mA	
				Full range	6			6			

† Full range is 0°C to 70°C.

‡ Referenced to 0 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274C operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2274C			TLC2274AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 0.5\text{ V to }2.5\text{ V}$, $R_L = 10\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C	2.3	3.6	2.3	3.6		V/ μs
			Full range	1.7		1.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C	50		50			nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	25°C	9		9			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C	1		1			μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	1.4		1.4			
I_n	Equivalent input noise current		25°C	0.6		0.6			fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 10\text{ k}\Omega^\ddagger$	25°C	$A_V = 1$	0.0013%	0.0013%			
				$A_V = 10$	0.004%	0.004%			
				$A_V = 100$	0.03%	0.03%			
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}^\ddagger$	25°C		2.18		2.18		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 10\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		1		1		MHz
t_s	Settling time	$A_V = -1$, Step = $0.5\text{ V to }2.5\text{ V}$, $R_L = 10\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C	To 0.1%	1.5		1.5		μs
				To 0.01%	2.6		2.6		
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		50°		50°		
	Gain margin		25°C		10		10		dB

† Full range is 0°C to 70°C.

‡ Referenced to 0 V

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TLC2274C electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2274C			TLC2274AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	300	2500		300	950		μV
		Full range		3000			1500		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 70°C	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.002			0.002			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		Full range		100			100		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		Full range		100			100		
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2		V
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C		4.99			4.99		V
	$I_O = -200\ \mu\text{A}$	25°C	4.85	4.93		4.85	4.93		
		Full range	4.85			4.85			
	$I_O = -1\text{ mA}$	25°C	4.25	4.65		4.25	4.65		
		Full range	4.25			4.25			
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0\text{ V}, I_O = 50\ \mu\text{A}$	25°C		-4.99			-4.99		V
		25°C	-4.85	-4.91		-4.85	-4.91		
	$V_{IC} = 0\text{ V}, I_O = 500\ \mu\text{A}$	25°C	-4.85	-4.91		-4.85	-4.91		
		Full range	-4.85			-4.85			
	$V_{IC} = 0\text{ V}, I_O = -5\text{ mA}$	25°C	-3.5	-4.1		-3.5	-4.1		
		Full range	-3.5			-3.5			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$	$R_L = 10\text{ k}\Omega$	25°C	25	50	25	50		V/mV
			Full range	25		25			
		$R_L = 1\text{ M}\Omega$	25°C	300		300			
r_{id} Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i Common-mode input capacitance	$f = 10\text{ kHz}, \text{ N package}$	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 1\text{ MHz}, A_V = 10$	25°C		130			130		Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5\text{ V to } 2.7\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	75	80		75	80		dB
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2\text{ V to } \pm 8\text{ V}, V_{IC} = 0\text{ V}, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 0\text{ V}, \text{ No load}$	25°C		4.8	6		4.8	6	mA
		Full range			6			6	

[†] Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2274C			TLC2274AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±2.3 V, C _L = 100 pF R _L = 10 kΩ,		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	50			50			nV/√Hz
		f = 1 Hz		25°C	9			9			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	1			1			μV
		f = 0.1 Hz to 10 Hz		25°C	1.4			1.4			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V, f = 20 kHz, R _L = 10 kΩ	A _V = 1	25°C	0.0011%			0.0011%			
			A _V = 10		0.004%			0.004%			
			A _V = 100		0.03%			0.03%			
	Gain-bandwidth product	f = 10 kHz, C _L = 100 pF	R _L = 10 kΩ,	25°C	2.25			2.25			MHz
BOM	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 10 kΩ,	A _V = 1, C _L = 100 pF	25°C	0.54			0.54			MHz
t _s	Settling time	A _V = −1, Step = −2.3 V to 2.3 V, R _L = 10 kΩ, C _L = 100 pF	To 0.1%	25°C	1.5			1.5			μs
			To 0.01%		3.2			3.2			
φ _m	Phase margin at unity gain	R _L = 10 kΩ, C _L = 100 pF		25°C	52°			52°			
	Gain margin			25°C	10			10			dB

[†] Full range is 0°C to 70°C.

TLC227x, TLC227xA

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TLC2272I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0 V, V _O = 0 V, V _{DD±} = ±2.5 V R _S = 50 Ω		25°C	300	2500		300	950	μV	
	Full range				3000		1500				
α _{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C	2			2		μV/°C	
	Input offset voltage long-term drift (see Note 4)			25°C	0.002			0.002		μV/mo	
I _{IO}	Input offset current			25°C	0.5	60		0.5	60	pA	
				–40°C to 85°C		150		150			
				Full range		800		800			
I _{IB}	Input bias current			25°C	1	60		1	60	pA	
				–40°C to 85°C		150		150			
				Full range		800		800			
V _{ICR}	Common-mode input voltage	R _S = 50 Ω, V _{IO} ≤ 5 mV	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2	V		
			Full range	0 to 3.5		0 to 3.5					
V _{OH}	High-level output voltage	I _{OH} = –20 μA	25°C	4.99			4.99	V			
		I _{OH} = –200 μA	25°C	4.85	4.93		4.85		4.93		
			Full range	4.85			4.85				
		I _{OH} = –1 mA	25°C	4.25	4.65		4.25		4.65		
Full range	4.25				4.25						
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA	25°C	0.01			0.01	V			
		V _{IC} = 2.5 V, I _{OL} = 500 μA	25°C	0.09	0.15		0.09		0.15		
			Full range		0.15		0.15				
		V _{IC} = 2.5 V, I _{OL} = 5 mA	25°C	0.9	1.5		0.9		1.5		
			Full range		1.5		1.5				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 10 kΩ [‡]	25°C	15	35		15	35	V/mV	
				Full range	15			15			
			R _L = 1 mΩ [‡]	25°C	175			175			
r _{id}	Differential input resistance			25°C	10 ¹²			10 ¹²	Ω		
r _i	Common-mode input resistance			25°C	10 ¹²			10 ¹²	Ω		
c _i	Common-mode input capacitance	f = 10 kHz, P package	25°C	8			8		pF		
z _o	Closed-loop output impedance	f = 1 MHz, A _V = 10	25°C	140			140		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = 0 V to 2.7 V, V _O = 2.5 V, R _S = 50 Ω	25°C	70	75		70	75	dB		
			Full range	70			70				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} /2, No load	25°C	80	95		80	95	dB		
			Full range	80			80				
I _{DD}	Supply current	V _O = 2.5 V, No load	25°C	2.2	3		2.2	3	mA		
			Full range		3			3			

† Full range is –40°C to 125°C.

‡ Referenced to 0 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLC2272I operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 0.5 V to 2.5 V, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	50			50			nV√Hz
		f = 1 kHz		25°C	9			9			
V _{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	1			1			μV
		f = 0.1 Hz to 10 Hz		25°C	1.4			1.4			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 20 kHz, R _L = 10 kΩ [‡]	A _V = 1	25°C	0.0013%			0.0013%			
			A _V = 10		0.004%			0.004%			
			A _V = 100		0.03%			0.03%			
	Gain-bandwidth product	f = 10 kHz, C _L = 100 pF [‡]	R _L = 10 kΩ [‡] ,	25°C	2.18			2.18			MHz
B _{OM}	Maximum output-swing bandwidth	V _O (PP) = 2 V, R _L = 10 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	1			1			MHz
t _s	Settling time	A _V = −1, Step = 0.5 V to 2.5 V, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]	To 0.1%	25°C	1.5			1.5			μs
			To 0.01%		2.6			2.6			
φ _m	Phase margin at unity gain	R _L = 10 kΩ [‡] , C _L = 100 pF [‡]		25°C	50°			50°			
	Gain margin			25°C	10			10			dB

† Full range is $-40^\circ\text{C to }125^\circ\text{C}$.

‡ Referenced to 0 V

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TLC2272I electrical characteristics at specified free-air temperature, $V_{DD} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0 V, R _S = 50 Ω		25°C	300		2500	300		950	μV
Full range				3000		1500					
α _{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C	2		2		μV/°C		
Input offset voltage long-term drift (see Note 4)				25°C	0.002		0.002		μV/mo		
I _{IO}	Input offset current			25°C	0.5		60	0.5		60	pA
				–40°C to 85°C		150		150			
				Full range		800		800			
I _{IB}	Input bias current			25°C	1		60	1		60	pA
				–40°C to 85°C		150		150			
				Full range		800		800			
V _{ICR}	Common-mode input voltage	R _S = 50 Ω, V _{IO} ≤ 5 mV	25°C	–5 to 4	–5.3 to 4.2	–5 to 4		–5.3 to 4.2	V		
			Full range	–5 to 3.5		–5 to 3.5					
V _{OM+}	Maximum positive peak output voltage	I _O = –20 μA		25°C	4.99		4.99		V		
		I _O = –200 μA	25°C	4.85	4.93	4.85		4.93			
			Full range	4.85		4.85					
		I _O = –1 mA	25°C	4.25	4.65	4.25		4.65			
			Full range	4.25		4.25					
V _{OM–}	Maximum negative peak output voltage	V _{IC} = 0 V, I _O = 50 μA		25°C	–4.99		–4.99		V		
		V _{IC} = 0 V, I _O = 500 μA	25°C	–4.85	–4.91	–4.85		–4.91			
			Full range	–4.85		–4.85					
		V _{IC} = 0 V, I _O = 5 mA	25°C	–3.5	–4.1	–3.5		–4.1			
			Full range	–3.5		–3.5					
A _{VD}	Large-signal differential voltage amplification	V _O = ±4 V	R _L = 10 kΩ	25°C	25	50	25		50	V/mV	
			R _L = 1 mΩ	Full range	25		25				
				25°C	300		300				
r _{id}	Differential input resistance			25°C	10 ¹²		10 ¹²		Ω		
r _i	Common-mode input resistance			25°C	10 ¹²		10 ¹²		Ω		
c _i	Common-mode input capacitance	f = 10 kHz,	P package	25°C	8		8		pF		
z _o	Closed-loop output impedance	f = 1 MHz,	A _V = 10	25°C	130		130		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = –5 V to 2.7 V, V _O = 0 V, R _S = 50 Ω		25°C	75	80	75		80	dB	
				Full range	75		75				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} ±/ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} /2, No load		25°C	80	95	80		95	dB	
				Full range	80		80				
I _{DD}	Supply current	V _O = 0 V, No load		25°C	2.4		3	2.4		3	mA
				Full range	3		3				

† Full range is –40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3\text{ V}$, $C_L = 100\text{ pF}$	$R_L = 10\text{ k}\Omega$,	25°C	2.3	3.6		2.3	3.6		V/ μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C		50			50		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C		1			1		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		$\text{fA}/\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$ $R_L = 10\text{ k}\Omega$, $f = 20\text{ kHz}$	$A_V = 1$	25°C		0.0011%			0.0011%		
			$A_V = 10$			0.004%			0.004%		
			$A_V = 100$			0.03%			0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 10\text{ k}\Omega$,	25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 10\text{ k}\Omega$,	$A_V = 1$, $C_L = 100\text{ pF}$	25°C		0.54			0.54		MHz
t_s	Settling time	$A_V = -1$, Step = $-2.3\text{ V to }2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is -40°C to 125°C .

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TLC2274I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2274I			TLC2274AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} = \pm 2.5\text{ V}, V_{IC} = 0\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	300	2500		300	950		μV
		Full range		3000			1500		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.002			0.002			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		–40°C to 85°C		150			150		
		Full range		800			800		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		–40°C to 85°C		150			150		
		Full range		800			800		
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.99			4.99		V
	$I_{OH} = -200\ \mu\text{A}$	25°C	4.85	4.93		4.85	4.93		
		Full range	4.85			4.85			
	$I_{OH} = -1\text{ mA}$	25°C	4.25	4.65		4.25	4.65		
		Full range	4.25			4.25			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01		V
	$V_{IC} = 2.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	25°C		0.09 0.15			0.09 0.15		
		Full range		0.15			0.15		
	$V_{IC} = 2.5\text{ V}, I_{OL} = 5\text{ mA}$	25°C		0.9 1.5			0.9 1.5		
		Full range		1.5			1.5		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}, V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega^\ddagger$	25°C	15	35	15	35		V/mV
			Full range	15		15			
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C	175		175			
r_{id} Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
C_i Common-mode input capacitance	$f = 10\text{ kHz}, \text{ N package}$	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 1\text{ MHz}, A_V = 10$	25°C		140			140		Ω
$CMRR$ Common-mode rejection ratio	$V_{IC} = 0\text{ V to }2.7\text{ V}, V_O = 2.5\text{ V}, R_S = 50\ \Omega$	25°C	70	75		70	75		dB
		Full range	70			70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C	4.4	6		4.4	6		mA
		Full range		6			6		

† Full range is –40°C to 125°C.

‡ Referenced to 0 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274I operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2274I			TLC2274AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 0.5 V to 2.5 V, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	50			50			nV/√Hz
		f = 1 kHz		25°C	9			9			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	1			1			μV
		f = 0.1 Hz to 10 Hz		25°C	1.4			1.4			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 20 kHz, R _L = 10 kΩ [‡]	A _V = 1	25°C	0.0013%			0.0013%			
			A _V = 10		0.004%			0.004%			
			A _V = 100		0.03%			0.03%			
	Gain-bandwidth product	f = 10 kHz, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]		25°C	2.18			2.18			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, A _V = 1, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]		25°C	1			1			MHz
t _s	Settling time	A _V = −1, Step = 0.5 V to 2.5 V, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]	To 0.1%	25°C	1.5			1.5			μs
			To 0.01%		2.6			2.6			
ϕ _m	Phase margin at unity gain	R _L = 10 kΩ [‡] , C _L = 100 pF [‡]		25°C	50°			50°			
	Gain margin			25°C	10			10			dB

† Full range is -40°C to 125°C .

‡ Referenced to 0 V

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TLC2274I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2274I			TLC2274AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	300	2500		300	950		μV
		Full range		3000			1500		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.002			0.002			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		–40°C to 85°C		150			150		
		Full range		800			800		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		–40°C to 85°C		150			150		
		Full range		800			800		
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	–5 to 4	–5.3 to 4.2		–5 to 4	–5.3 to 4.2		V
		Full range	–5 to 3.5			–5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C		4.99			4.99		V
	$I_O = -200\ \mu\text{A}$	25°C	4.85	4.93		4.85	4.93		
		Full range	4.85			4.85			
	$I_O = -1\text{ mA}$	25°C	4.25	4.65		4.25	4.65		
		Full range	4.25			4.25			
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0\text{ V}, I_O = 50\ \mu\text{A}$	25°C		–4.99			–4.99		V
	$V_{IC} = 0\text{ V}, I_O = 500\ \mu\text{A}$	25°C	–4.85	–4.91		–4.85	–4.91		
		Full range	–4.85			–4.85			
	$V_{IC} = 0\text{ V}, I_O = 5\text{ mA}$	25°C	–3.5	–4.1		–3.5	–4.1		
		Full range	–3.5			–3.5			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$	$R_L = 10\text{ k}\Omega$	25°C	25	50	25	50		V/mV
			Full range	25		25			
		$R_L = 1\text{ M}\Omega$	25°C	300		300			
r_{id} Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
C_i Common-mode input capacitance	$f = 10\text{ kHz}, \text{ N package}$	25°C		8			8		pF
Z_o Closed-loop output impedance	$f = 1\text{ MHz}, A_V = 10$	25°C		130			130		Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5\text{ V to } 2.7\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	75	80		75	80		dB
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2\text{ V to } \pm 8\text{ V}, V_{IC} = 0\text{ V}, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 0\text{ V}, \text{ No load}$	25°C	4.8	6		4.8	6		mA
		Full range		6			6		

† Full range is –40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLC2274I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLC2274I			TLC2274AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3\text{ V}$, $C_L = 100\text{ pF}$	$R_L = 10\text{ k}\Omega$	25°C	2.3	3.6		2.3	3.6		V/ μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C		50			50		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C		1			1		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $f = 20\text{ kHz}$	$A_V = 1$	25°C		0.0011%			0.0011%		
			$A_V = 10$			0.004%			0.004%		
			$A_V = 100$			0.03%			0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 10\text{ k}\Omega$	25°C		2.25			2.25		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 10\text{ k}\Omega$	$A_V = 1$, $C_L = 100\text{ pF}$	25°C		0.54			0.54		MHz
t_s	Settling time	$A_V = -1$, Step = $-2.3\text{ V to }2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is -40°C to 125°C .

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TLC2272Q and TLC2272M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2272Q, TLC2272M			TLC2272AQ, TLC2272AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0\text{ V}, V_O = 0\text{ V}, V_{DD\pm} = \pm 2.5\text{ V}, R_S = 50\ \Omega$	25°C	300	2500		300	950		μV
		Full range		3000			1500		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.002			0.002			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		Full range		800			800		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		Full range		800			800		
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.99			4.99		V
	$I_{OH} = -200\ \mu\text{A}$	25°C	4.85	4.93		4.85	4.93		
	$I_{OH} = -1\text{ mA}$	Full range	4.85			4.85			
		25°C	4.25	4.65		4.25	4.65		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01		V
	$V_{IC} = 2.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	25°C		0.09	0.15		0.09	0.15	
	$V_{IC} = 2.5\text{ V}, I_{OL} = 5\text{ mA}$	Full range			0.15			0.15	
		25°C		0.9	1.5		0.9	1.5	
		Full range			1.5			1.5	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}, V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega^\ddagger$	25°C	10	35		10	35	V/mV
		$R_L = 1\text{ m}\Omega^\ddagger$	25°C	175			175		
		Full range	10			10			
r_{id} Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
C_i Common-mode input capacitance	$f = 10\text{ kHz}, \text{ P package}$	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 1\text{ MHz}, A_V = 10$	25°C		140			140		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ V to }2.7\text{ V}, V_O = 2.5\text{ V}, R_S = 50\ \Omega$	25°C	70	75		70	75		dB
		Full range	70			70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C		2.2	3		2.2	3	mA
		Full range			3			3	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272Q and TLC2272M operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2272Q, TLC2272M			TLC2272AQ, TLC2272AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1.25\text{ V to }2.75\text{ V},$ $R_L = 10\text{ k}\Omega^\ddagger, \quad C_L = 100\text{ pF}^\ddagger$	25°C	2.3	3.6		2.3	3.6		V/ μs
		Full range	1.7			1.7			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		50			50		nV/ $\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		9			9		
V_{NPP} Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		1			1		μV
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.4			1.4		
I_n Equivalent input noise current		25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V},$ $f = 20\text{ kHz},$ $R_L = 10\text{ k}\Omega^\ddagger,$	$A_V = 1$		0.0013%			0.0013%		
		$A_V = 10$		0.004%			0.004%		
		$A_V = 100$		0.03%			0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}, \quad R_L = 10\text{ k}\Omega^\ddagger,$ $C_L = 100\text{ pF}^\ddagger$	25°C		2.18			2.18	MHz
B_{OM} Maximum output- swing bandwidth	$V_{O(PP)} = 2\text{ V},$ $R_L = 10\text{ k}\Omega^\ddagger, \quad A_V = 1,$ $C_L = 100\text{ pF}^\ddagger$	25°C		1			1		MHz
t_s Settling time	$A_V = -1,$ Step = 0.5 V to 2.5 V, $R_L = 10\text{ k}\Omega^\ddagger,$ $C_L = 100\text{ pF}^\ddagger$	To 0.1%	25°C	1.5			1.5		μs
		To 0.01%		2.6			2.6		
ϕ_m Phase margin at unity gain	$R_L = 10\text{ k}\Omega^\ddagger, \quad C_L = 100\text{ pF}^\ddagger$	25°C		50°			50°		
	Gain margin	25°C		10			10		dB

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

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TLC2272Q and TLC2272M electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2272Q, TLC2272M			TLC2272AQ, TLC2272AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	300	2500		300	950		μV
		Full range		3000			1500		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.002			0.002			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		Full range		800			800		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		Full range		800			800		
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2		V
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C		4.99			4.99		V
	$I_O = -200\ \mu\text{A}$	25°C	4.85	4.93		4.85	4.93		
		Full range	4.85			4.85			
	$I_O = -1\text{ mA}$	25°C	4.25	4.65		4.25	4.65		
		Full range	4.25			4.25			
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0\text{ V}, I_O = 50\ \mu\text{A}$	25°C		-4.99			-4.99		V
	$V_{IC} = 0\text{ V}, I_O = 500\ \mu\text{A}$	25°C	-4.85	-4.91		-4.85	-4.91		
		Full range	-4.85			-4.85			
	$V_{IC} = 0\text{ V}, I_O = 5\text{ mA}$	25°C	-3.5	-4.1		-3.5	-4.1		
		Full range	-3.5			-3.5			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$	$R_L = 10\text{ k}\Omega$	25°C	20	50	20	50		V/mV
			Full range	20		20			
		$R_L = 1\text{ m}\Omega$	25°C	300		300			
r_{id} Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i Common-mode input capacitance	$f = 10\text{ kHz}, \text{ P package}$	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 1\text{ MHz}, A_V = 10$	25°C		130			130		Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5\text{ V to } 2.7\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	75	80		75	80		dB
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = \pm 2.2\text{ V to } \pm 8\text{ V}, V_{IC} = 0\text{ V}, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C	2.4	3		2.4	3		mA
		Full range		3			3		

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLC2272Q and TLC2272M operating characteristics at specified free-air temperature,
 $V_{DD\pm} = \pm 5\text{ V}$**

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2272Q, TLC2272M			TLC2272AQ, TLC2272AM			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain	V _O = ±1 V, C _L = 100 pF		R _L = 10 kΩ,	25°C	2.3	3.6		2.3	3.6	V/μs	
					Full range	1.7			1.7			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	50			50			nV/√Hz	
		f = 1 kHz		25°C	9			9				
V _{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	1			1			μV	
		f = 0.1 Hz to 10 Hz		25°C	1.4			1.4				
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz	
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V R _L = 10 kΩ, f = 20 kHz	A _V = 1	25°C	0.0011%			0.0011%				
			A _V = 10		0.004%			0.004%				
			A _V = 100		0.03%			0.03%				
	Gain-bandwidth product	f = 10 kHz, C _L = 100 pF		R _L = 10 kΩ,	25°C	2.25			2.25			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 10 kΩ,		A _V = 1, C _L = 100 pF	25°C	0.54			0.54			MHz
t _s	Settling time	A _V = −1, Step = −2.3 V to 2.3 V, R _L = 10 kΩ, C _L = 100 pF	To 0.1%	25°C	1.5			1.5			μs	
			To 0.01%		3.2			3.2				
φ _m	Phase margin at unity gain	R _L = 10 kΩ,		C _L = 100 pF	25°C	52°			52°			
	Gain margin				25°C	10			10			dB

[†] Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

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TLC2274Q and TLC2274M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2274Q, TLC2274M			TLC2274AQ, TLC2274AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0\text{ V}$, $V_{IC} = 0\text{ V}$, $R_S = 50\ \Omega$	25°C	300	2500		300	950		μV
		Full range		3000			1500		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.002			0.002			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		Full range		800			800		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		Full range		800			800		
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.99			4.99		V
	$I_{OH} = -200\ \mu\text{A}$	25°C	4.85	4.93		4.85	4.93		
		Full range	4.85			4.85			
	$I_{OH} = -1\text{ mA}$	25°C	4.25	4.65		4.25	4.65		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01		V
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C		0.09	0.15		0.09	0.15	
		Full range			0.15			0.15	
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 5\text{ mA}$	25°C		0.9	1.5		0.9	1.5	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega^\ddagger$	25°C	10	35		10	35	V/mV
			Full range	10			10		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C	175			175		
r_{id} Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i Common-mode input capacitance	$f = 10\text{ kHz}$, N package	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 1\text{ MHz}$, $A_V = 10$	25°C		140			140		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ V to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	75		70	75		dB
		Full range	70			70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C		4.4	6		4.4	6	mA
		Full range			6			6	

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLC2274Q and TLC2274M operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2274Q, TLC2274M			TLC2274AQ, TLC2274AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.5\text{ V to }2.5\text{ V},$ $R_L = 10\text{ k}\Omega^\ddagger,$ $C_L = 100\text{ pF}^\ddagger$	25°C	2.3	3.6		2.3	3.6		V/ μs
		Full range	1.7			1.7			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		50			50		nV/ $\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		9			9		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		1			1		μV
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.4			1.4		
I_n Equivalent input noise current		25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V},$ $f = 20\text{ kHz},$ $R_L = 10\text{ k}\Omega^\ddagger$	$A_V = 1$		0.0013%			0.0013%		
		$A_V = 10$		0.004%			0.004%		
		$A_V = 100$		0.03%			0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz},$ $C_L = 100\text{ pF}^\ddagger$ $R_L = 10\text{ k}\Omega^\ddagger,$	25°C		2.18		2.18		MHz
B_{OM} Maximum out-put-swing band-width	$V_{O(PP)} = 2\text{ V},$ $R_L = 10\text{ k}\Omega^\ddagger,$ $A_V = 1,$ $C_L = 100\text{ pF}^\ddagger$	25°C		1			1		MHz
t_s Settling time	$A_V = -1,$ Step = $0.5\text{ V to }2.5\text{ V},$ $R_L = 10\text{ k}\Omega^\ddagger,$ $C_L = 100\text{ pF}^\ddagger$	To 0.1%	25°C		1.5		1.5		μs
		To 0.01%	25°C		2.6		2.6		
ϕ_m Phase margin at unity gain	$R_L = 10\text{ k}\Omega^\ddagger,$ $C_L = 100\text{ pF}^\ddagger$	25°C		50°			50°		
Gain margin		25°C		10			10		dB

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

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TLC2274Q and TLC2274M electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2274Q, TLC2274M			TLC2274AQ, TLC2274AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω		25°C	300	2500		300	950	μV	
	Full range			3000			1500				
αV _{IO}	Temperature coefficient of input offset voltage			25°C to 125°C	2			2			μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C	0.002			0.002			μV/mo
I _{IO}	Input offset current			25°C	0.5	60		0.5	60	pA	
				Full range	800			800			
I _{IB}	Input bias current			25°C	1	60		1	60	pA	
				Full range	800			800			
V _{ICR}	Common-mode input voltage	R _S = 50 Ω, V _{IO} ≤ 5 mV		25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
				Full range	-5 to 3.5			-5 to 3.5			
V _{OM+}	Maximum positive peak output voltage	I _O = -20 μA		25°C	4.99			4.99			V
		I _O = -200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
				I _O = -1 mA		25°C	4.25	4.65		4.25	
				Full range	4.25			4.25			
V _{OM-}	Maximum negative peak output voltage	V _{IC} = 0 V, I _O = 50 μA		25°C	-4.99			-4.99			V
		V _{IC} = 0 V, I _O = 500 μA		25°C	-4.85	-4.91		-4.85	-4.91		
				Full range	-4.85			-4.85			
				V _{IC} = 0 V, I _O = 5 mA		25°C	-3.5	-4.1		-3.5	
				Full range	-3.5			-3.5			
A _{VD}	Large-signal differential voltage amplification	V _O = ±4 V	R _L = 10 kΩ	25°C	20	50		20	50	V/mV	
				Full range	20			20			
			R _L = 1 MΩ	25°C	300			300			
r _{id}	Differential input resistance			25°C	10 ¹²			10 ¹²			Ω
r _i	Common-mode input resistance			25°C	10 ¹²			10 ¹²			Ω
c _i	Common-mode input capacitance	f = 10 kHz,	N package	25°C	8			8			pF
z _o	Closed-loop output impedance	f = 1 MHz,	A _V = 10	25°C	130			130			Ω
CMRR	Common-mode rejection ratio	V _{IC} = -5 V to 2.7 V V _O = 0 V, R _S = 50 Ω		25°C	75	80		75	80	dB	
				Full range	75			75			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD±} = ± 2.2 V to ±8 V, V _{IC} = 0 V, No load		25°C	80	95		80	95	dB	
				Full range	80			80			
I _{DD}	Supply current	V _O = 0 V, No load		25°C	4.8	6		4.8	6	mA	
				Full range	6			6			

† Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

**TLC2274Q and TLC2274M operating characteristics at specified free-air temperature,
 $V_{DD\pm} = \pm 5\text{ V}$**

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2274Q, TLC2274M			TLC2274AQ, TLC2274AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±2.3 V, C _L = 100 pF		R _L = 10 kΩ,	25°C	2.3	3.6		2.3	3.6	V/μs
					Full range	1.7			1.7		
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	50			50			nV/√Hz
		f = 1 kHz		25°C	9			9			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	1			1			μV
		f = 0.1 Hz to 10 Hz		25°C	1.4			1.4			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V, R _L = 10 kΩ, f = 20 kHz	A _V = 1	25°C	0.0011%			0.0011%			
			A _V = 10		0.004%			0.004%			
			A _V = 100		0.03%			0.03%			
	Gain-bandwidth product	f = 10 kHz, C _L = 100 pF	R _L = 10 kΩ,	25°C	2.25			2.25			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 10 kΩ,	A _V = 1, C _L = 100 pF	25°C	0.54			0.54			MHz
t _s	Settling time	A _V = -1, Step = -2.3 V to 2.3 V, R _L = 10 kΩ, C _L = 100 pF	To 0.1%	25°C	1.5			1.5			μs
			To 0.01%		3.2			3.2			
φ _m	Phase margin at unit gain	R _L = 10 kΩ, C _L = 100 pF		25°C	52°			52°			
	Gain margin			25°C	10			10			dB

[†] Full range is -40°C to 125°C for Q level part, -55°C to 125°C for M level part.

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k_{SVR}	Supply-voltage rejection ratio	vs Frequency	33, 34
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NOTE: For all graphs where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

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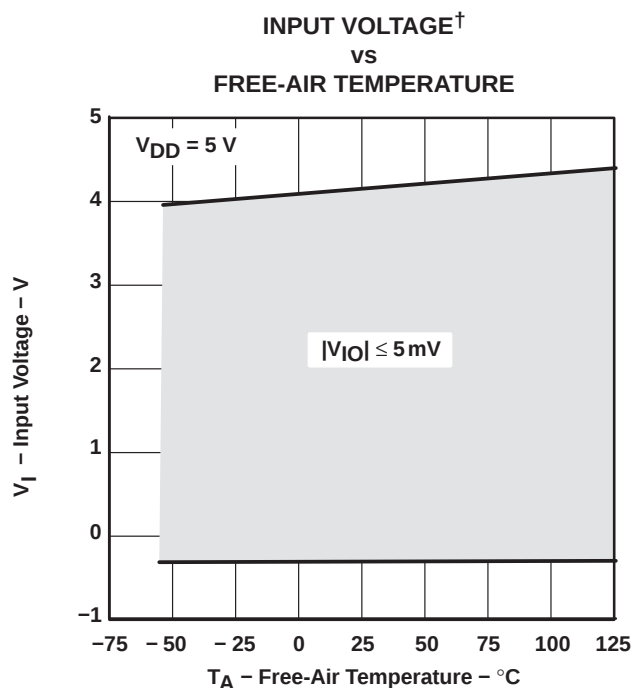


Figure 13

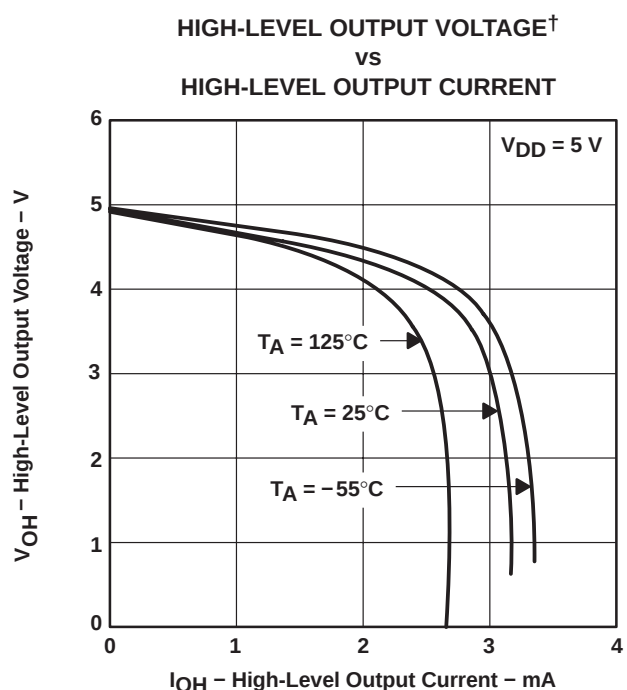


Figure 14

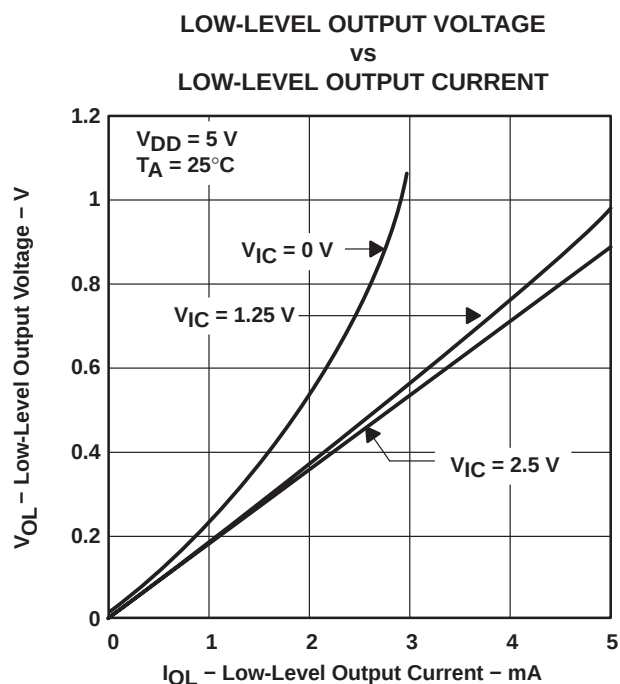


Figure 15

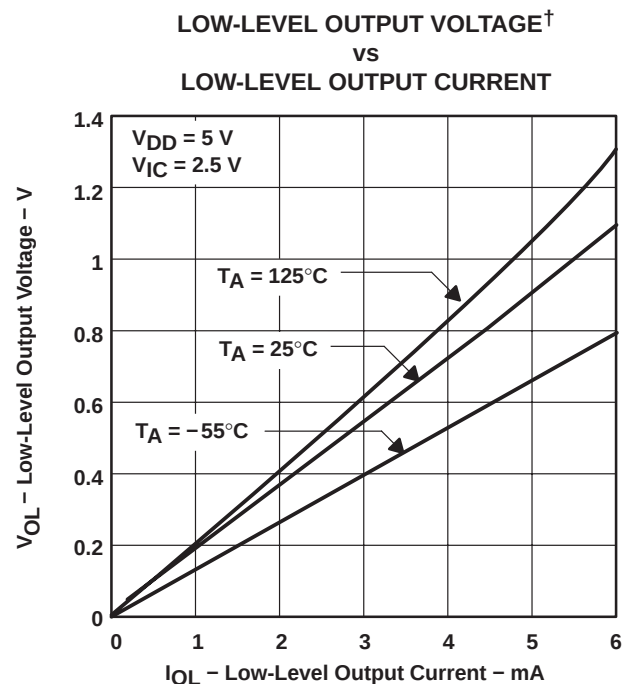
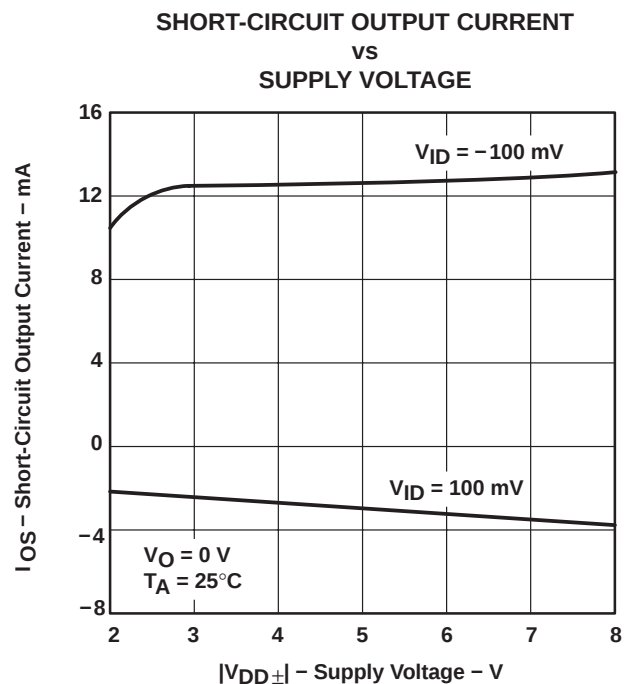
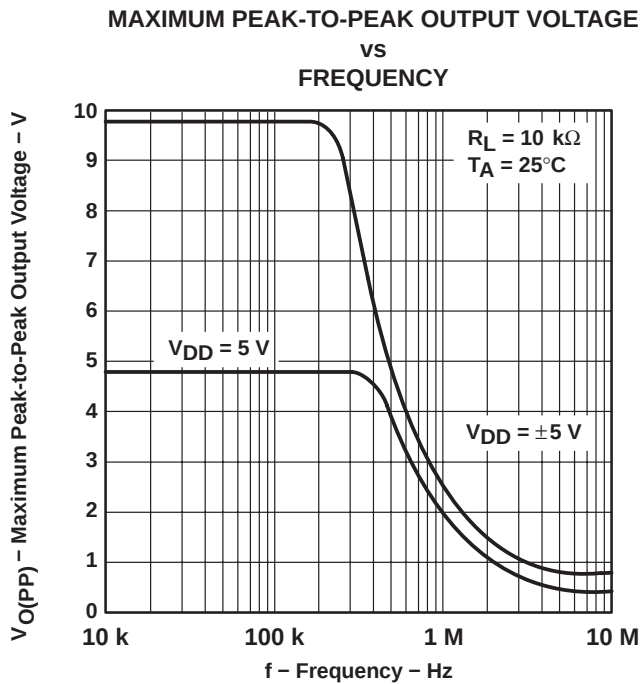
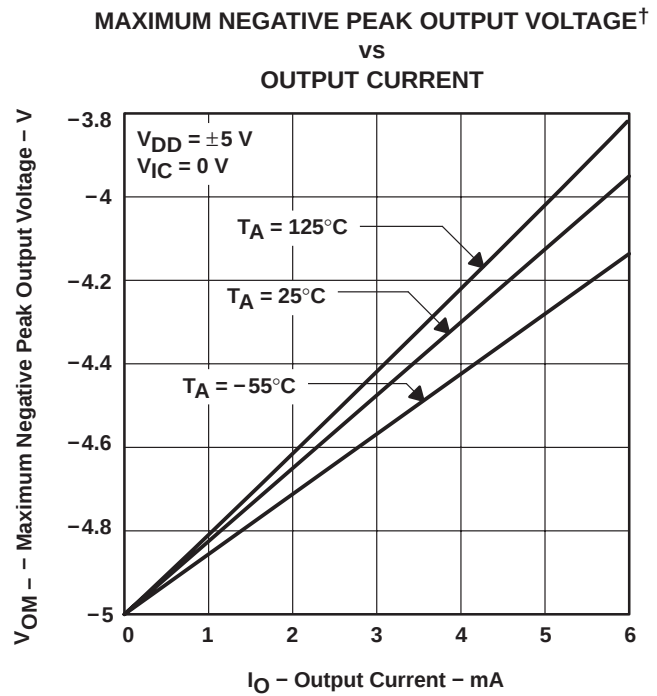
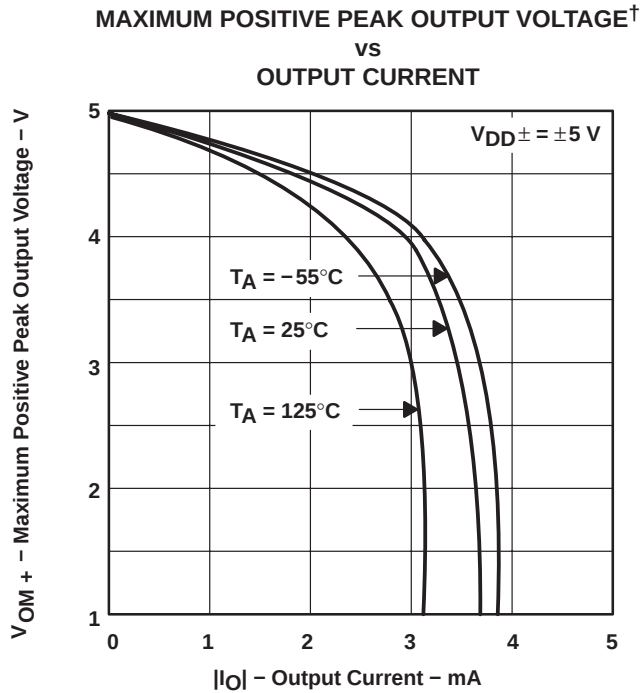


Figure 16

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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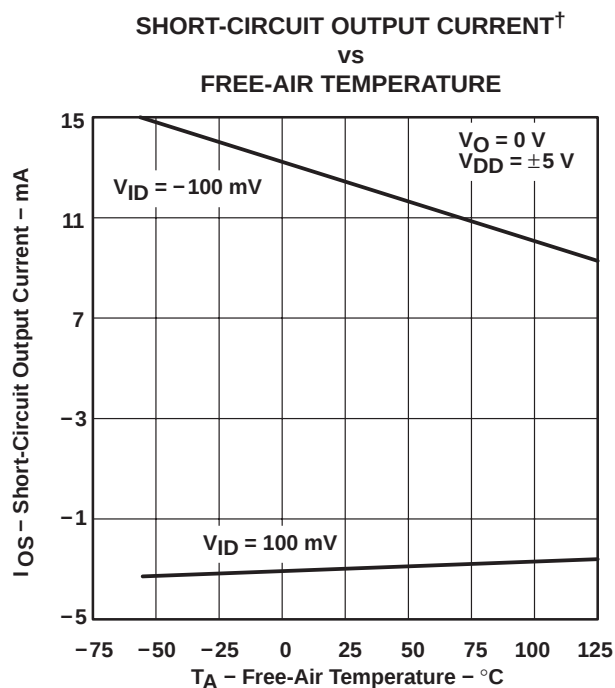


Figure 21

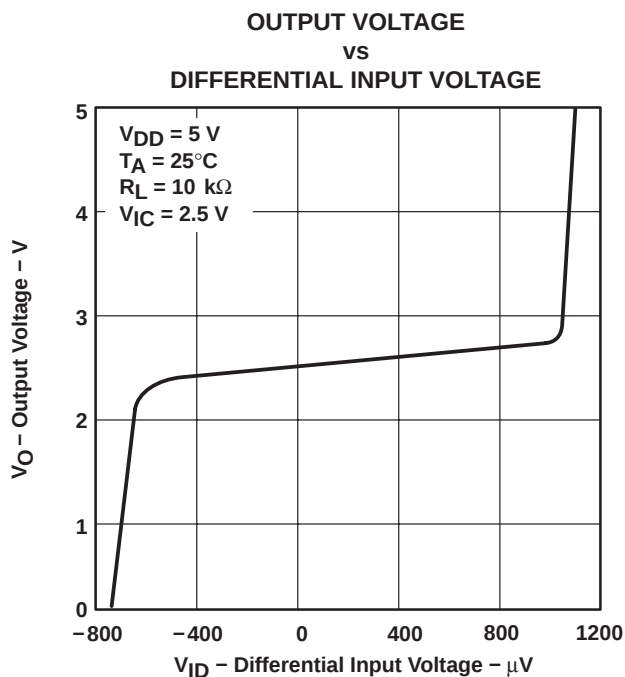


Figure 22

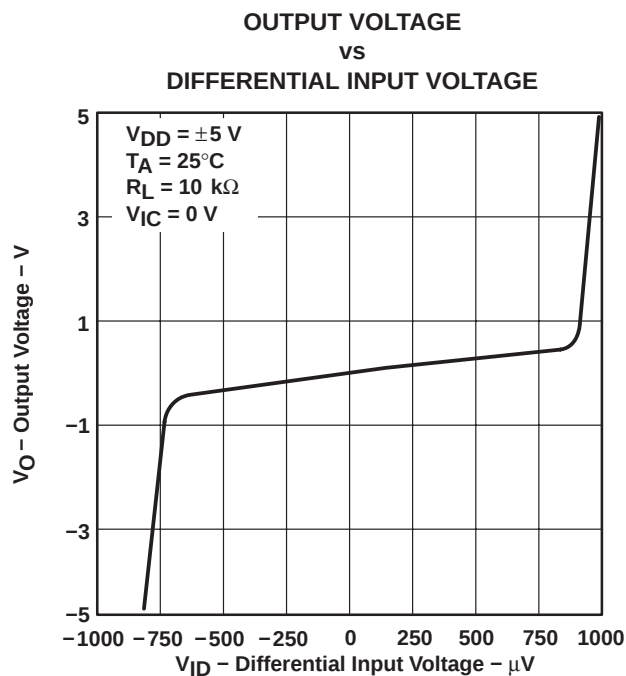


Figure 23

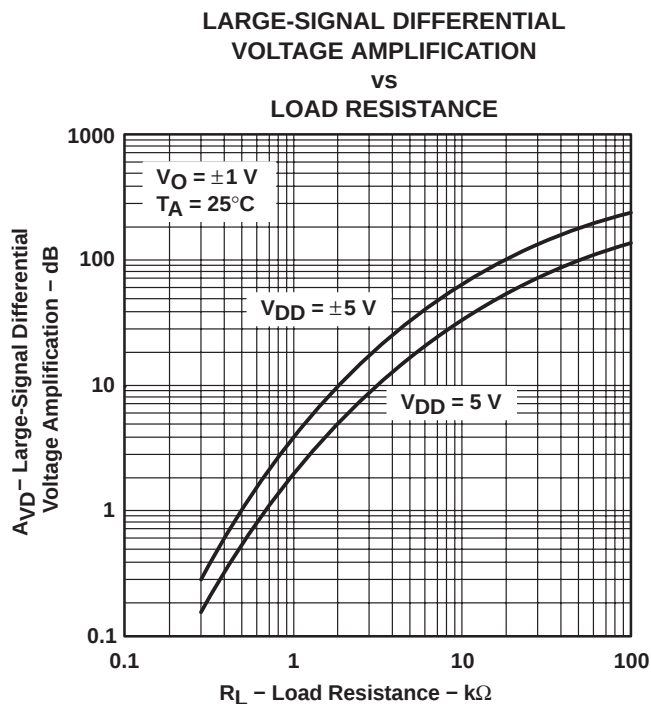


Figure 24

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN

VS
FREQUENCY

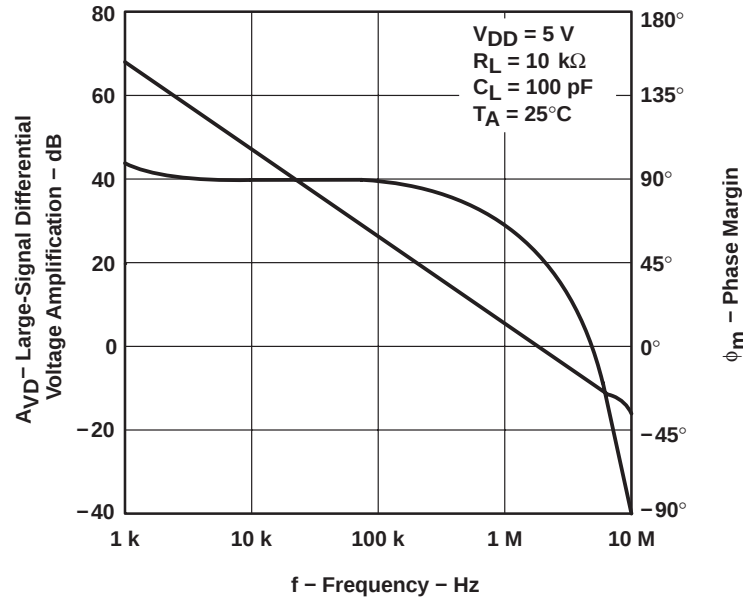


Figure 25

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN

VS
FREQUENCY

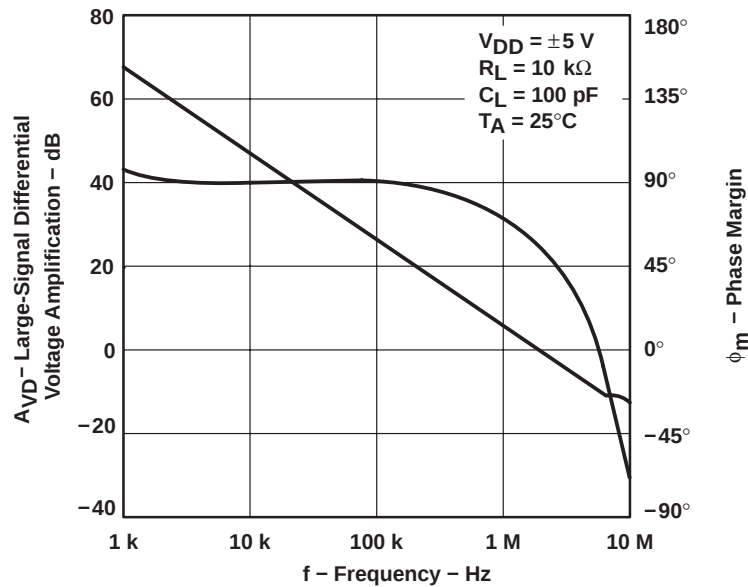


Figure 26

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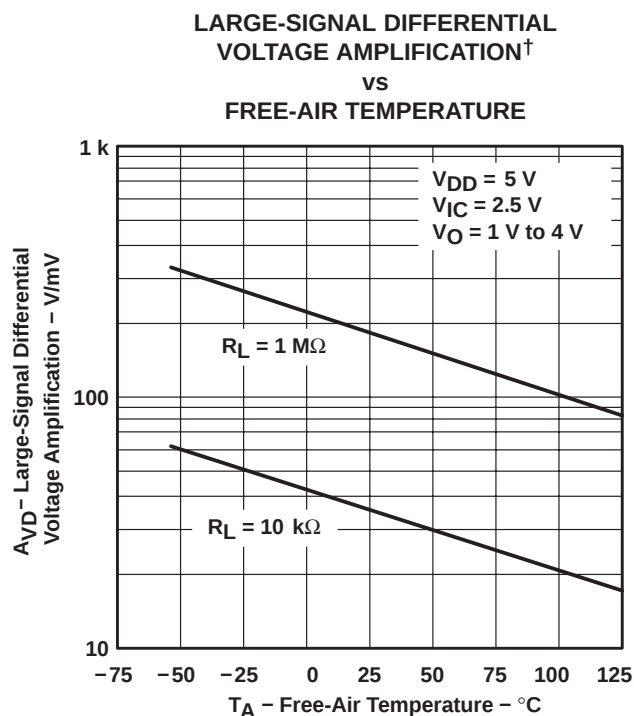


Figure 27

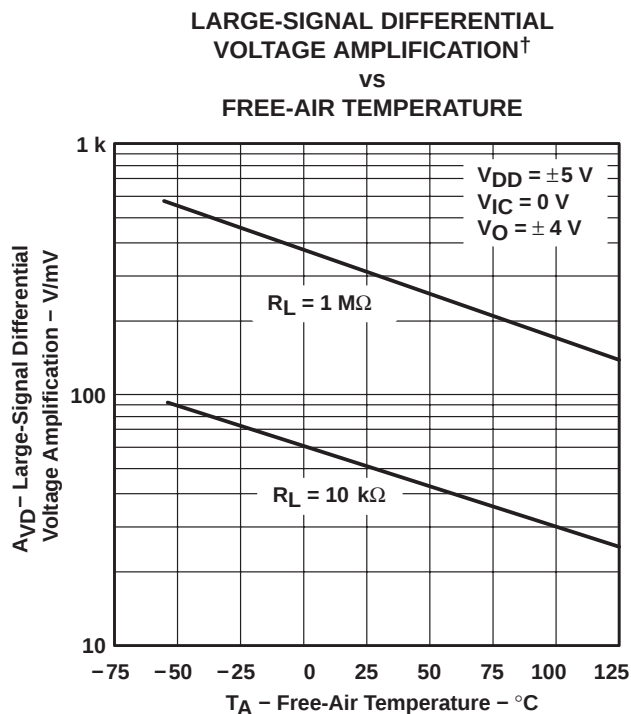


Figure 28

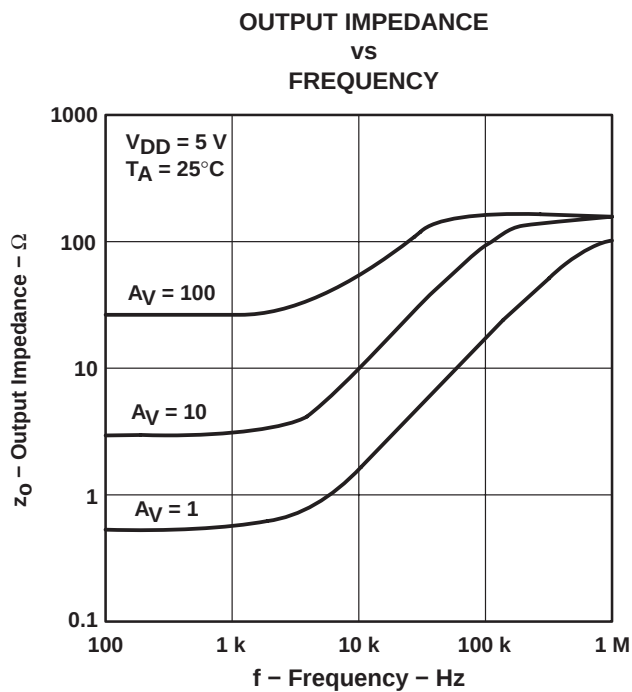


Figure 29

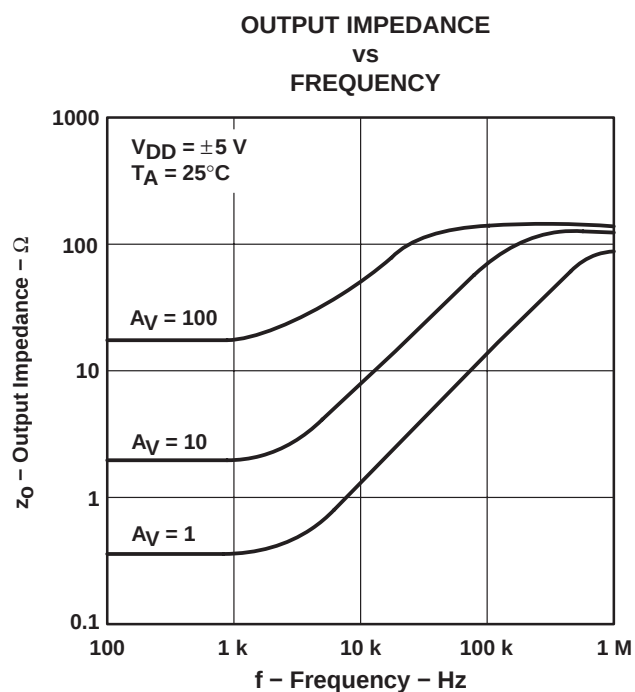


Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

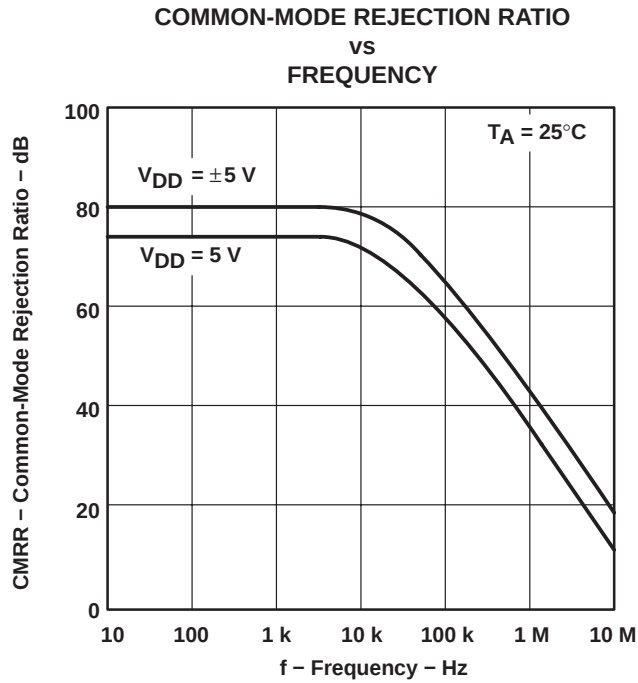


Figure 31

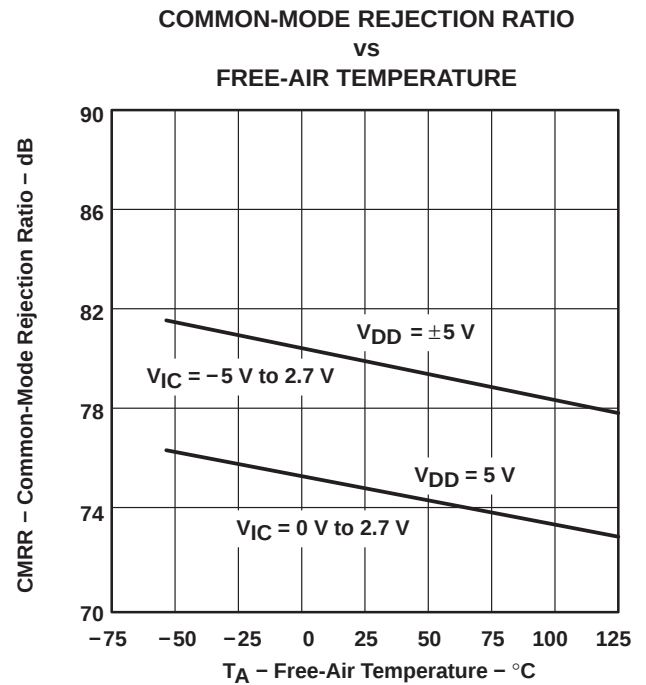


Figure 32

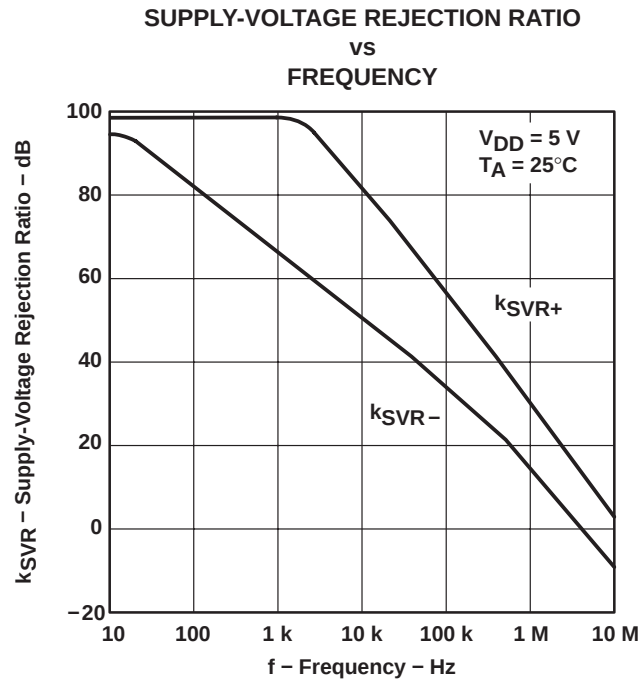


Figure 33

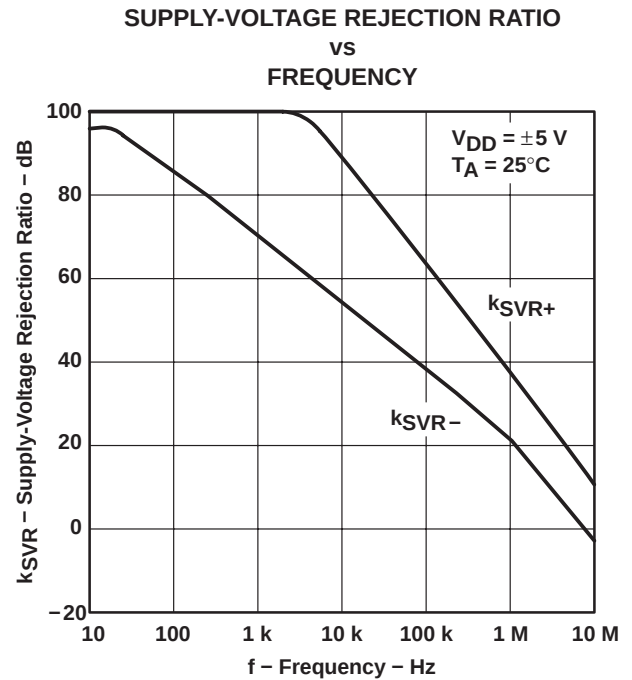


Figure 34

TLC227x, TLC227xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS190G – FEBRUARY 1997 – REVISED MAY 2004

TYPICAL CHARACTERISTICS

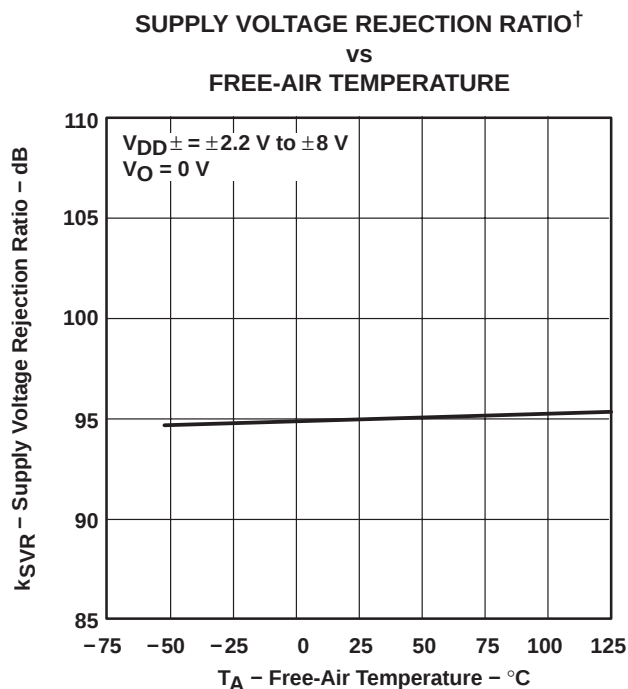


Figure 35

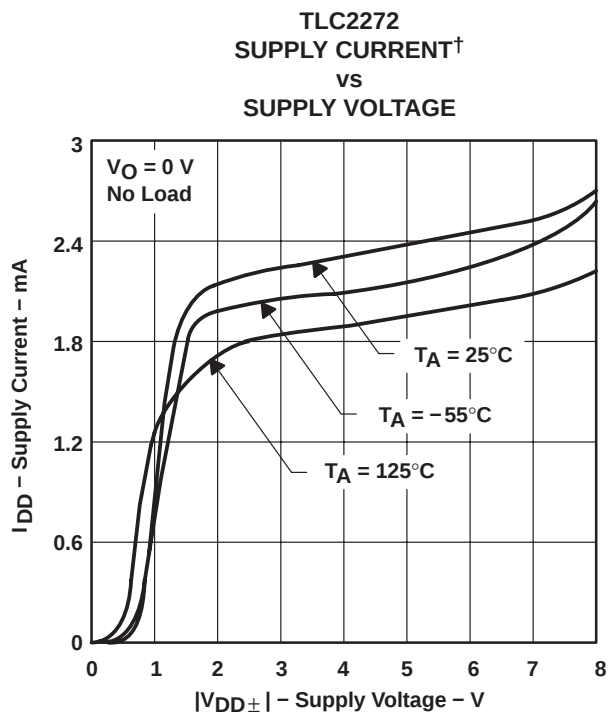


Figure 36

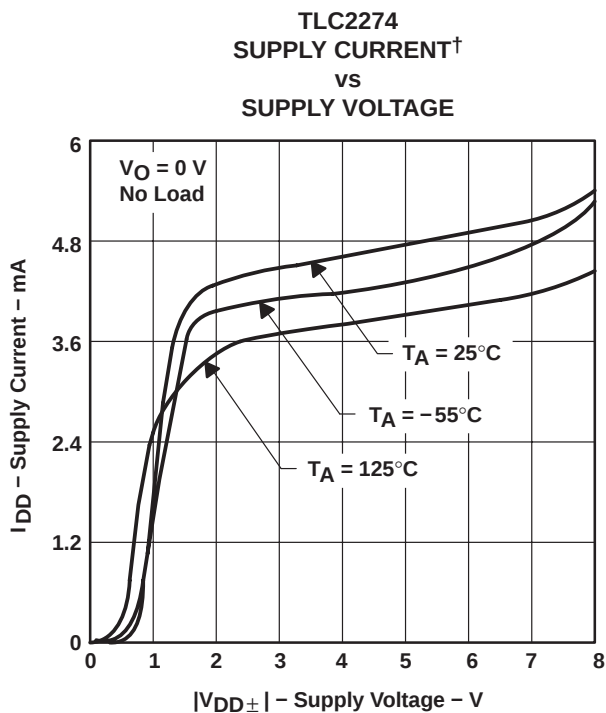


Figure 37

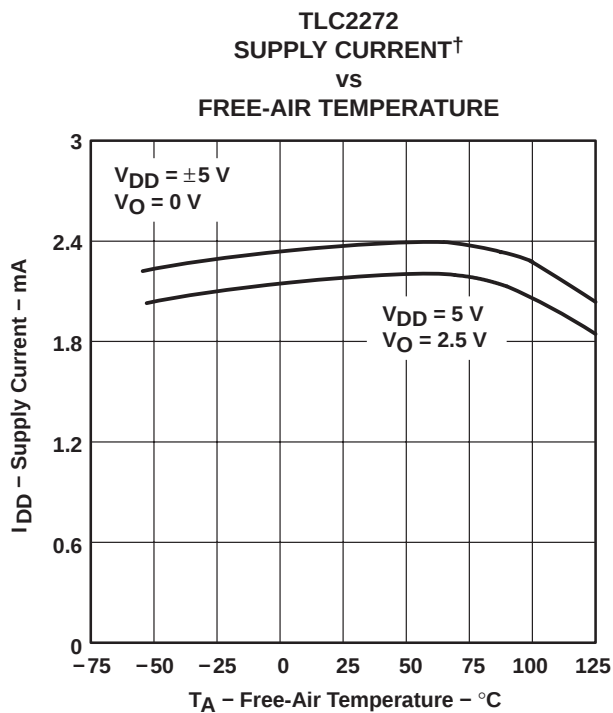


Figure 38

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

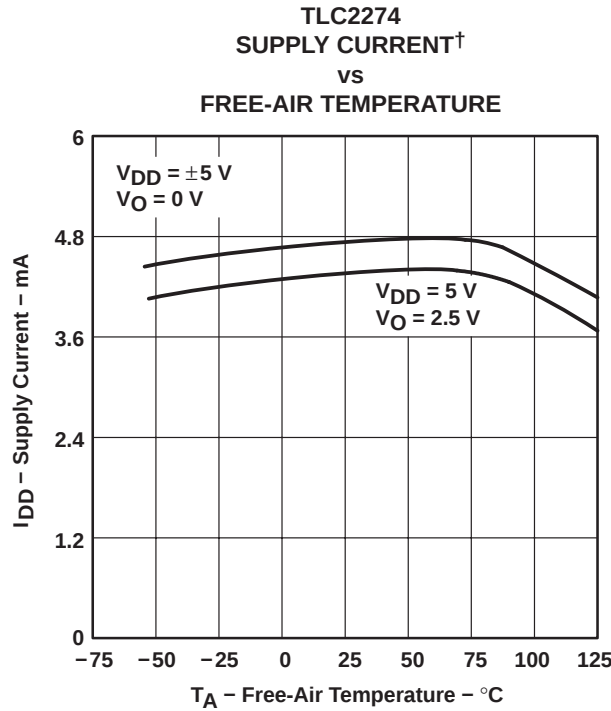


Figure 39

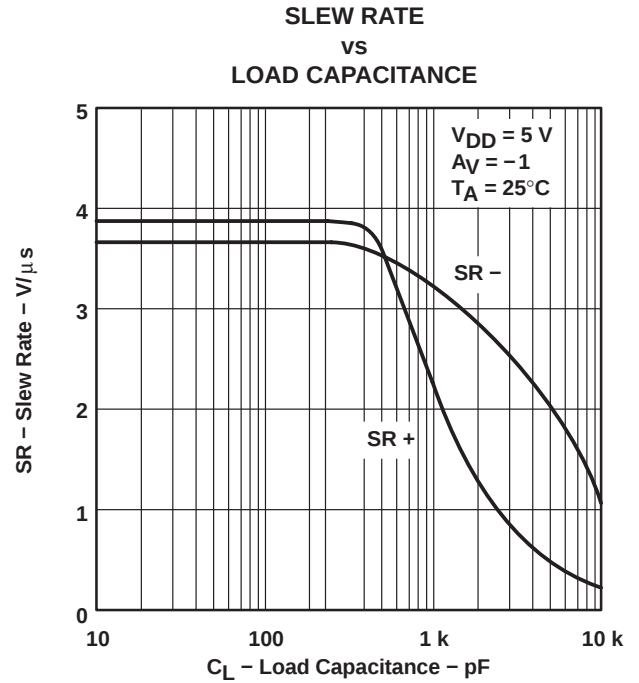


Figure 40

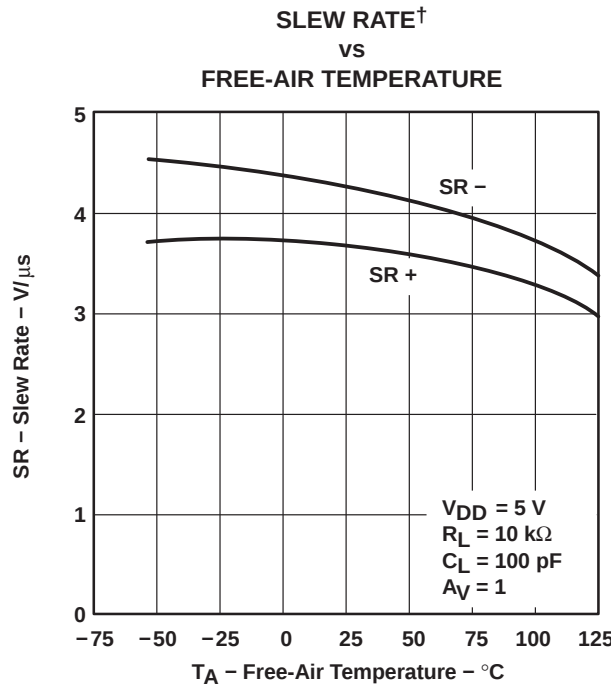


Figure 41

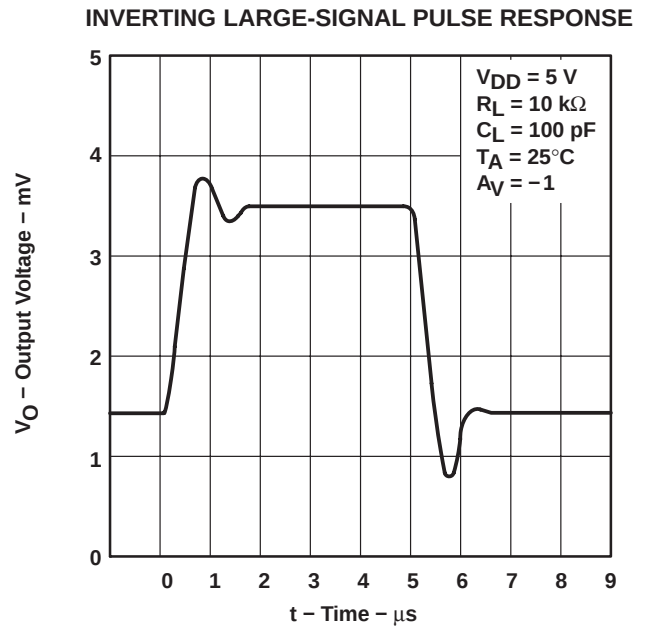


Figure 42

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLC227x, TLC227xA

Advanced LinCMOS™ RAIL-TO-RAIL

OPERATIONAL AMPLIFIERS

SLOS190G – FEBRUARY 1997 – REVISED MAY 2004

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE

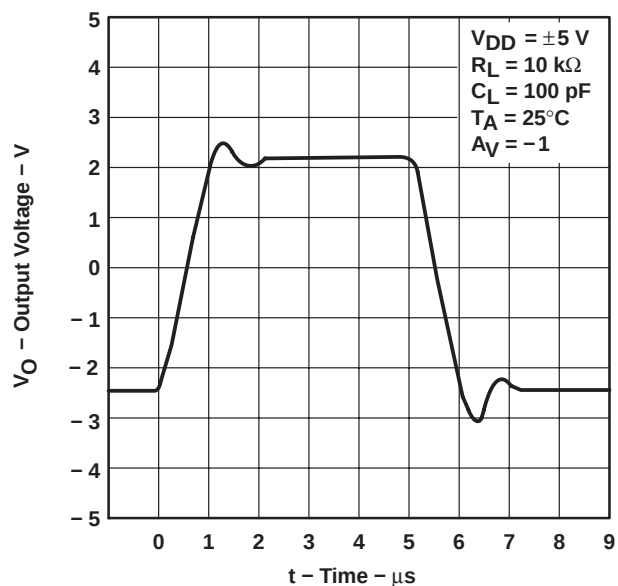


Figure 43

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

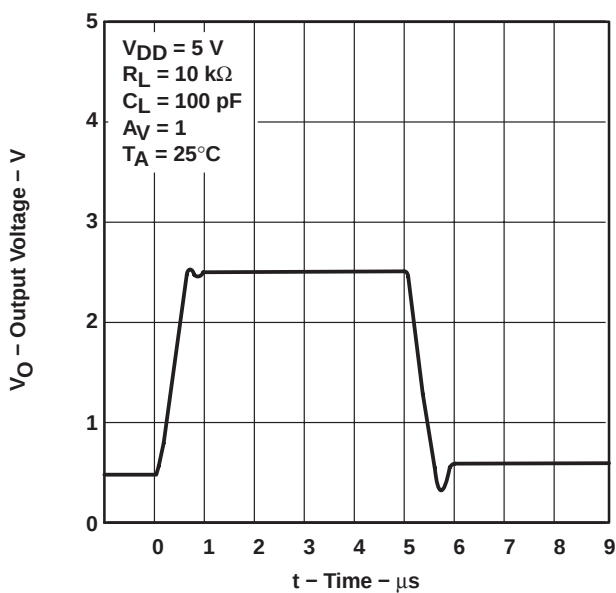


Figure 44

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

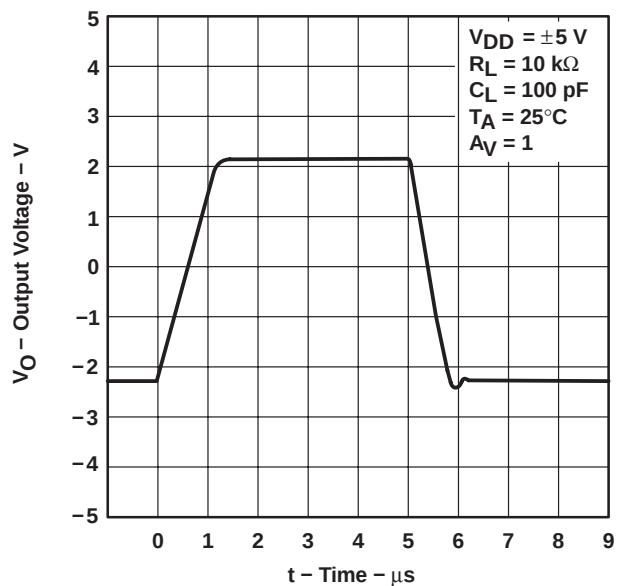


Figure 45

INVERTING SMALL-SIGNAL PULSE RESPONSE

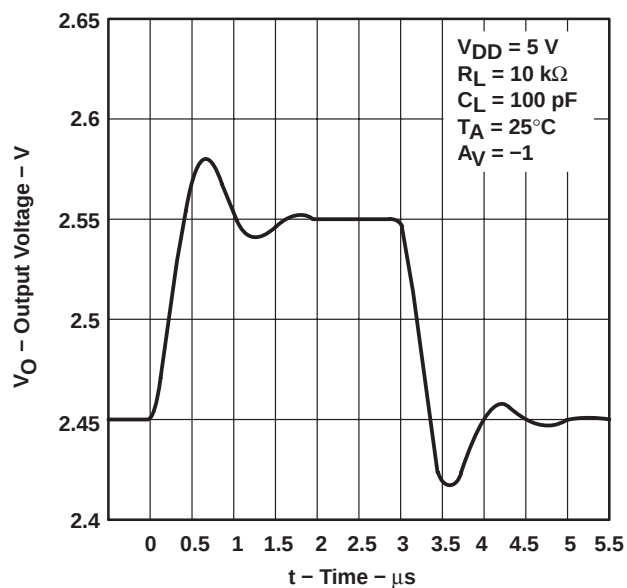
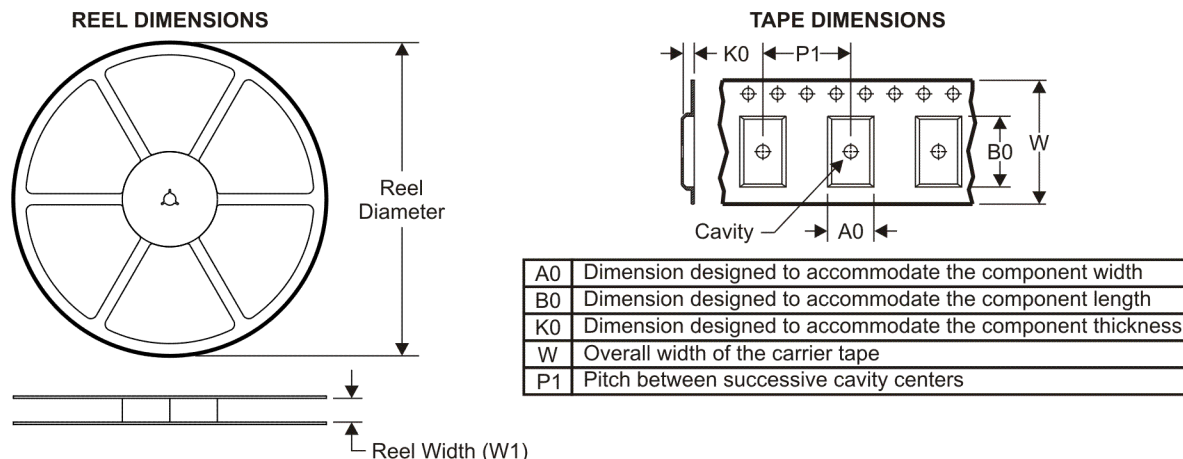
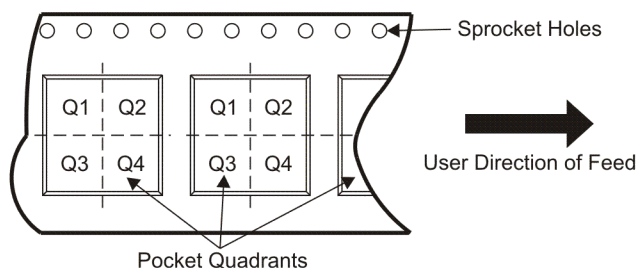


Figure 46

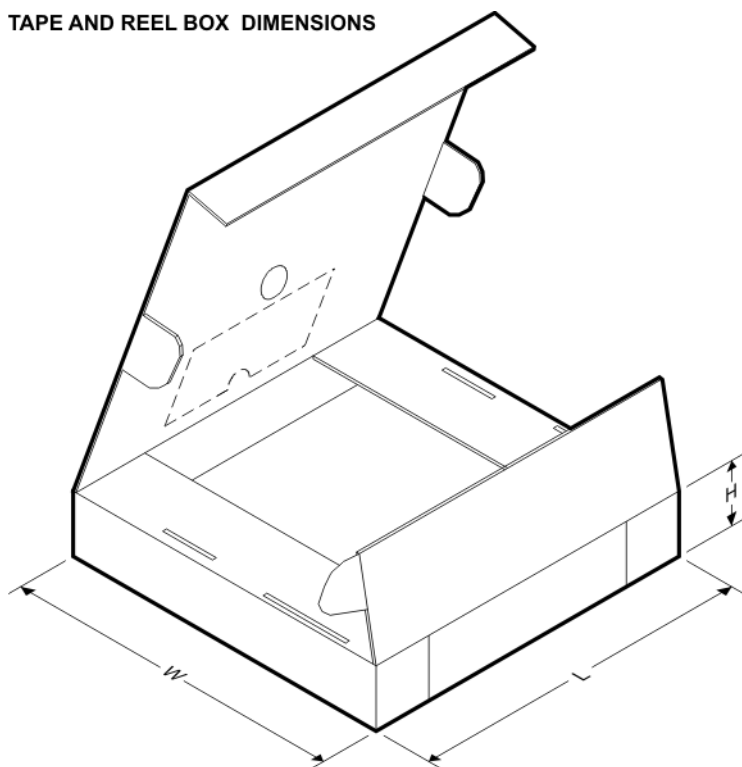
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962-9555201NXDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272ACPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272AMDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TLC2272CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2274ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274ACPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274AMDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274AQDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2274CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TLC2274CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274MDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



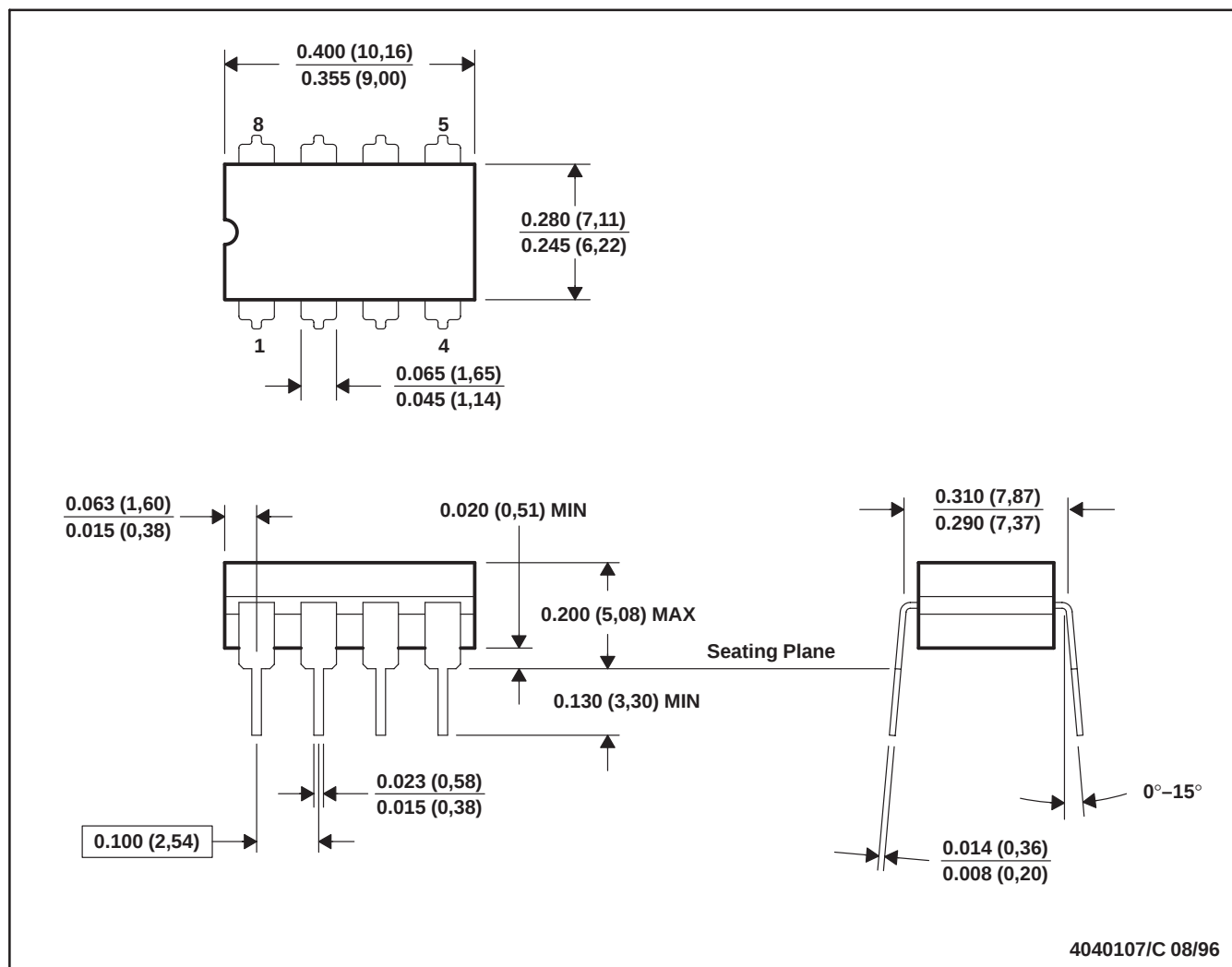
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962-9555201NXDR	SOIC	D	8	2500	346.0	346.0	29.0
TLC2272ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272ACPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TLC2272AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272AMDR	SOIC	D	8	2500	346.0	346.0	29.0
TLC2272CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272CPSR	SO	PS	8	2000	346.0	346.0	33.0
TLC2272CPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TLC2272IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272IPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TLC2272MDR	SOIC	D	8	2500	346.0	346.0	29.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2274ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274ACPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
TLC2274AIDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274AIPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
TLC2274AMDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC2274AQDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC2274CDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274CNSR	SO	NS	14	2000	346.0	346.0	33.0
TLC2274CPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
TLC2274IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
TLC2274MDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC2274QDR	SOIC	D	14	2500	346.0	346.0	33.0

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

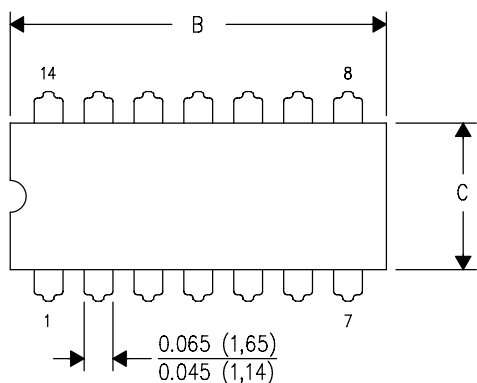


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification.
 - E. Falls within MIL STD 1835 GDIP1-T8

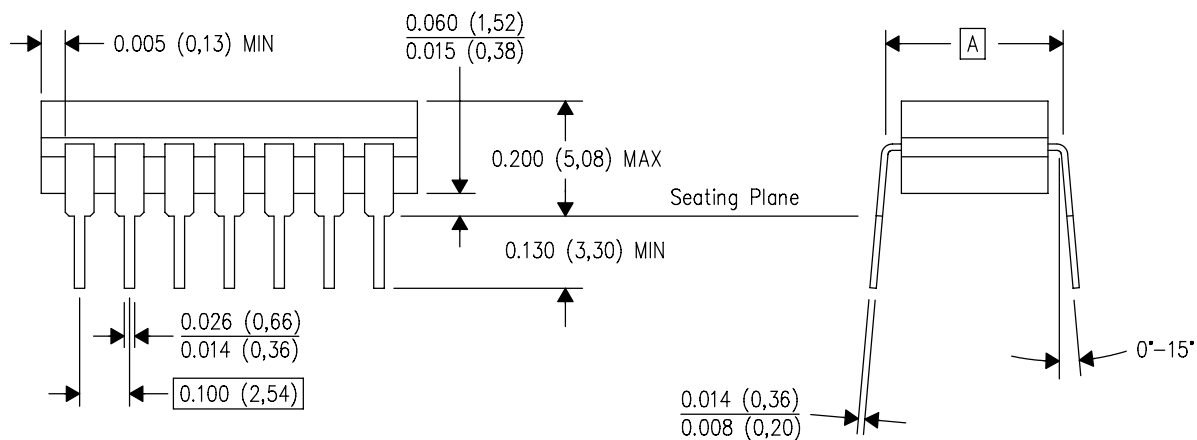
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

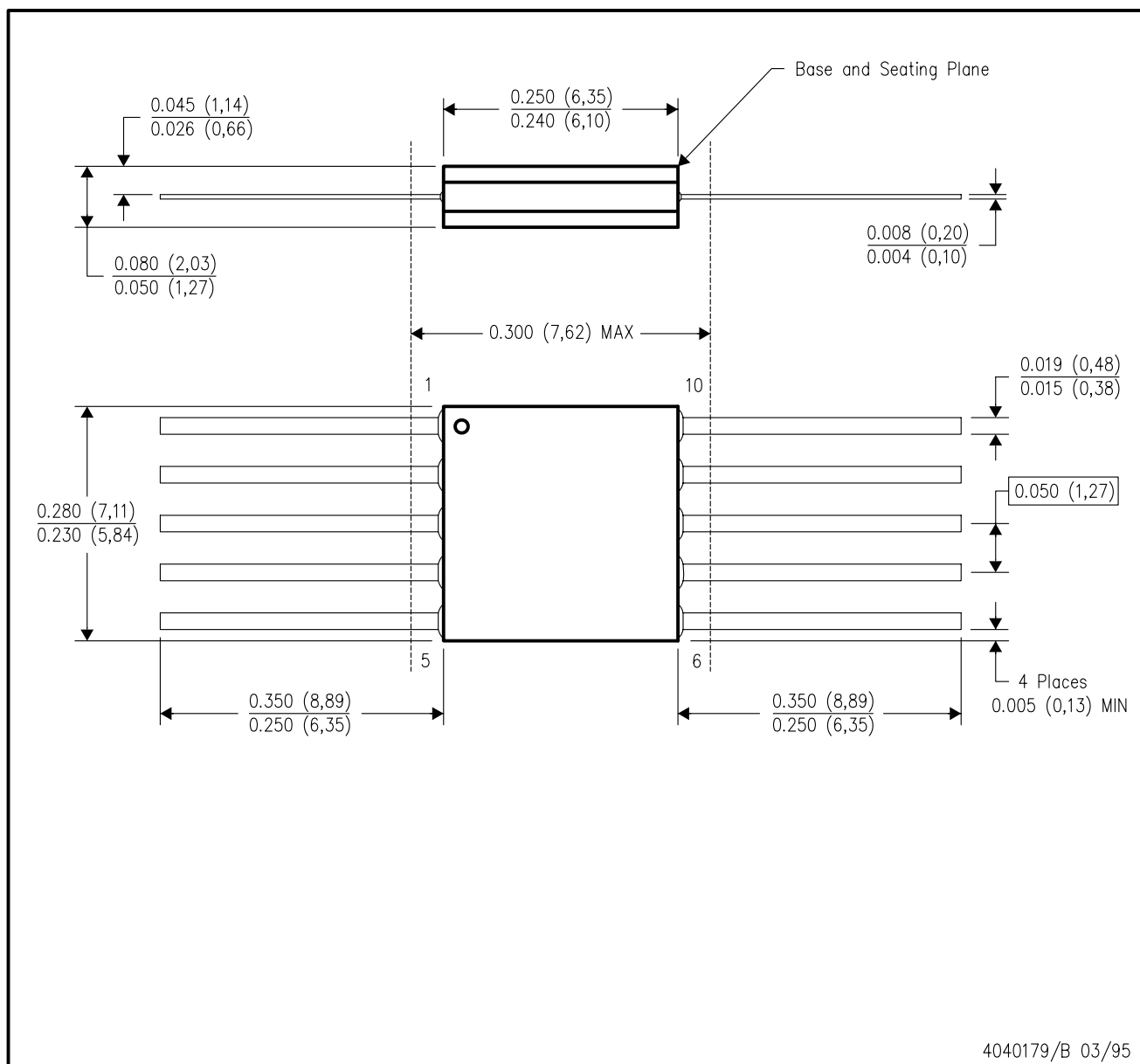


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

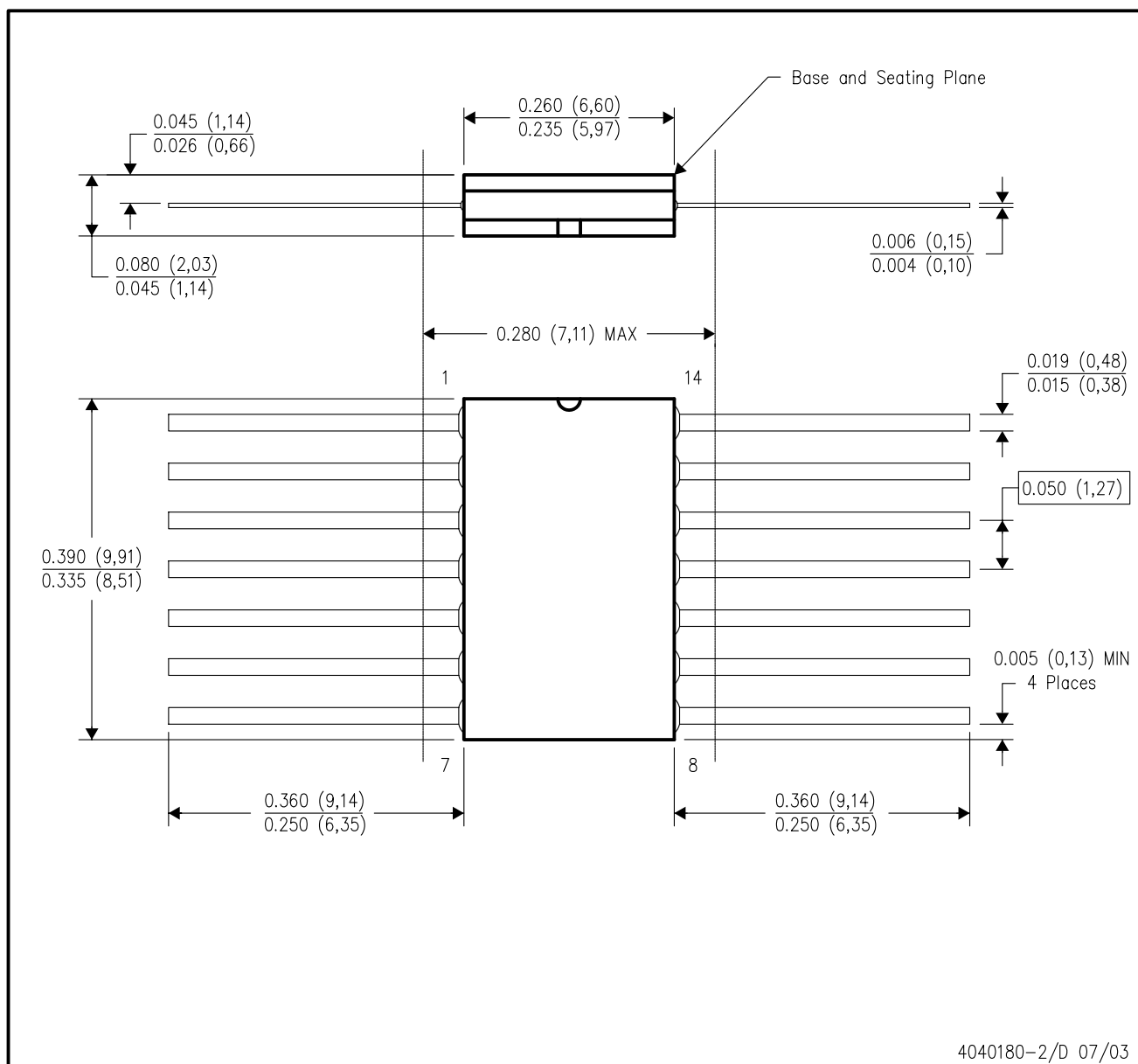
U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



W (R-GDFP-F14)

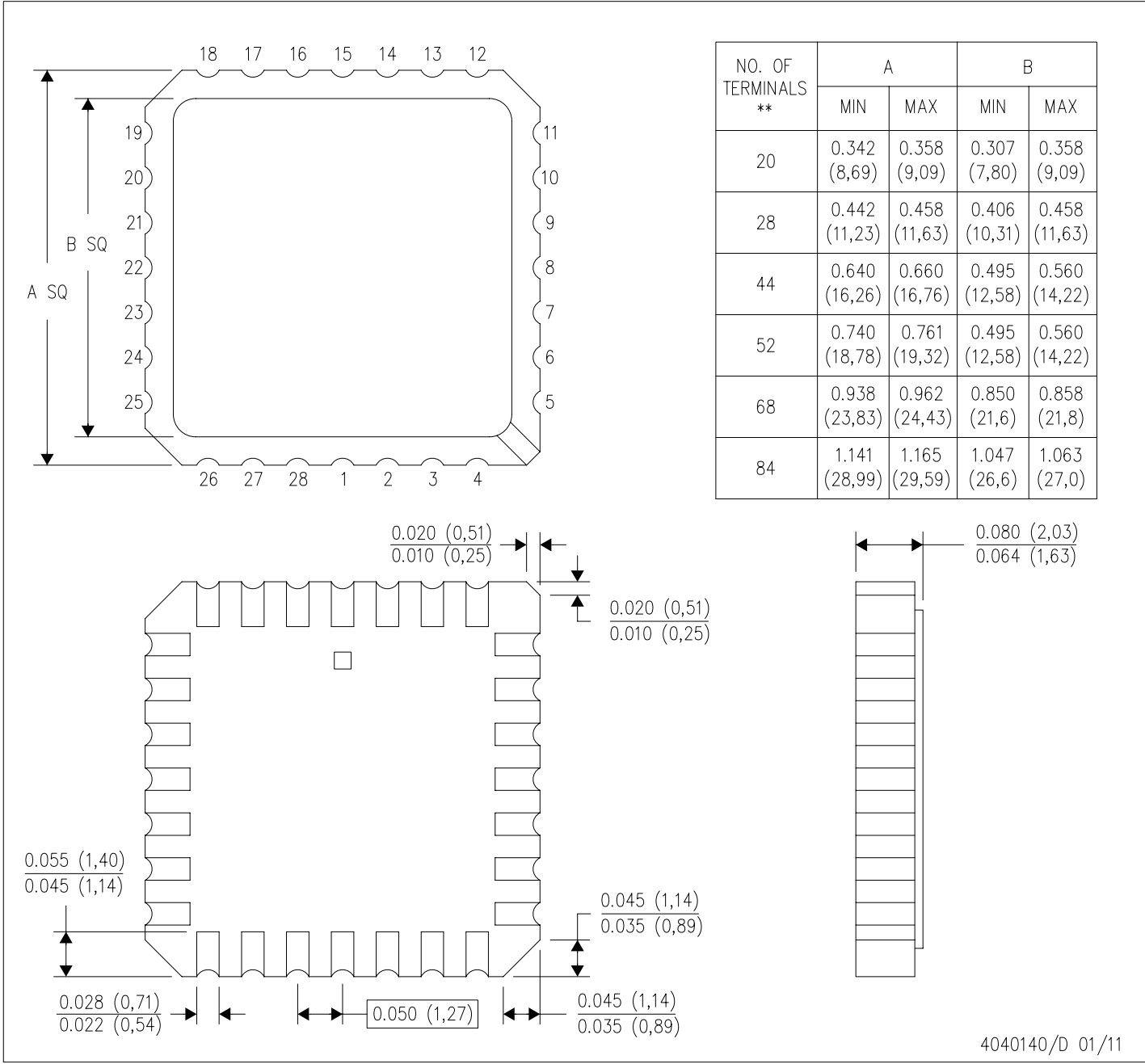
CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)
 28 TERMINAL SHOWN

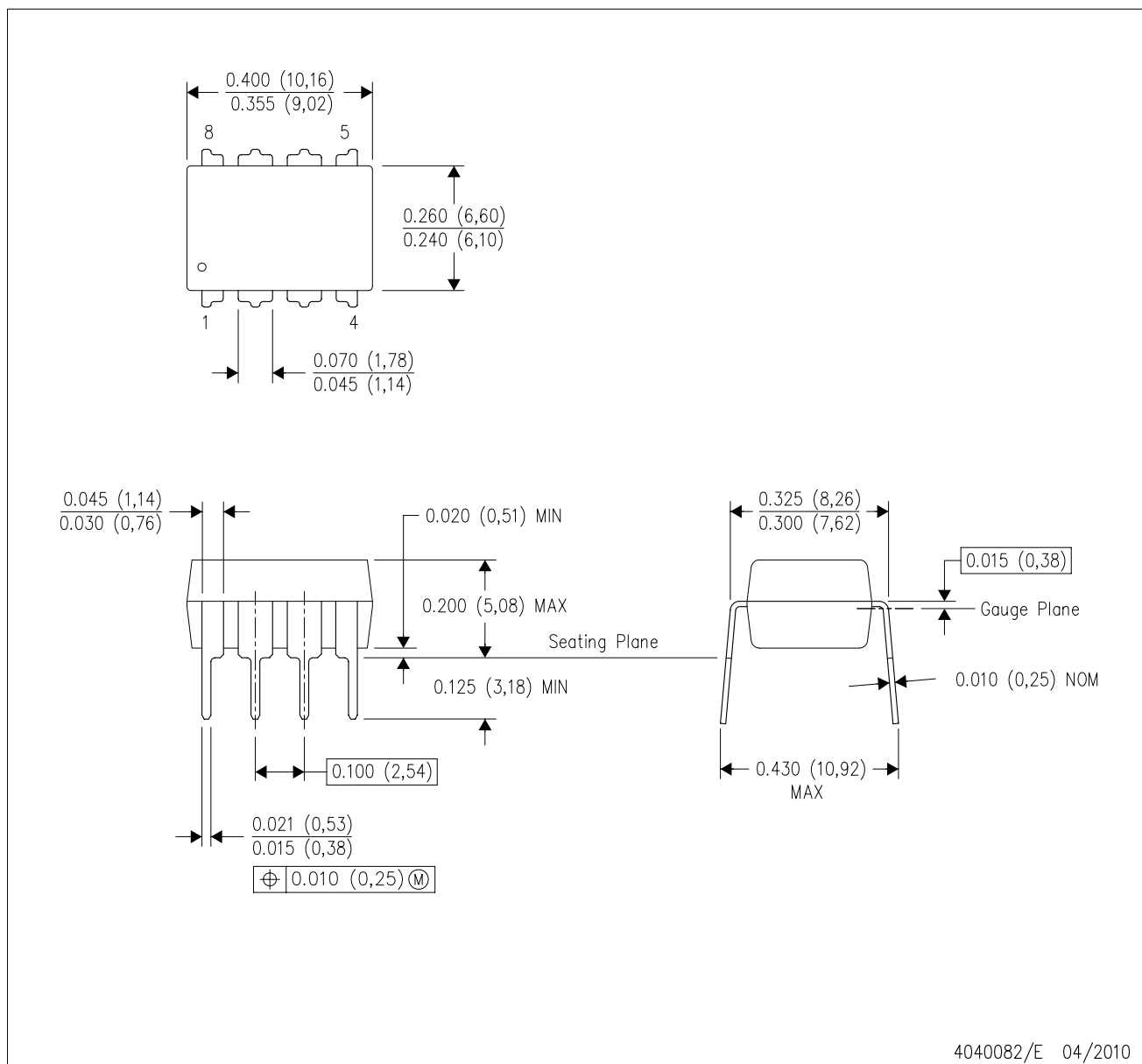
LEADLESS CERAMIC CHIP CARRIER



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. Falls within JEDEC MS-004

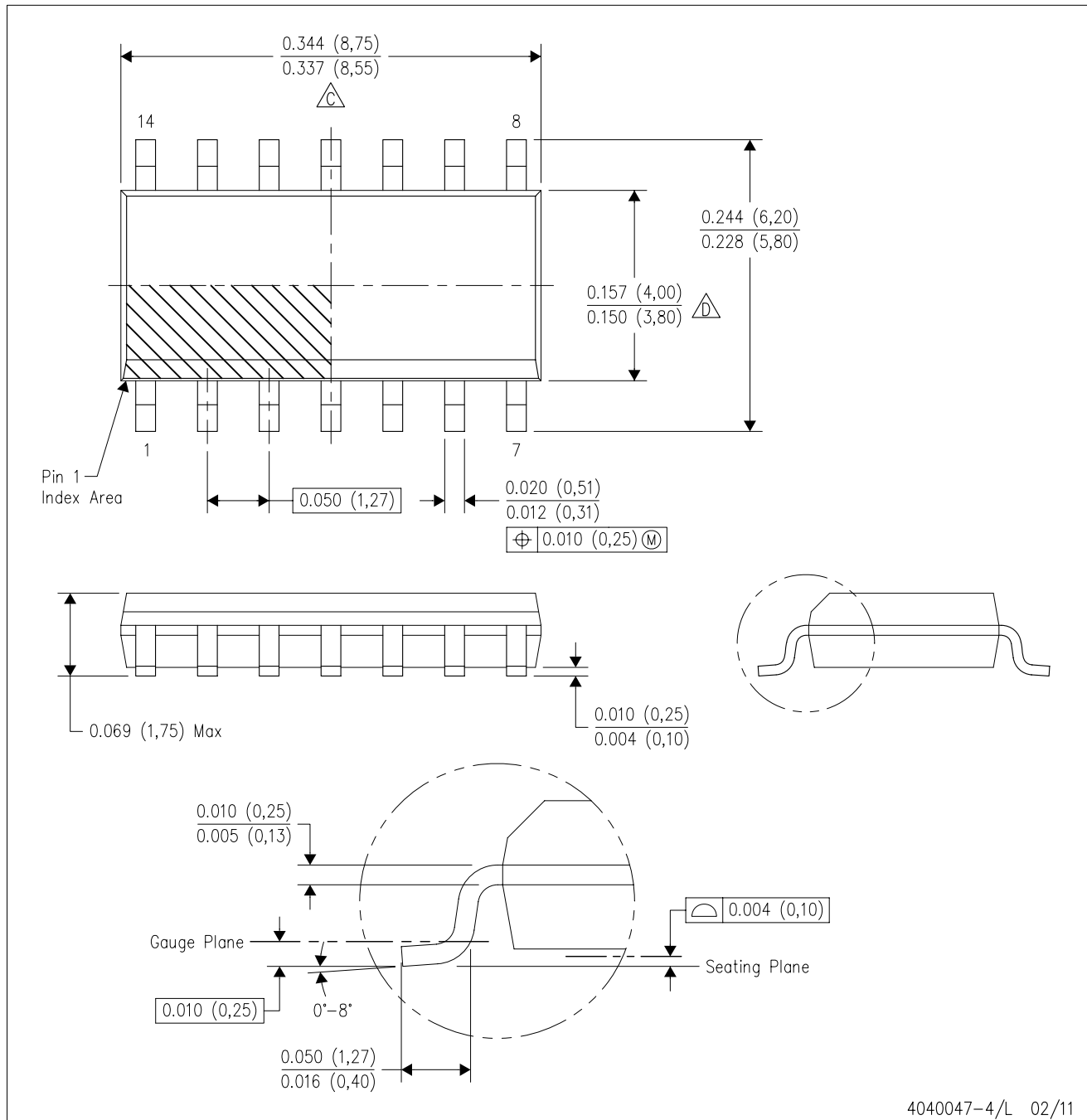
P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

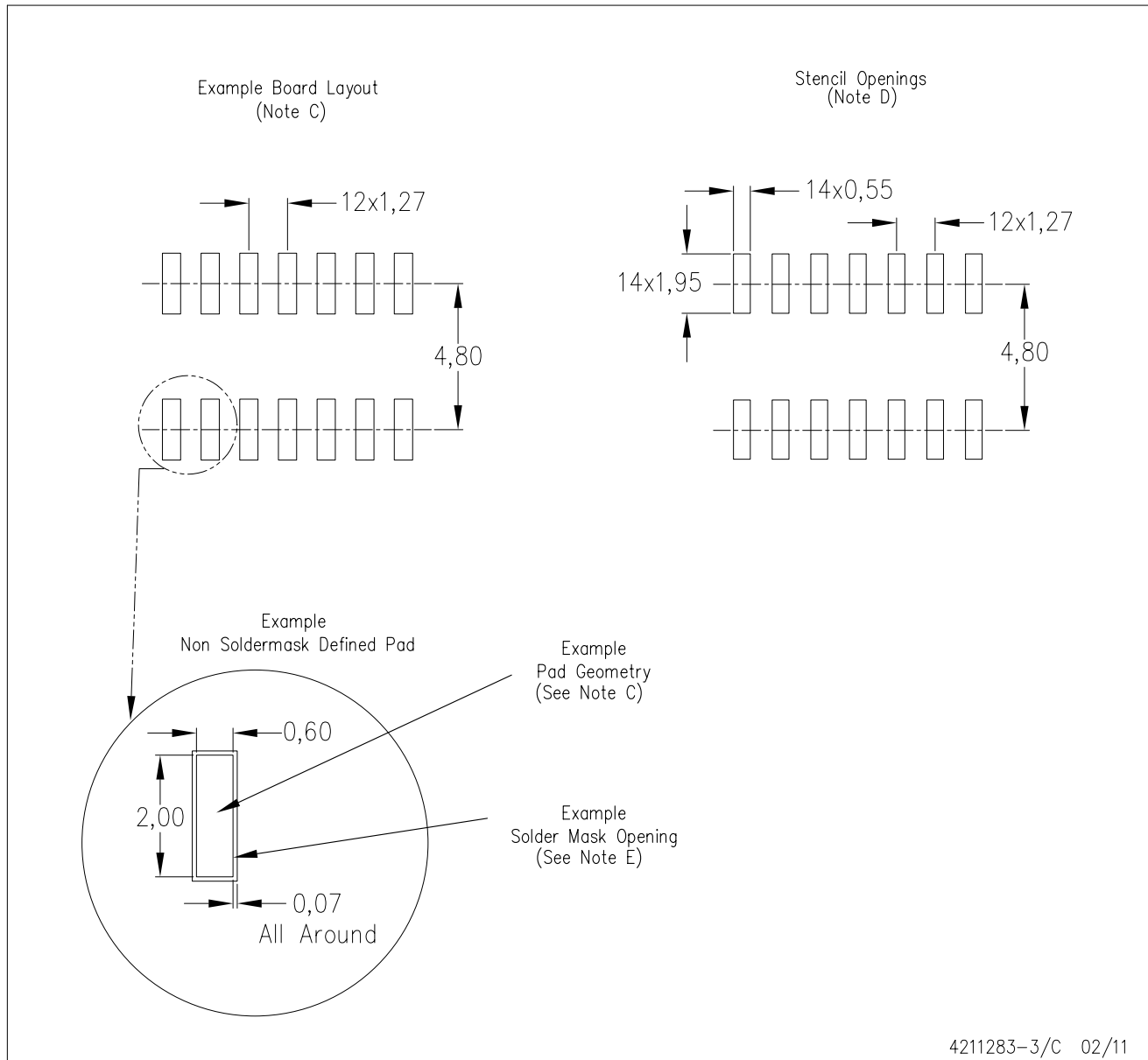


4040047-4/L 02/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

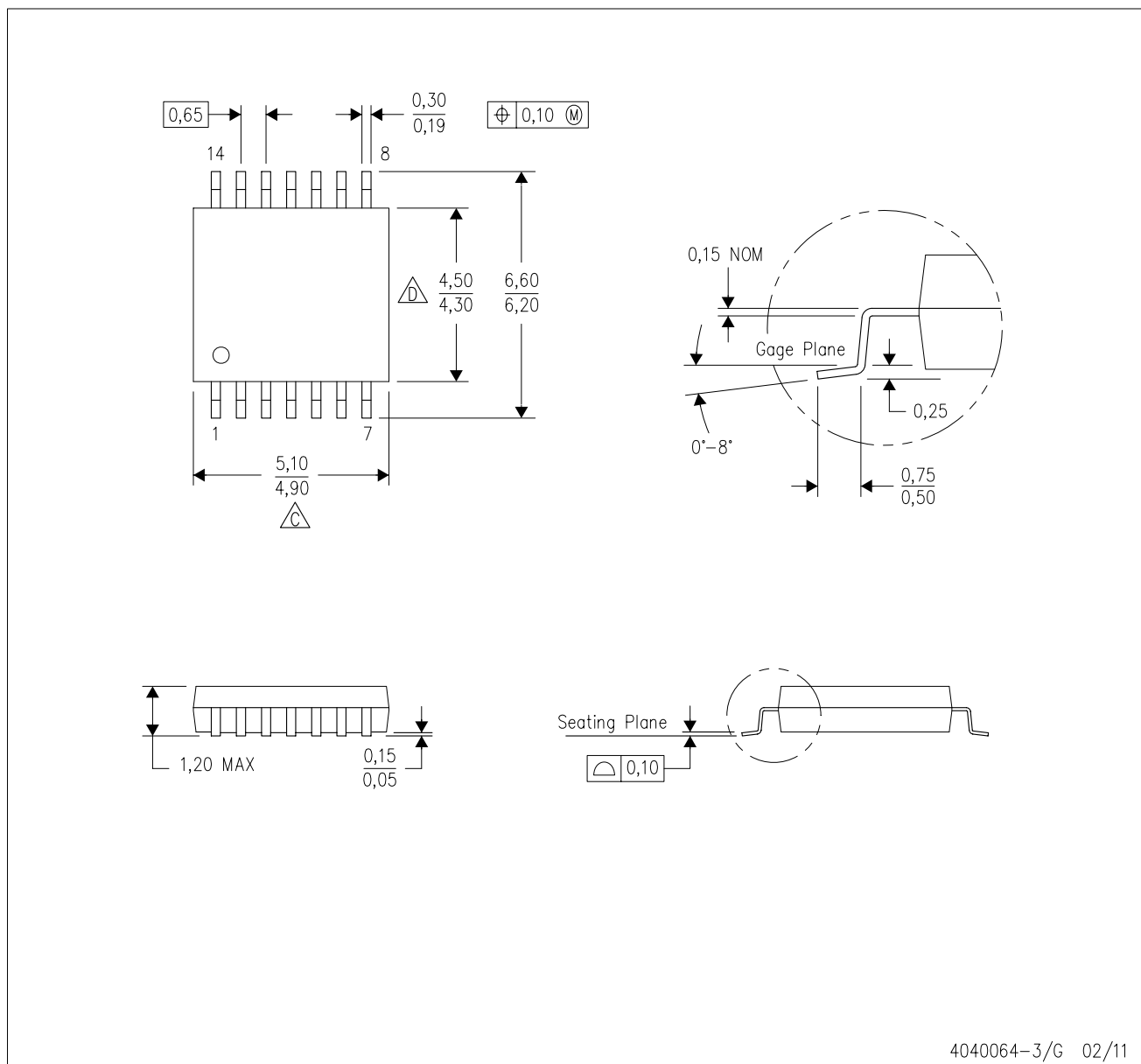


4211283-3/C 02/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

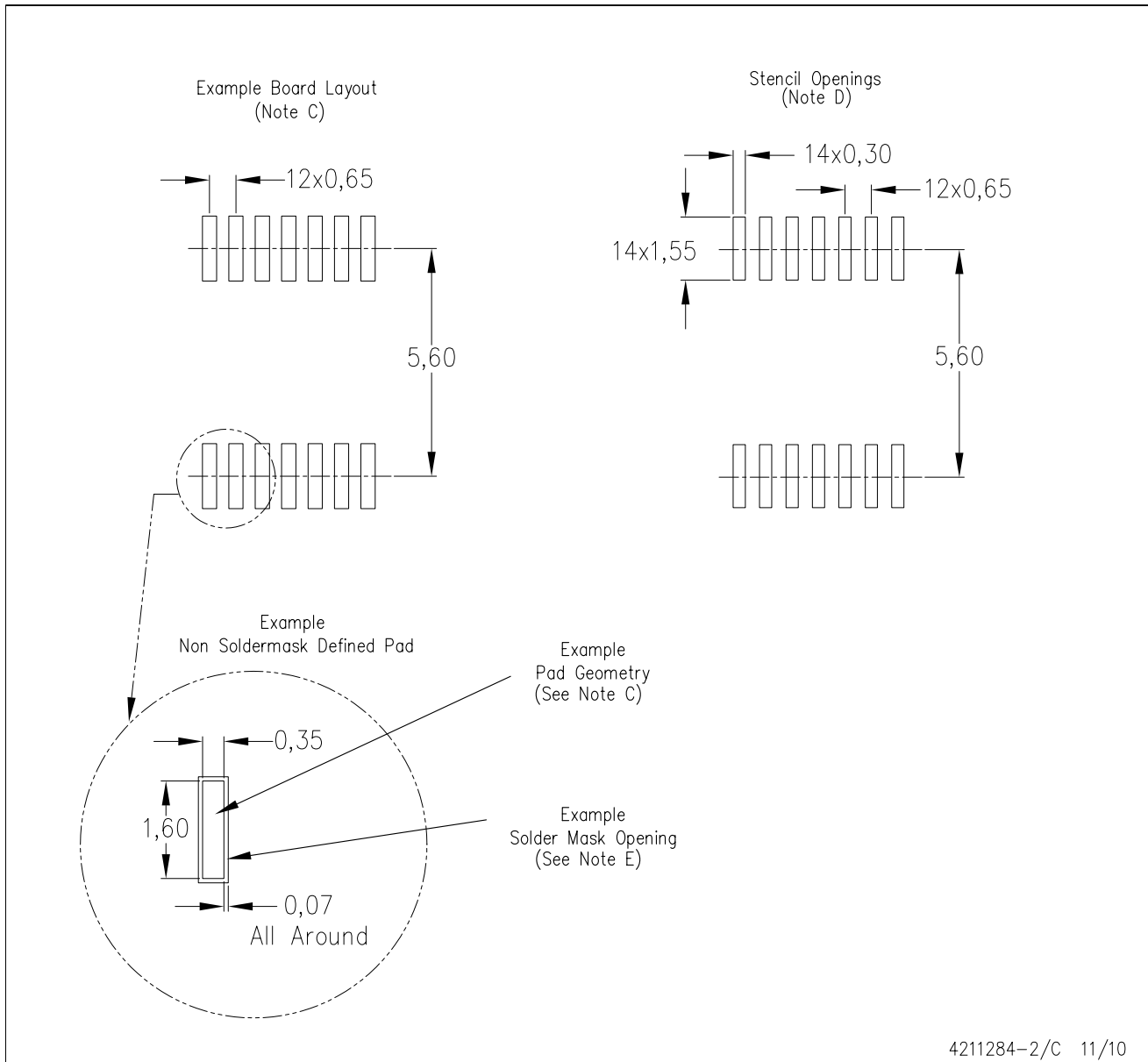


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

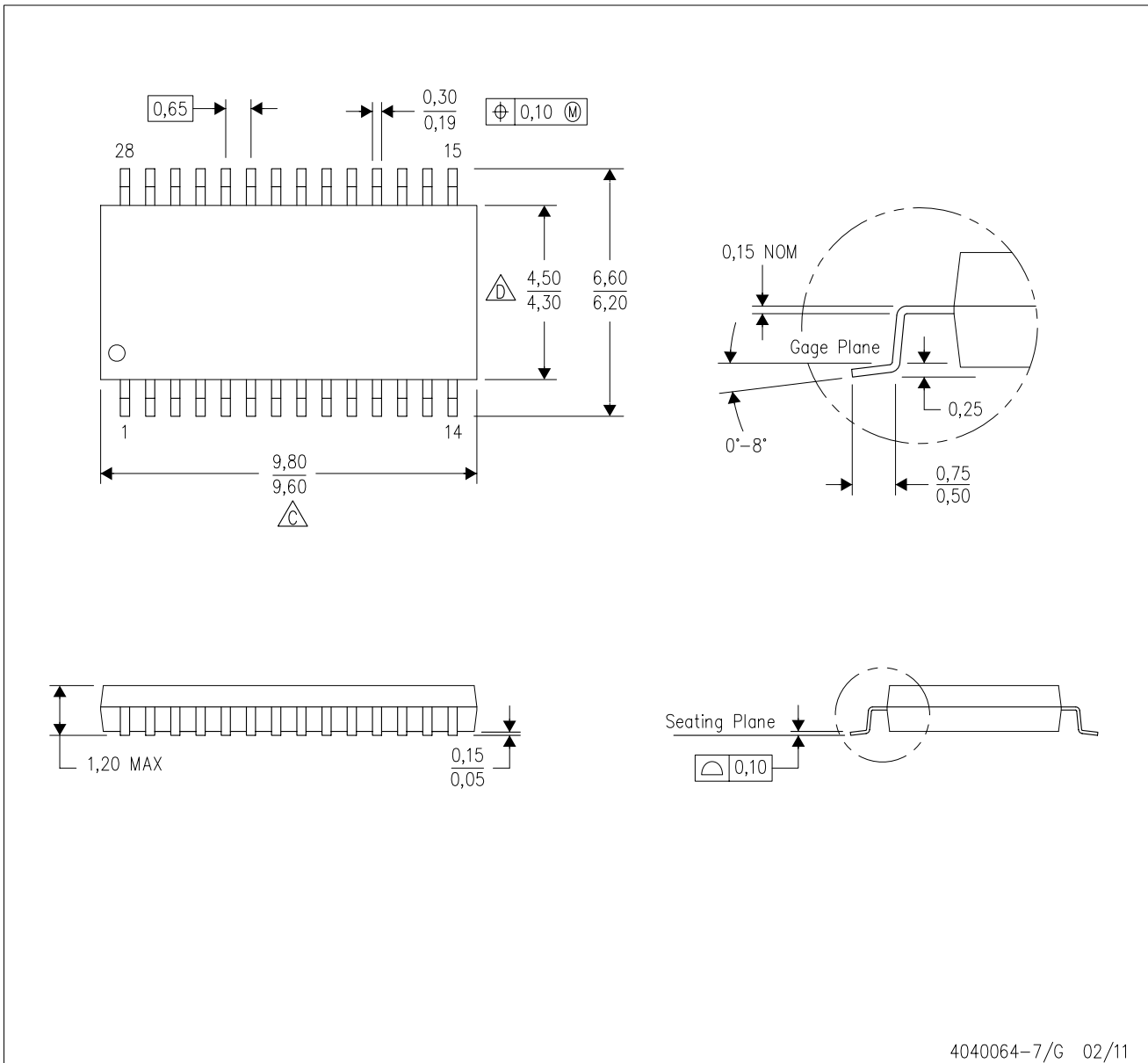
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

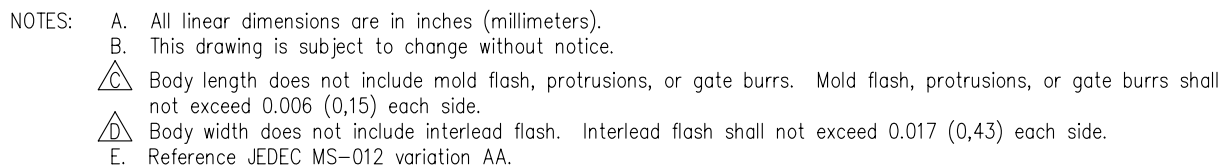
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



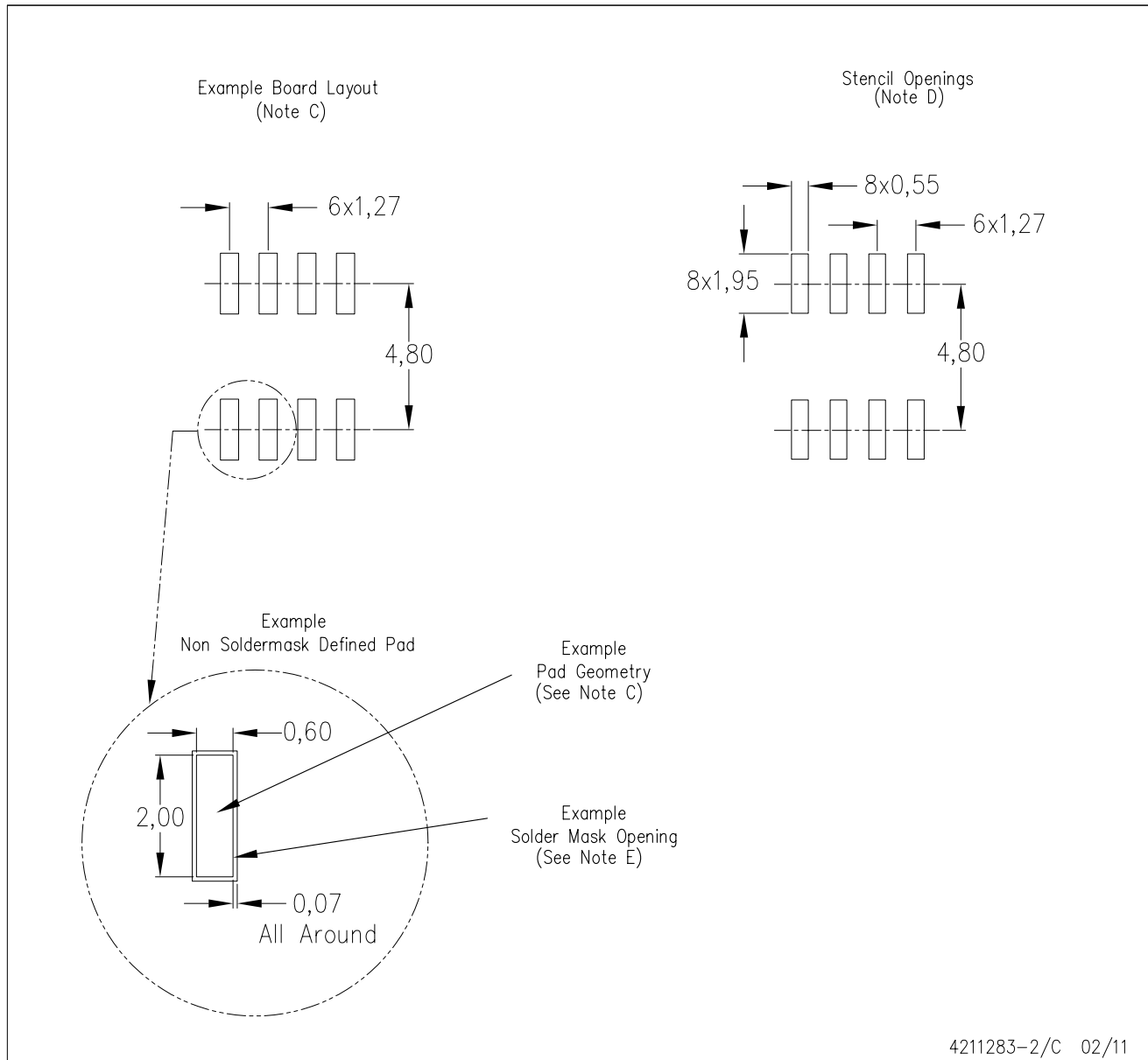
4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

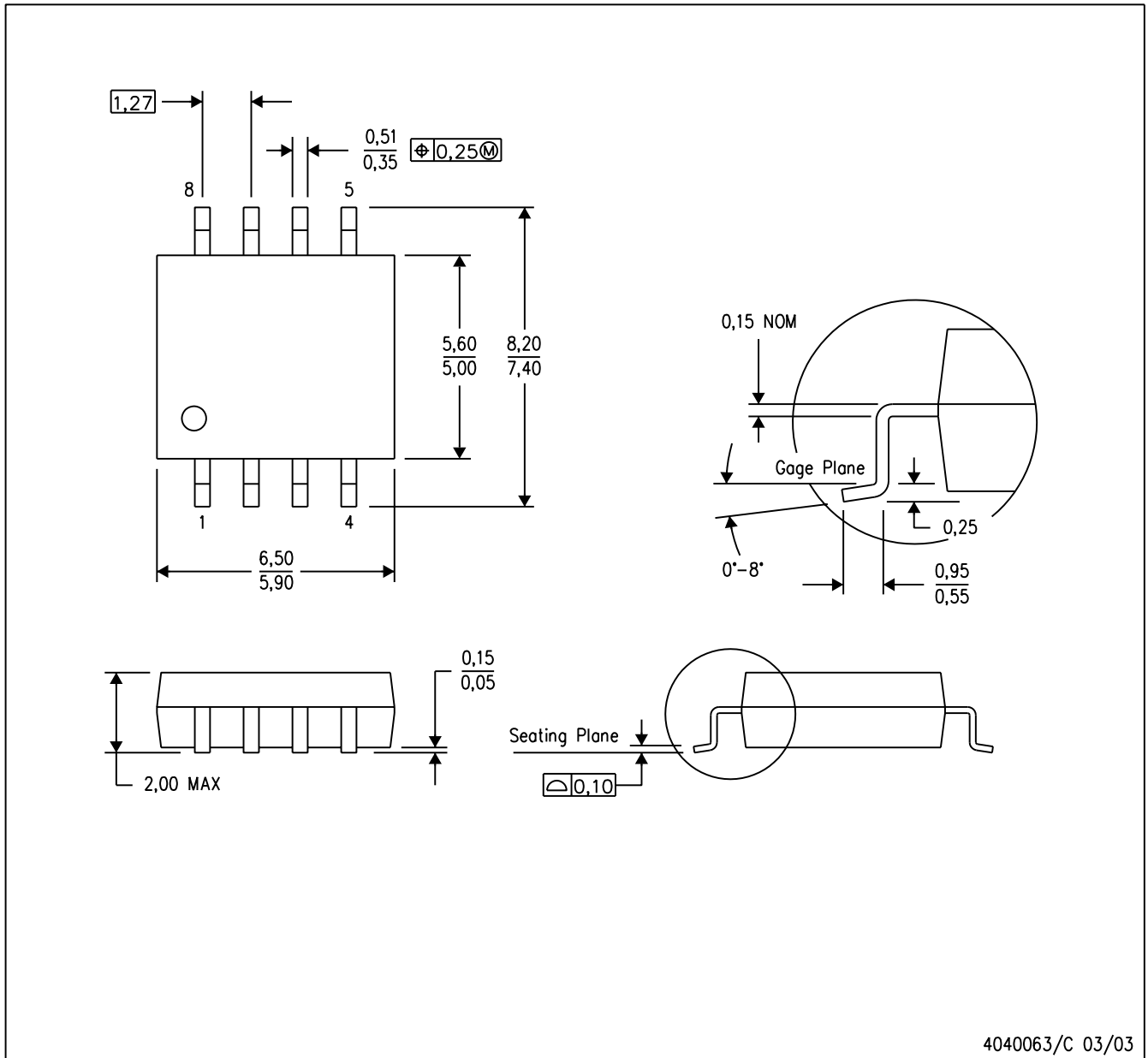


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



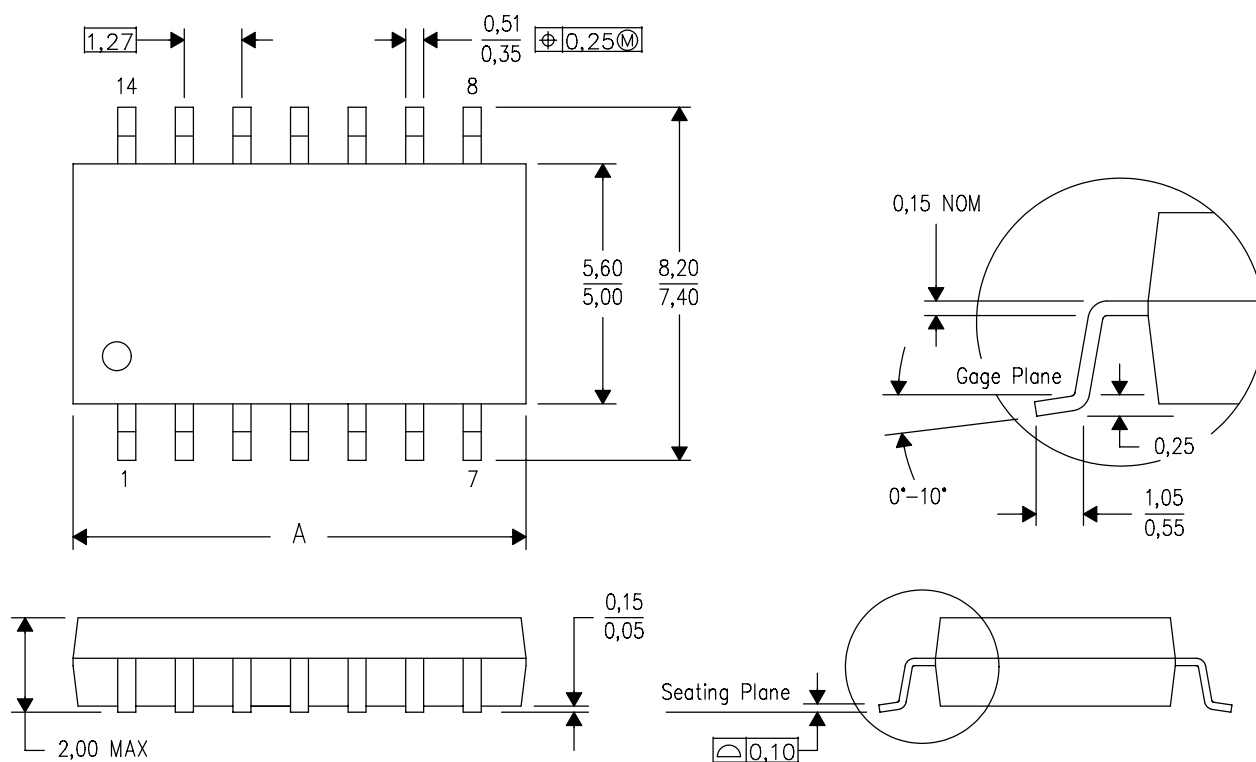
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



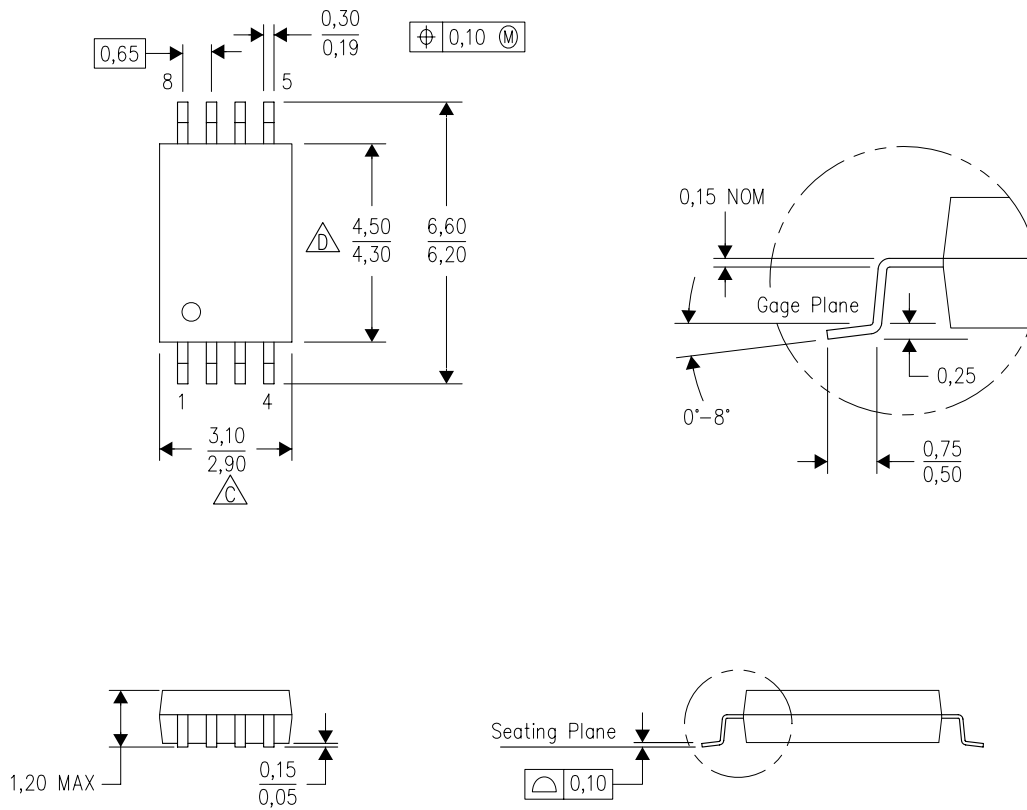
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153