UNIVERSAL ACTIVE FILTER

FEATURES

- **VERSATILE:**
  - **Low-Pass, High-Pass**
  - **Band-Pass, Band-Reject**
- **SIMPLE DESIGN PROCEDURE**
- **ACCURATE FREQUENCY AND Q:**
  - **Includes On-Chip 1000pF ±0.5% Capacitors**

APPLICATIONS

- **TEST EQUIPMENT**
- **COMMUNICATIONS EQUIPMENT**
- **MEDICAL INSTRUMENTATION**
- **DATA ACQUISITION SYSTEMS**
- **MONOLITHIC REPLACEMENT FOR UAF41**

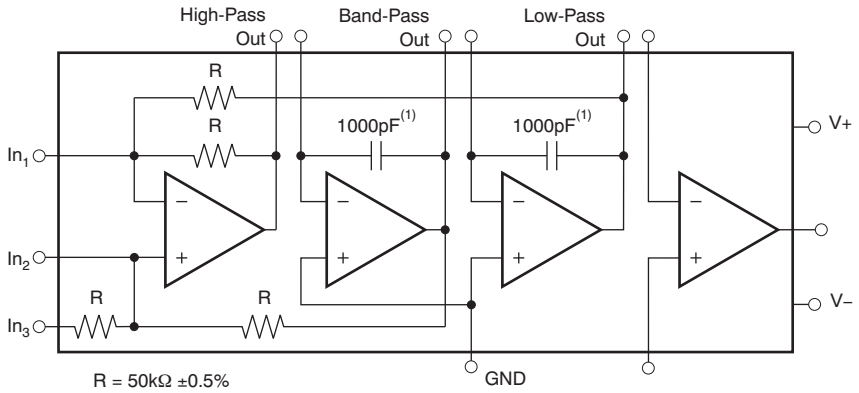
DESCRIPTION

The UAF42 is a universal active filter that can be configured for a wide range of low-pass, high-pass, and band-pass filters. It uses a classic state-variable analog architecture with an inverting amplifier and two integrators. The integrators include on-chip 1000pF capacitors trimmed to 0.5%. This architecture solves one of the most difficult problems of active filter design—obtaining tight tolerance, low-loss capacitors.

A DOS-compatible filter design program allows easy implementation of many filter types, such as Butterworth, Bessel, and Chebyshev. A fourth, uncommitted FET-input op amp (identical to the other three) can be used to form additional stages, or for special filters such as band-reject and Inverse Chebyshev.

The classical topology of the UAF42 forms a time-continuous filter, free from the anomalies and switching noise associated with switched-capacitor filter types.

The UAF42 is available in 14-pin plastic DIP and SOIC-16 surface-mount packages, specified for the –25°C to +85°C temperature range.



NOTE: (1) ±0.5%.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range unless otherwise noted.

	UAF42	UNIT
Power Supply Voltage	±18	V
Input Voltage	$\pm V_S$ ±0.7	V
Output Short-Circuit	Continuous	
Operating Temperature	–40 to +85	°C
Storage Temperature	–40 to +125	°C
Junction Temperature	+125	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended period may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

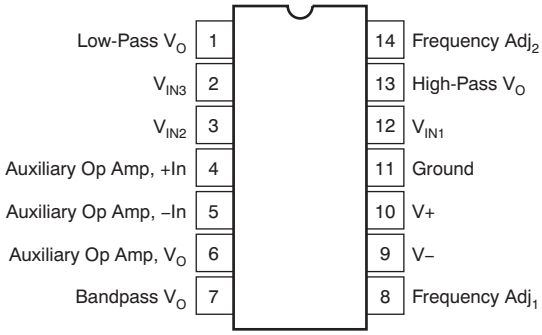
ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
UAF42AP	PDIP-14	N	UAF42AP
UAF42APG4			
UAF42AU	SOIC-16	DW	UAF42AU
UAF42AUE4			

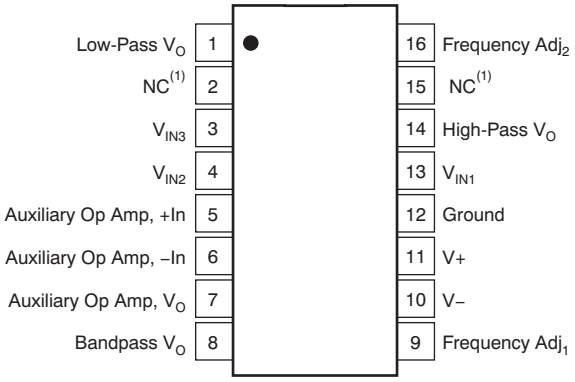
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI

PIN CONFIGURATIONS

P PACKAGE
PDIP-14
(TOP VIEW)



U PACKAGE
SOIC-16
(TOP VIEW)



NOTE: (1) NC = no connection. For best performance connect all *NC* pins to ground to minimize inter-lead capacitance.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

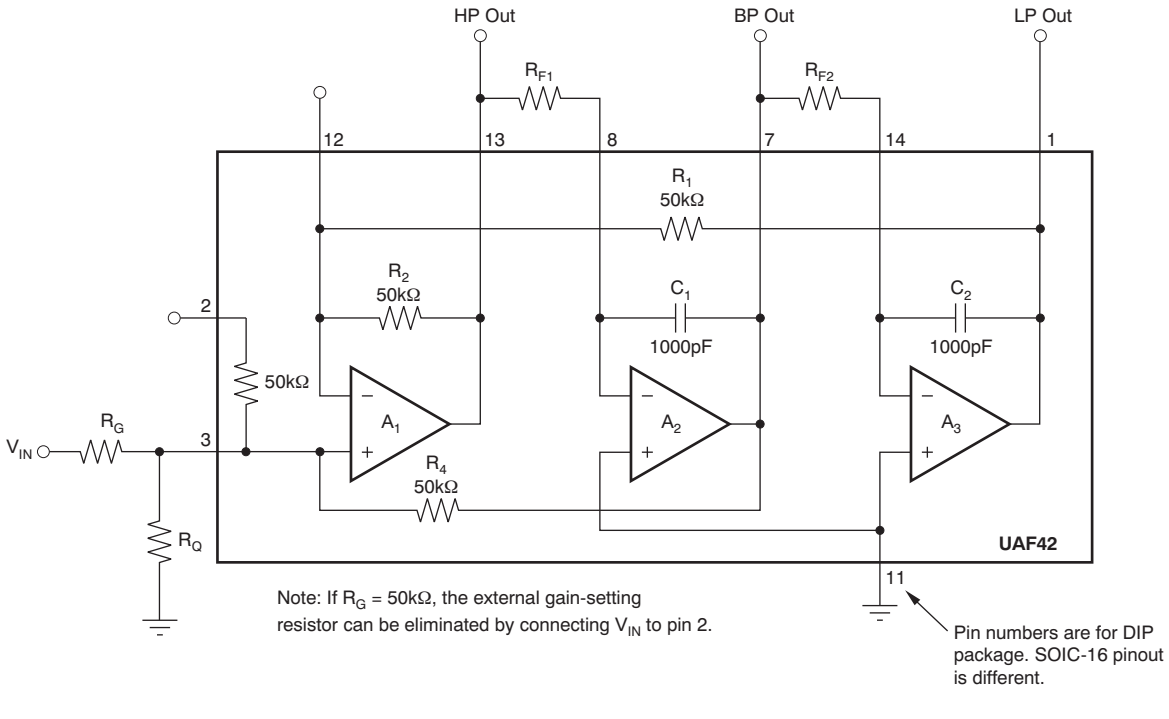
PARAMETER	CONDITIONS	UAF42AP, AU			UNIT
		MIN	TYP	MAX	
FILTER PERFORMANCE					
Frequency Range, f_n			0 to 100		kHz
Frequency Accuracy	f = 1kHz			1	%
vs Temperature			0.01		%/°C
Maximum Q			400		—
Maximum (Q • Frequency) Product			500		kHz
Q vs Temperature	$(f_O \bullet Q) < 10^4$		0.01		%/°C
	$(f_O \bullet Q) < 10^5$		0.025		%/°C
Q Repeatability	$(f_O \bullet Q) < 10^5$		2		%
Offset Voltage, Low-Pass Output				±5	mV
Resistor Accuracy			0.5	1	%
OFFSET VOLTAGE(1)					
Input Offset Voltage			±0.5	±5	mV
vs Temperature			±3		µV/°C
vs Power Supply	V_S = ±6V to ±18V	80	96		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		10	50	pA
Input Offset Current	V_{CM} = 0V		5		pA
NOISE					
Input Voltage Noise					
Noise Density: f = 10Hz			25		nV/√Hz
Noise Density: f = 10kHz			10		nV/√Hz
Voltage Noise: BW = 0.1Hz to 10Hz			2		μV_{PP}
Input Bias Current Noise					
Noise Density: f = 10kHz			2		fA/√Hz
INPUT VOLTAGE RANGE(1)					
Common-Mode Input Range			±11.5		V
Common-Mode Rejection	V_{CM} = ±10V	80	96		dB
INPUT IMPEDANCE(1)					
Differential			10^{13} || 2		Ω || pF
Common-Mode			10^{13} || 6		Ω || pF
OPEN-LOOP GAIN(1)					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	90	126		dB
FREQUENCY RESPONSE					
Slew Rate			10		V/µs
Gain-Bandwidth Product	G = +1		4		MHz
Total Harmonic Distortion	G = +1, f = 1kHz		0.1		%
OUTPUT(1)					
Voltage Output	R_L = 2kΩ	±11	±11.5		V
Short Circuit Current			±25		mA

(1) Specifications apply to uncommitted op amp, A_4. The three op amps forming the filter are identical to A_4 but are tested as a complete filter.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_S = ±15V, unless otherwise noted.

PARAMETER	CONDITIONS	UAF42AP, AU			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±6		±18	V
Current			±6	±7	mA
TEMPERATURE RANGE					
Specified		–25		+85	°C
Operating		–25		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W



Design Equations

1. $$\omega_n^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$$

2. $$= \frac{1 + \dfrac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \dfrac{R_2}{R_1}} \left(\frac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2} \right)^{1/2}$$

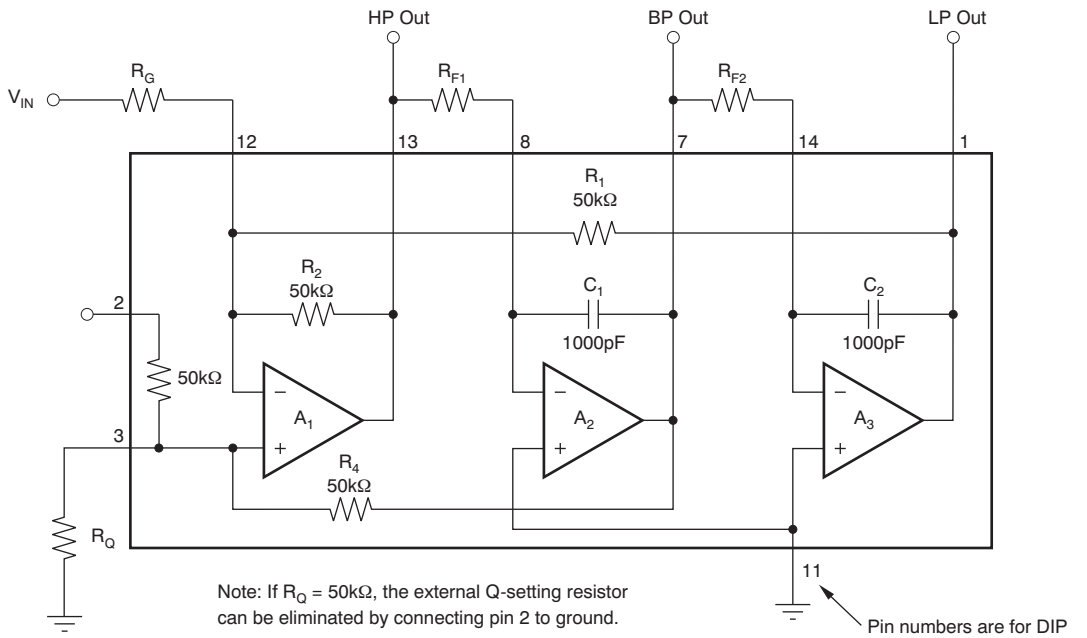
3. $$_{LP} = QA_{HP} \left(\frac{R_1}{R_2} \right) = A_{BP} \left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2} \right)^{1/2}$$

4. $$A_{LP} = \frac{1 + \dfrac{R_1}{R_2}}{R_G \left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4} \right)}$$

5. $$_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{1 + \dfrac{R_2}{R_1}}{R_G \left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4} \right)}$$

6. $$A_{BP} = \frac{R_4}{R_G}$$

Figure 1. Noninverting Pole-Pair



Design Equations

1. $\omega_n^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \left(1 + \dfrac{R_4}{R_Q}\right) \dfrac{1}{\left(\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_G}\right)} \left(\dfrac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$

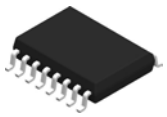
3. $QA_{LP} = QA_{HP}\left(\dfrac{R_1}{R_2}\right) = A_{BP}\left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{R_1}{R_G}$

5. $A_{HP} = \dfrac{R_2}{R_1} A_{LP} = \dfrac{R_2}{R_G}$

6. $A_{BP} = \left(1 + \dfrac{R_4}{R_Q}\right) \dfrac{1}{R_G\left(\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_G}\right)}$

Figure 2. Inverting Pole-Pair

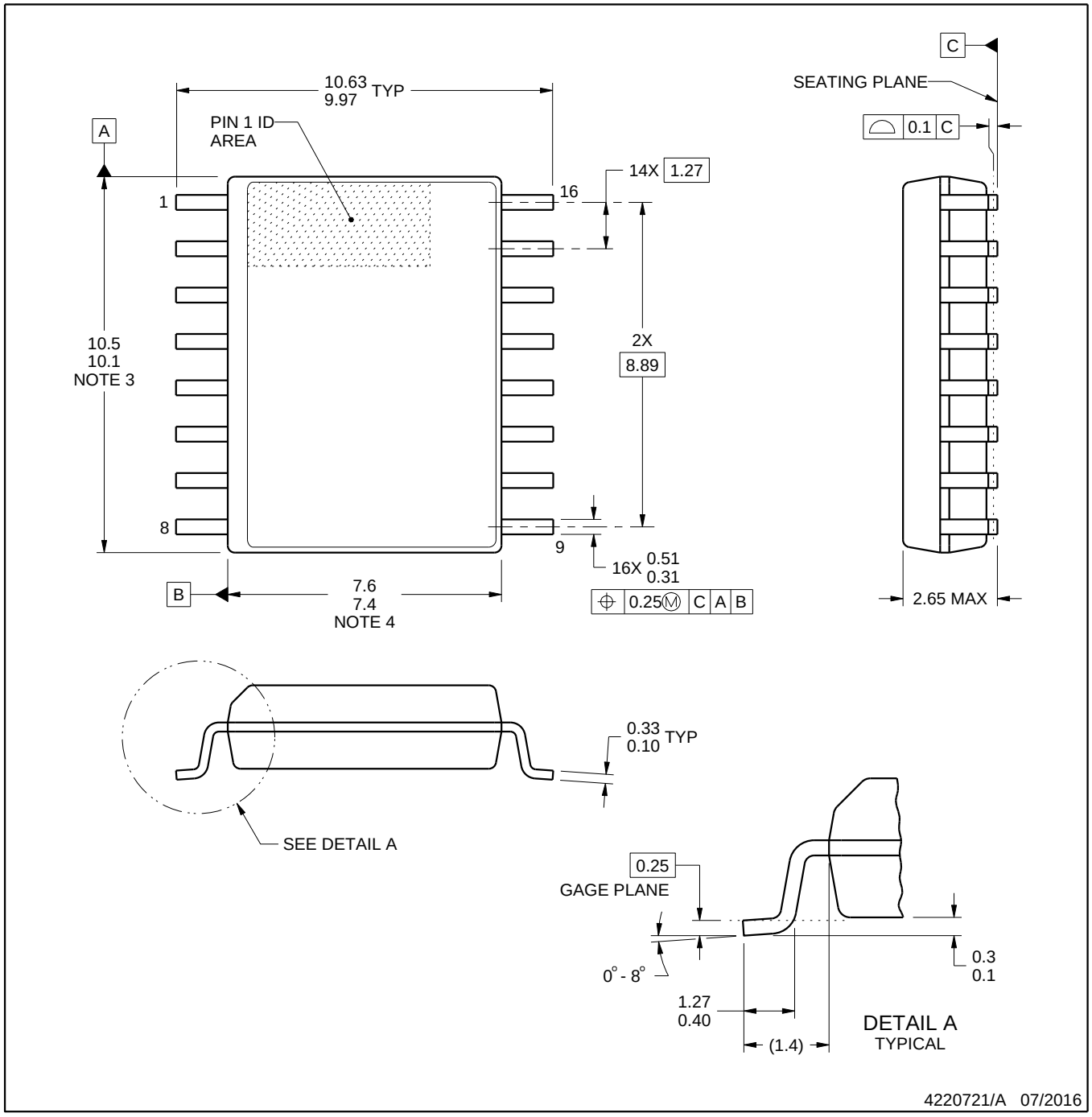


PACKAGE OUTLINE

DW0016A

SOIC - 2.65 mm max height

SOIC

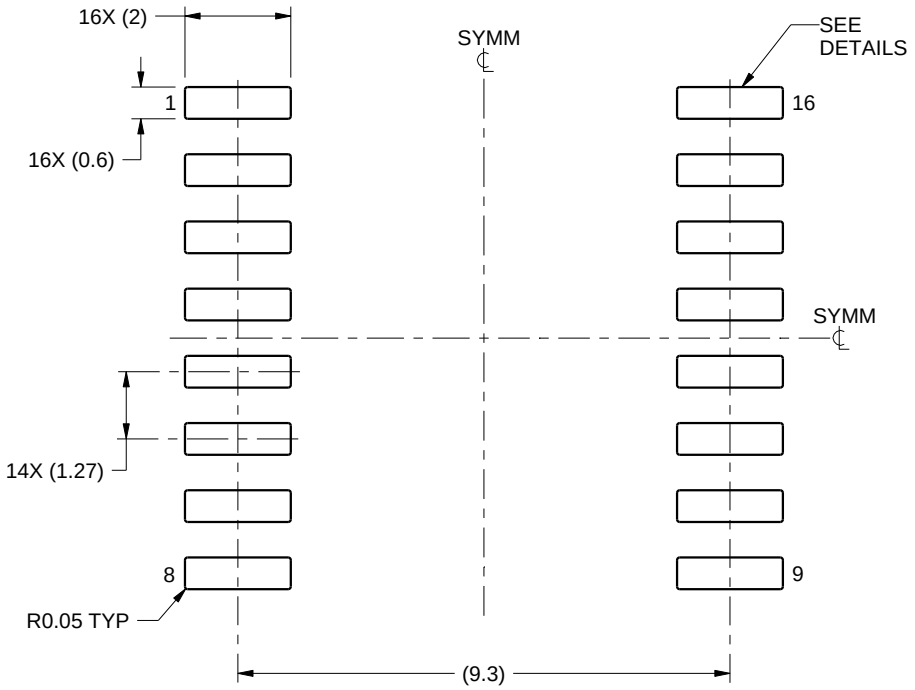


EXAMPLE BOARD LAYOUT

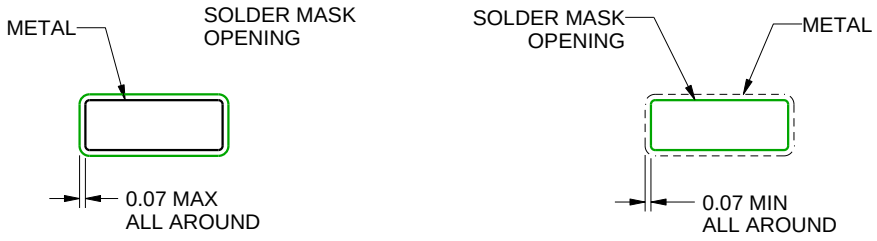
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

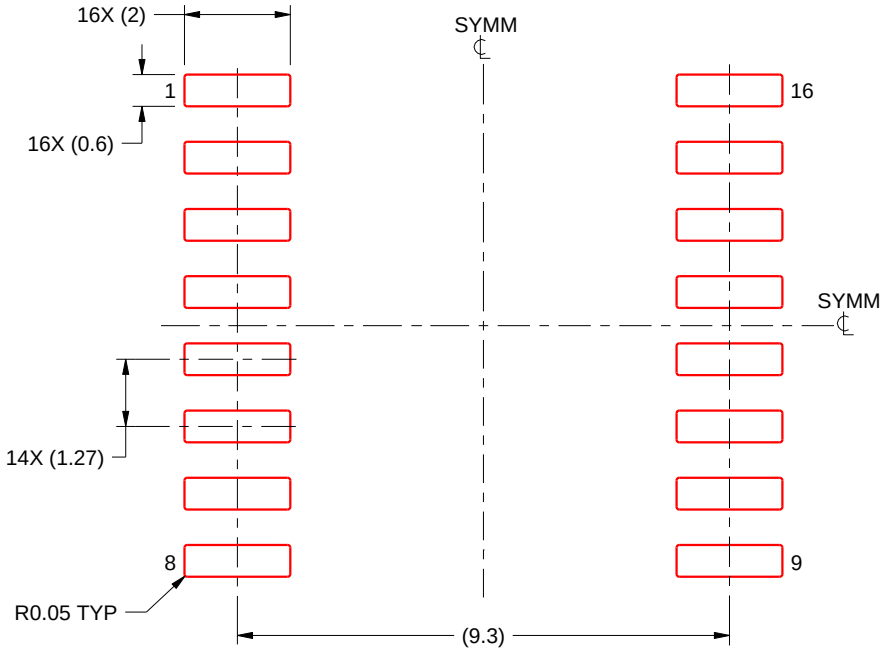
4220721/A 07/2016

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



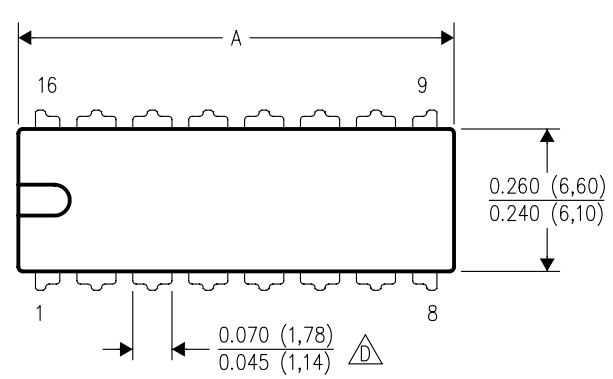
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

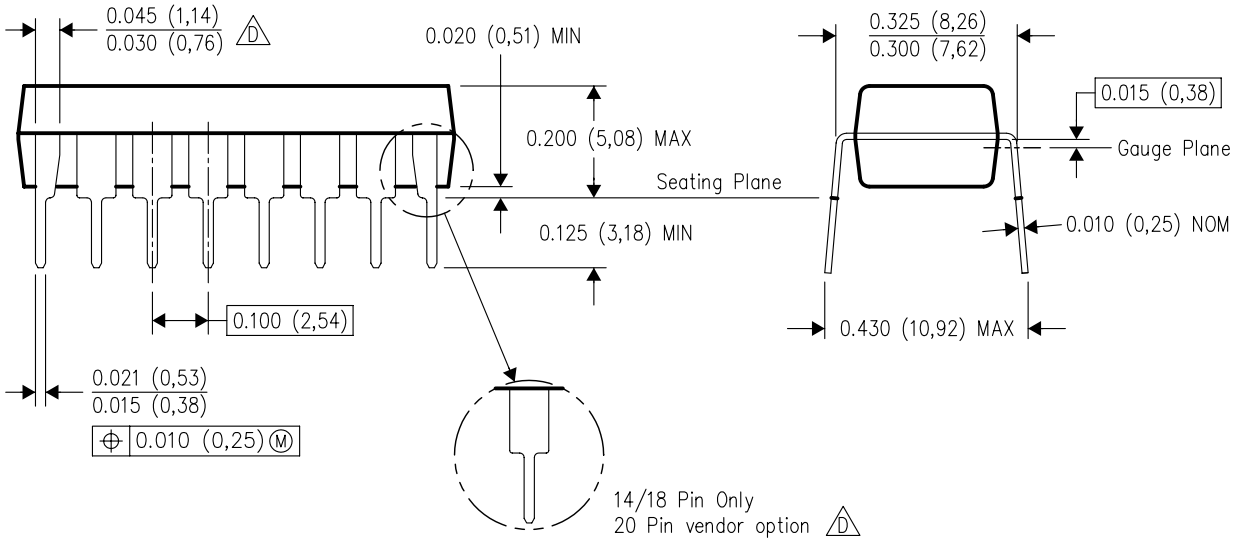
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.