



UC1524A
UC2524A
UC3524A

Advanced Regulating Pulse Width Modulators

FEATURES

- Fully Interchangeable with Standard UC1524 Family
- Precision Reference Internally Trimmed to $\pm 1\%$
- High-Performance Current Limit Function
- Under-Voltage Lockout with Hysteretic Turn-on
- Start-Up Supply Current Less Than 4mA
- Output Current to 200mA
- 60V Output Capability
- Wide Common-Mode Input Range for both Error and Current Limit Amplifiers
- PWM Latch Insures Single Pulse per Period
- Double Pulse Suppression Logic
- 200ns Shutdown through PWM Latch
- Guaranteed Frequency Accuracy
- Thermal Shutdown Protection

DESCRIPTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

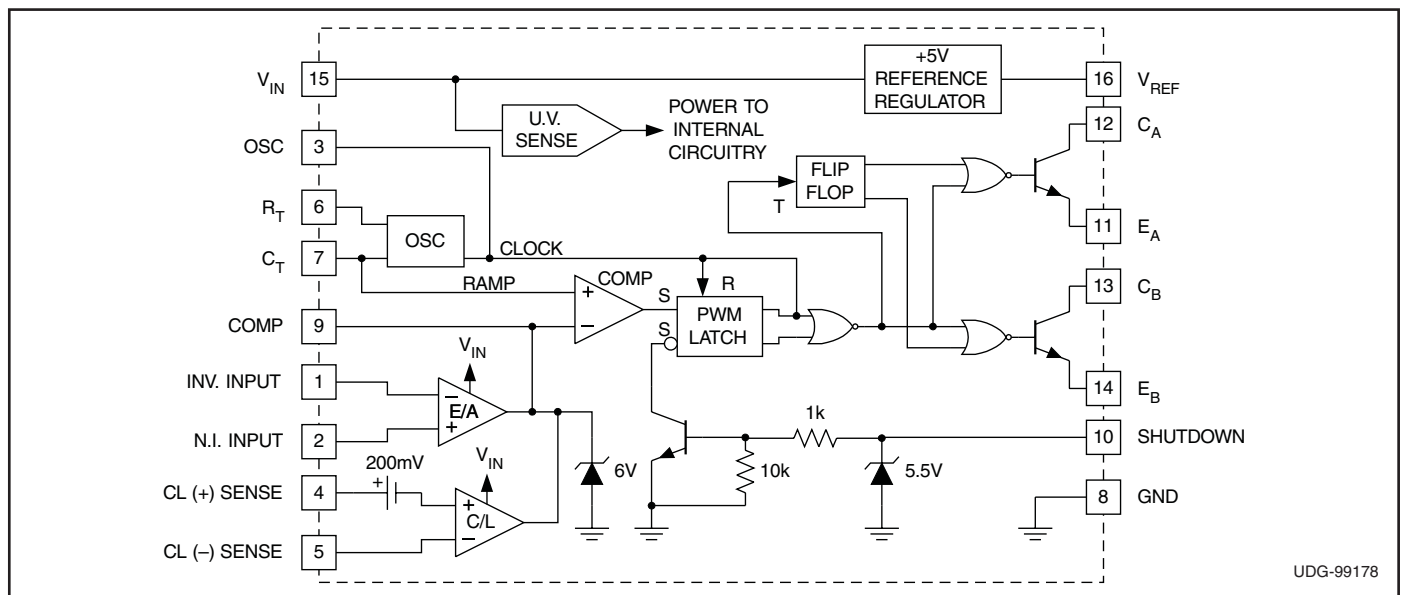
The UC1524A includes a precise 5V reference trimmed to $\pm 1\%$ accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter-free activation.

Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments, logic to eliminate double pulsing on a single output, a 200ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit of the UC1524A is usable beyond 500kHz and is now easier to synchronize with an external clock pulse.

The UC1524A is packaged in a hermetic 16-pin DIP and is rated for operation from -55°C to $+125^{\circ}\text{C}$. The UC2524A and 3524A are available in either ceramic or plastic packages and are rated for operation from -25°C to $+85^{\circ}\text{C}$ and 0°C to 70°C , respectively. Surface mount devices are also available.

BLOCK DIAGRAM



SLUS181A - NOVEMBER 1999

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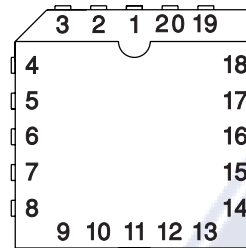
ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------|
| Supply Voltage (VIN) | 40V |
| Collector Supply Voltage (Vc) | 60V |
| Output Current (each Output) | 200mA |
| Maximum Forced Voltage (Pin 9, 10) | -3 to +5V |
| Maximum Forced Current (Pin 9, 10) | ±10mA |
| Reference Output Current | 50mA |
| Oscillator Charging Current | 5mA |
| Power Dissipation at TA = +25°C | 1000mW |
| Power Dissipation at Tc = +25°C | 2000mW |
| Operating Temperature Range | -55°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature, (Soldering, 10 seconds) | +300°C |

Note: Consult packaging section of Databook for thermal limitations and considerations of package.

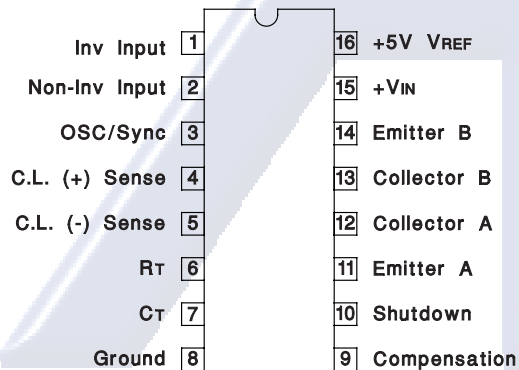
CONNECTION DIAGRAMS

PLCC-20, LCC-20 (TOP VIEW)
Q or L Package



| PACKAGE PIN FUNCTION | |
|----------------------|-----|
| FUNCTION | PIN |
| N/C | 1 |
| Inv. Input | 2 |
| Non-Inv. Input | 3 |
| OSC/SYNC | 4 |
| C.L. (+) sense | 5 |
| N/C | 6 |
| C.L. (-) sense | 7 |
| RT | 8 |
| CT | 9 |
| Ground | 10 |
| N/C | 11 |
| Compensation | 12 |
| Shutdown | 13 |
| Emitter A | 14 |
| Collector A | 15 |
| N/C | 16 |
| Collector B | 17 |
| Emitter B | 18 |
| +VIN | 19 |
| +5V VREF | 20 |

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; VIN = Vc = 20V, TA = TJ.

| PARAMETER | TEST CONDITIONS | UC1524A / UC2524A | | | UC3524A | | | UNITS |
|--------------------------------|-------------------------------|-------------------|------|------|---------|------|------|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Turn-on Characteristics | | | | | | | | |
| Input Voltage | Operating Range after Turn-on | 8 | | 40 | 8 | | 40 | V |
| Turn-on Threshold | | 6.5 | 7.5 | 8.5 | 6.5 | 7.5 | 8.5 | V |
| Turn-on Current | VIN = 6V | | 2.5 | 4 | | 2.5 | 4 | mA |
| Operating Current | VIN = 8 to 40V | | 5 | 10 | | 5 | 10 | mA |
| Turn-on Hysteresis* | | | 0.5 | | | 0.5 | | V |
| Reference Section | | | | | | | | |
| Output Voltage | TJ = 25°C | 4.95 | 5.00 | 5.05 | 4.90 | 5.00 | 5.10 | V |
| | Over Operating Range | 4.9 | | 5.1 | 4.85 | | 5.15 | V |
| Line Regulation | VIN = 10 to 40V | | 10 | 20 | | 10 | 30 | mV |
| Load Regulation | IL = 0 to 20 mA | | 20 | 25 | | 20 | 35 | mV |
| Temperature Stability* | Over Operating Range* | | 20 | 25 | | 20 | 35 | mV |
| Short Circuit Current | VREF = 0, 25°C ≤ TJ ≤ 125°C | | 80 | 100 | | 80 | 100 | mA |
| Output Noise Voltage* | 10Hz ≤ f ≤ 10kHz, TJ = 25°C | | 40 | | | 40 | | µVrms |
| Long Term Stability* | TJ = 125°C, 1000 Hrs. | | 20 | 50 | | 20 | 50 | mV |

* These parameters are guaranteed by design but not 100% tested in production.

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ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ for the UC1524A, -25° to $+85^{\circ}\text{C}$ for the UC2524A, and 0°C to $+70^{\circ}\text{C}$ for the UC3524A; $V_{IN} = V_C = 20\text{V}$, $T_A = T_J$.

| PARAMETER | TEST CONDITIONS | UC1524A / UC2524A | | | UC3524A | | | UNITS |
|---|---|-------------------|------|------|---------|------|------|------------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Oscillator Section (Unless otherwise specified, $R_T = 2700\Omega$, $C_T = 0.01\text{ mfd}$) | | | | | | | | |
| Initial Accuracy | $T_J = 25^{\circ}\text{C}$ | 41 | 43 | 45 | 39 | 43 | 47 | kHz |
| | Over Operating Range | 40.2 | | 45.9 | 38.2 | | 47.9 | kHz |
| Temperature Stability* | Over Operating Temperature Range | | 1 | 2 | | 1 | 2 | % |
| Minimum Frequency | $R_T = 150\text{k}\Omega$, $C_T = 0.1\text{ mfd}$ | | | 140 | | | 120 | Hz |
| Maximum Frequency | $R_T = 2.0\text{k}\Omega$, $C_T = 470\text{pF}$ | 500 | | | 500 | | | kHz |
| Output Amplitude* | | 3 | 3.5 | | 3 | 3.5 | | V |
| Output Pulse Width* | | 0.29 | 0.5 | 1.0 | 0.3 | 0.5 | 1.0 | μs |
| Ramp Peak | | 3.3 | 3.5 | 3.7 | 3.3 | 3.5 | 3.7 | V |
| Ramp Valley | $T_J = 25^{\circ}\text{C}$ | 0.7 | 0.8 | 0.9 | 0.7 | 0.8 | 0.9 | V |
| Ramp Valley T.C. | | | -1.0 | | | -1.0 | | $\text{mV}/^{\circ}\text{C}$ |
| Error Amplifier Section (Unless otherwise specified, $V_{CM} = 2.5\text{V}$) | | | | | | | | |
| Input Offset Voltage | | | 0.5 | 5 | | 2 | 10 | mV |
| Input Bias Current | | | 1 | 5 | | 1 | 10 | μA |
| Input Offset Current | | | .05 | 1 | | 0.5 | 1 | μA |
| Common Mode Rejection Ratio | $V_{CM} = 1.5$ to 5.5V | 70 | 80 | | 70 | 80 | | dB |
| Power Supply Rejection Ratio | $V_{IN} = 10$ to 40V | 70 | 80 | | 70 | 80 | | dB |
| Output Swing (Note 1) | | 5.0 | | 0.5 | 5.0 | | 0.5 | V |
| Open Loop Voltage Gain | $\Delta V_O = 1$ to 4V , $R_L \geq 10\text{M}\Omega$ | 72 | 80 | | 64 | 80 | | dB |
| Gain-Bandwidth* | $T_J = 25^{\circ}\text{C}$, $A_V = 0\text{dB}$ | 1 | 3 | | 1 | 3 | | MHz |
| DC Transconductance*§ | $T_J = 25^{\circ}\text{C}$, $30\text{k}\Omega \leq R_L \leq 1\text{M}\Omega$ | 1.7 | 2.3 | | 1.7 | 2.3 | | mS |
| P.W.M. Comparator ($R_T = 2\text{k}\Omega$, $C_T = 0.01\text{ mfd}$) | | | | | | | | |
| Minimum Duty Cycle | $V_{COMP} = 0.5\text{V}$ | | | 0 | | | 0 | % |
| Maximum Duty Cycle | $V_{COMP} = 3.8\text{V}$ | 45 | | | 45 | | | % |
| Current Limit Amplifier (Unless otherwise specified, $\text{Pin } 5 = 0\text{V}$) | | | | | | | | |
| Input Offset Voltage | $T_J = 25^{\circ}\text{C}$, E/A Set for Maximum Output | 190 | 200 | 210 | 180 | 200 | 220 | mV |
| | Over Operating Temperature Range | 180 | | 220 | 170 | | 230 | mV |
| Input Bias Current | | | -1 | -10 | | -1 | -10 | μA |
| Common Mode Rejection Ratio | $V_{(\text{pin } 5)} = -0.3\text{V}$ to $+5.5\text{V}$ | 50 | 60 | | 50 | 60 | | dB |
| Power Supply Rejection Ratio | $V_{IN} = 10$ to 40V | 50 | 60 | | 50 | 60 | | dB |
| Output Swing (Note 1) | Minimum Total Range | 5.0 | | 0.5 | 5.0 | | 0.5 | V |
| Open-Loop Voltage Gain | $\Delta V_O = 1$ to 4V , $R_L \geq 10\text{M}\Omega$ | 70 | 80 | | 70 | 80 | | dB |
| Delay Time* | Pin 4 to Pin 9, $\Delta V_{IN} = 300\text{mV}$ | | 300 | | | 300 | | ns |
| Output Section (Each Output) | | | | | | | | |
| Collector Emitter Voltage | $I_C = 100\mu\text{A}$ | 60 | 80 | | 60 | 80 | | V |
| Collector Leakage Current | $V_{CE} = 50\text{V}$ | | .1 | 20 | | .1 | 20 | μA |

* These parameters are guaranteed by design but not 100% tested in production.

§ DC transconductance (gm) relates to DC open-loop voltage gain according to the following equation: $A_V = gmR_L$ where R_L is the resistance from pin 9 to the common mode voltage.

The minimum gm specification is used to calculate minimum A_V when the error amplifier output is loaded.

Note 1: Min Limit applies to output high level, max limit applies to output low level.

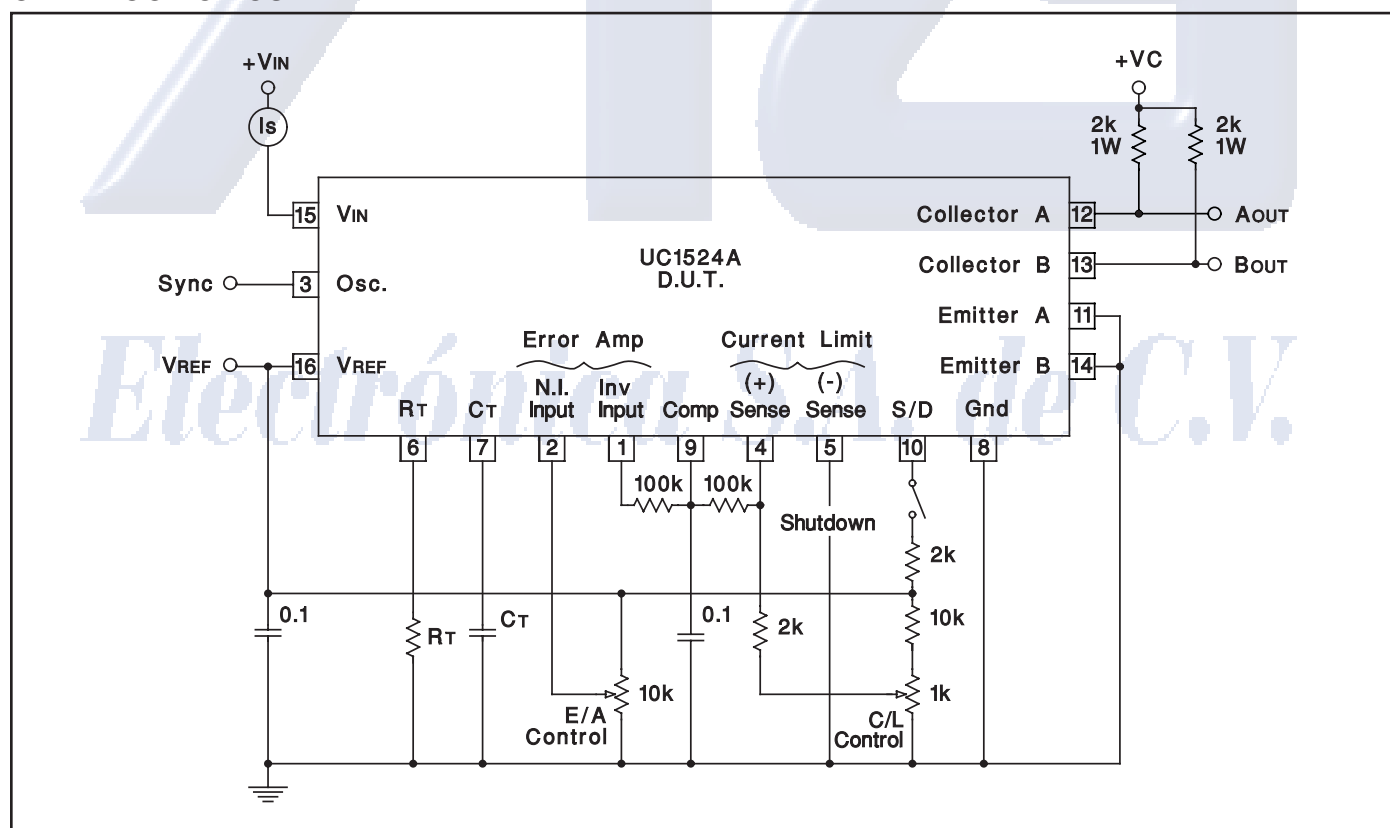
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ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1524A, -25° to $+85^\circ\text{C}$ for the UC2524A, and 0°C to $+70^\circ\text{C}$ for the UC3524A; $V_{IN} = V_C = 20\text{V}$. $T_A = T_J$.

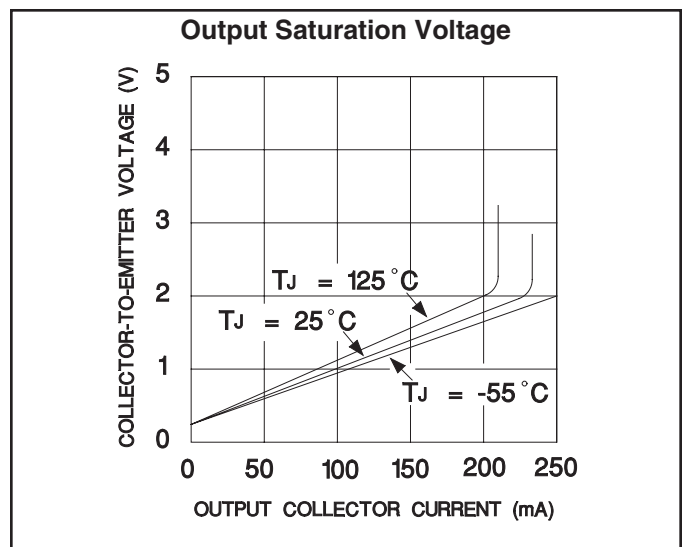
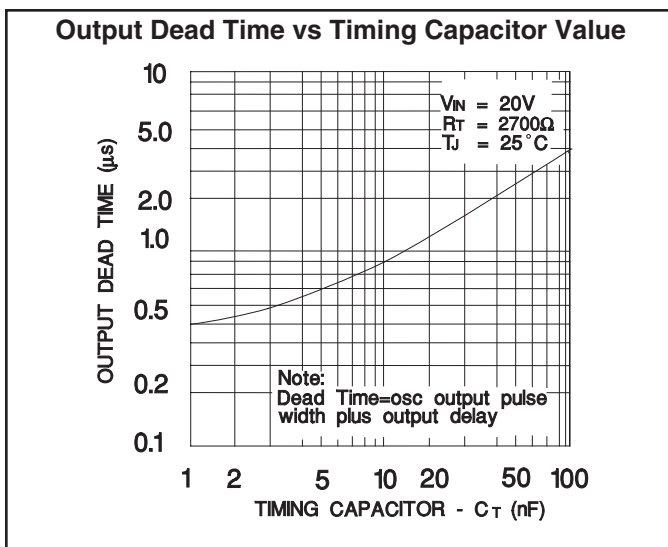
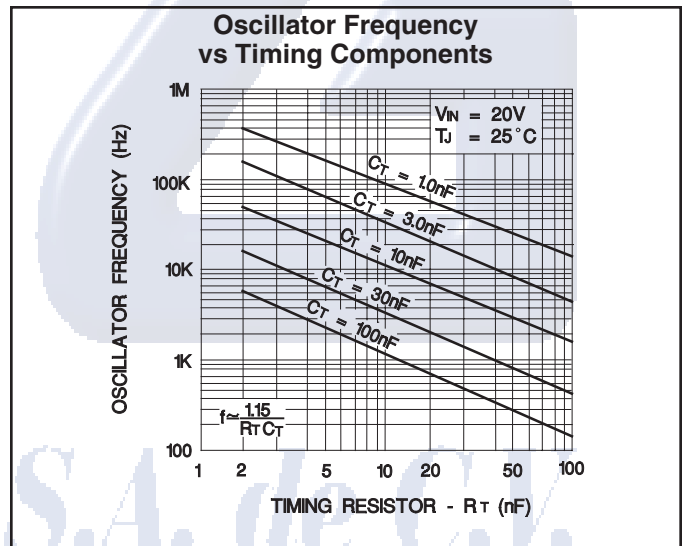
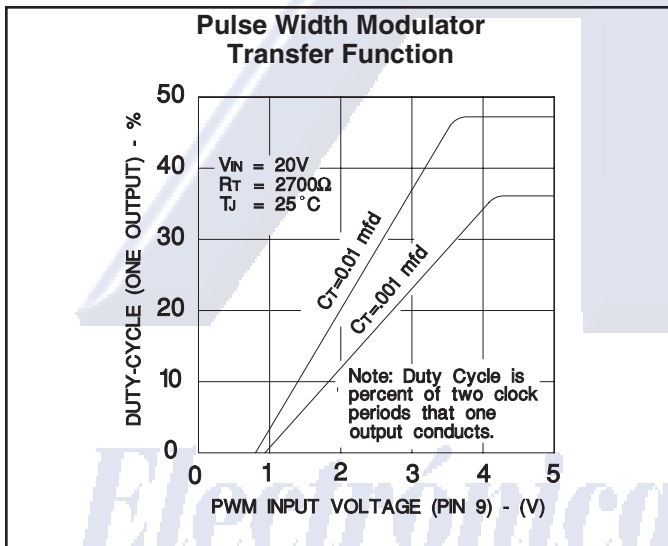
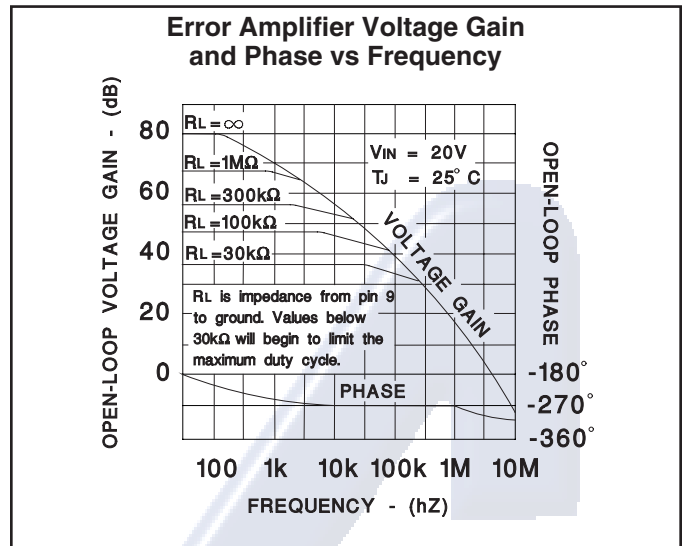
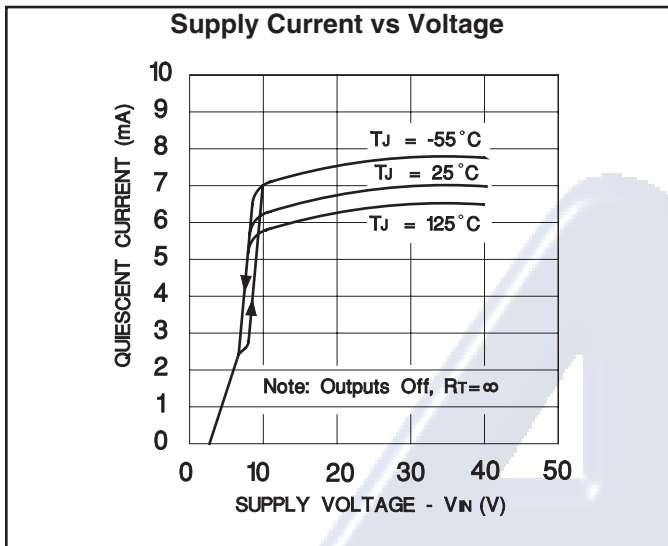
| PARAMETER | TEST CONDITIONS | UC1524A / UC2524A | | | UC3524A | | | UNITS |
|--|--|-------------------|---------|-----------|---------|---------|-----------|------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Output Section (cont.) (Each Output) | | | | | | | | |
| Saturation Voltage | $I_C = 20\text{mA}$ $I_C = 200\text{mA}$ | | .2 1 | .4 2.2 | | .2 1 | .4 2.2 | V V |
| Emitter Output Voltage | $I_E = 50\text{mA}$ | 17 | 18 | | 17 | 18 | | V |
| Rise Time* | $T_J = 25^\circ\text{C}$, $R = 2\text{k}\Omega$ | | 120 | 400 | | 120 | 400 | ns |
| Fall Time* | $T_J = 25^\circ\text{C}$, $R = 2\text{k}\Omega$ | | 25 | 200 | | 25 | 200 | ns |
| Comparator Delay* | $T_J = 25^\circ\text{C}$, Pin 9 to output | | 300 | | | 300 | | ns |
| Shutdown Delay* | $T_J = 25^\circ\text{C}$, Pin 10 to output | | 200 | | | 200 | | ns |
| Shutdown Threshold | $T_J = 25^\circ\text{C}$, $R_C = 2\text{k}\Omega$ | 0.6 | .7 | 1.0 | 0.6 | .7 | 1.0 | V |
| S/D Threshold Over Temp. | Over Operating Temperature Range | 0.4 | | 1.2 | 0.4 | | 1.0 | V |
| Thermal Shutdown* | | | 165 | | | 165 | | $^\circ\text{C}$ |

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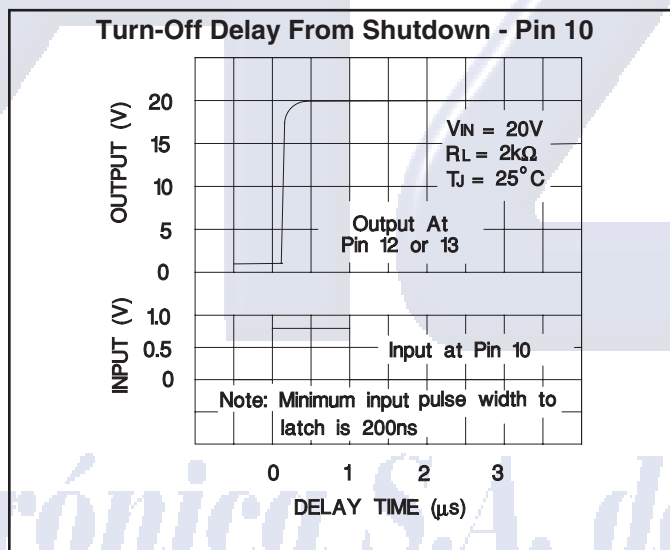
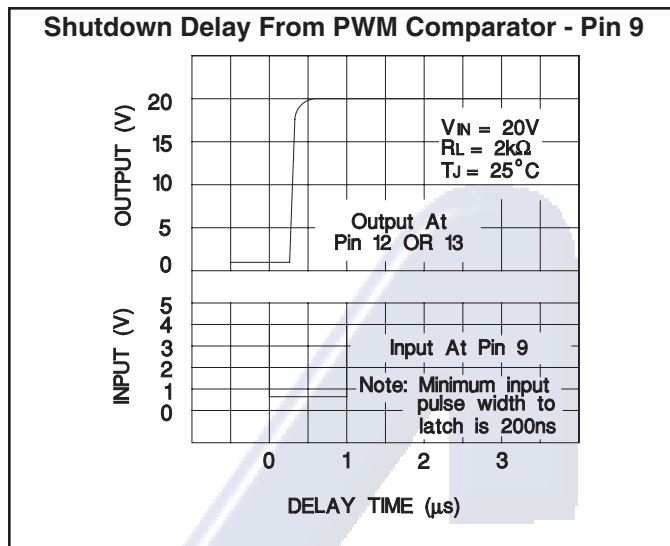
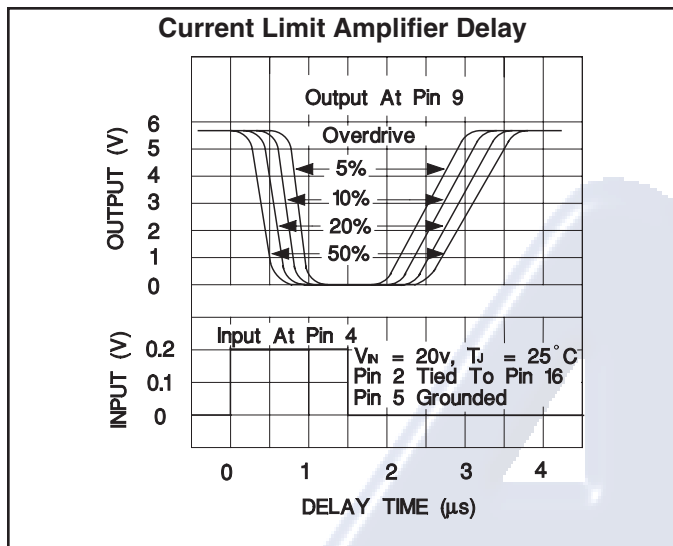
OPEN-LOOP CIRCUIT



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