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DATA SHEET

NEC

COMPOUND FIELD EFFECT POWER TRANSISTOR
μPA1556A

N-CHANNEL POWER MOS FET ARRAY
SWITCHING TYPE

DESCRIPTION

The μPA1556A is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance
  $I_{D(pulse)}$ = ±20 A
  $R_{DS(on)}$ = 0.20 Ω TYP. (V_{GS} = 10 V)
  $R_{DS(on)}$ = 0.25 Ω TYP. (V_{GS} = 4 V)
- Low Capacitance C_{iss} = 700 pF TYP.
- Gate Protecter built in.
- 2.54 mm Pitch (0.1 inch)

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPA1556AH	10 Pin SIP	Standard

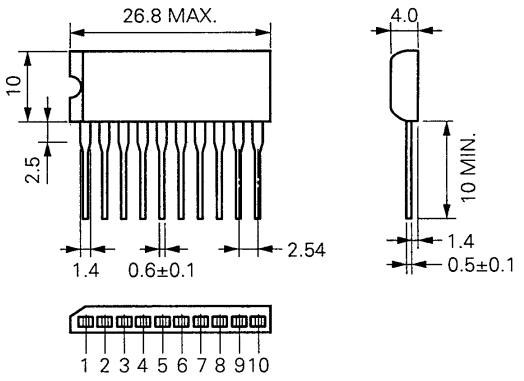
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

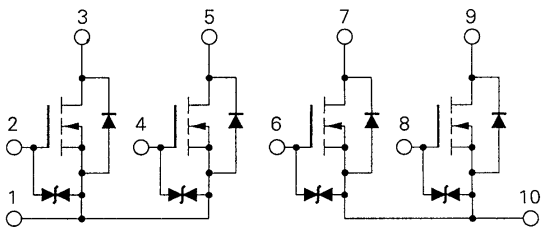
Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage (AC)	V_{GSS}	±20	V
Gate to Source Voltage (DC)	V_{GSS}	+20,–10	V
Drain Current (DC)	$I_{D(DC)}$	±5.0	A/unit
Drain Current (pulse)	$I_{D(pulse)}$*	±20	A/unit
Total Power Dissipation (4 circuits)			
<T_c = 25 °C>	P_{T1}	28	W
Total Power Dissipation (4 circuits)			
<T_a = 25 °C>	P_{T2}	3.5	W
Storage Temperature	T_{stg}	–55 to +150	°C
Junction Temperature	T_j	150	°C

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

PACKAGE DIMENSION
(in millimeters)

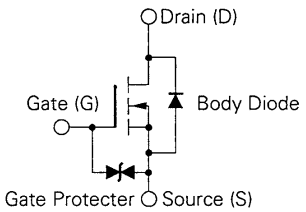


CONNECTION DIAGRAM



PIN No.

2, 4, 6, 8	Gate (G)
3, 5, 7, 9	Drain (D)
1, 10	Source (S)



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ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	I_{DSS}			10	μA	V_{DS} = 100 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±20 V, V_{DS} = 0
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	4.0			S	V_{DS} = 10 V, I_D = 3 A
Drain to Source On-state Resistance	$R_{DS(on)1}$		0.20	0.25	Ω	V_{GS} = 10 V, I_D = 3 A
Drain to Source On-state Resistance	$R_{DS(on)2}$		0.25	0.33	Ω	V_{GS} = 4 V, I_D = 3 A
Input Capacitance	C_{iss}		700		pF	V_{DS} = 10 V V_{GS} = 0 f = 1.0 MHz
Output Capacitance	C_{oss}		200		pF	
Reverse Transfer Capacitance	C_{rss}		30		pF	
Turn-On Delay Time	$t_{d(on)}$		35		ns	I_D = 3 A V_{GS} = 10 V V_{CC} = 50 V R_L = 17 Ω, R_{in} = 10 Ω See Fig. 1
Rise Time	t_r		60		ns	
Turn-Off Delay Time	$t_{d(off)}$		800		ns	
Fall Time	t_f		200		ns	
Total Gate Charge	Q_G		17		nC	V_{GS} = 10 V I_D = 5 A V_{DD} = 80 V See Fig. 2
Gate to Source Charge	Q_{GS}		2.5		nC	
Gate to Drain Charge	Q_{GD}		4		nC	
Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	I_F = 5 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		120		ns	I_F = 5 A, V_{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		230		nC	

Fig. 1 Switching Time Test Circuit

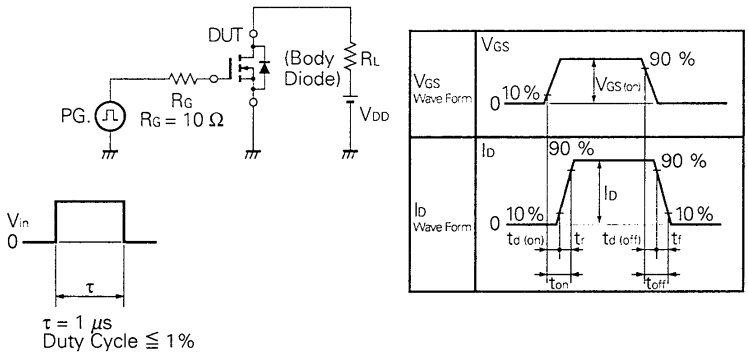
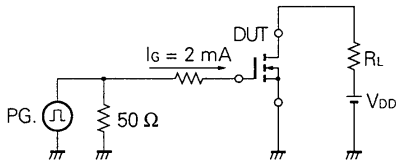
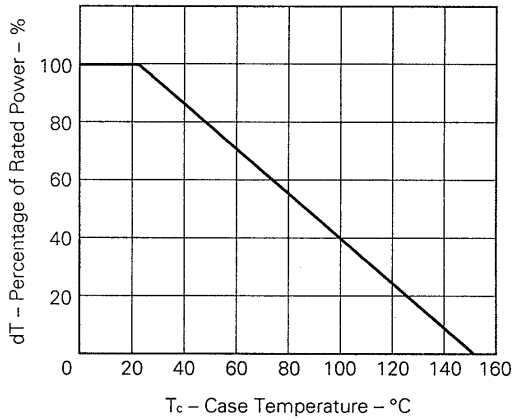


Fig. 2 Gate Charge Test Circuit

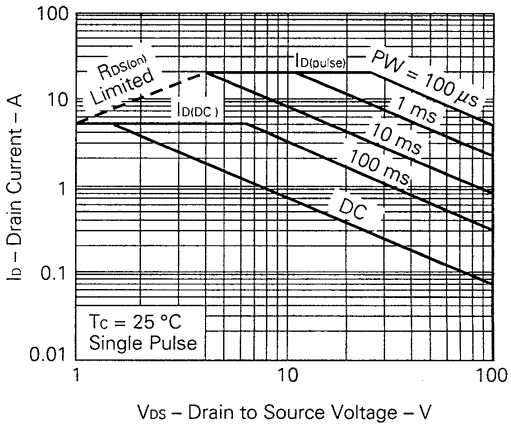


TYPICAL CHARACTERISTICS (T_a = 25 °C)

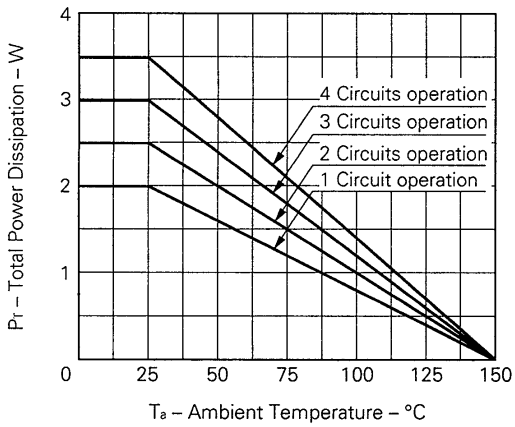
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



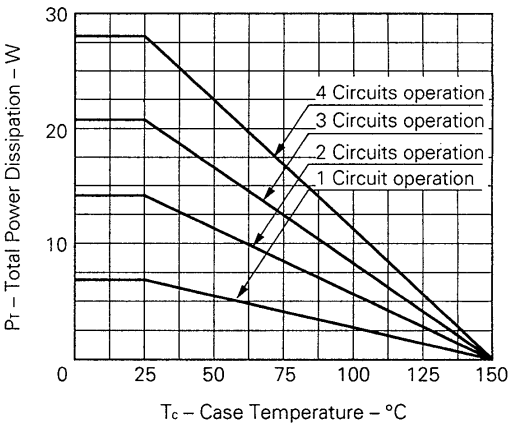
FORWARD BIAS SAFE OPERATING AREA



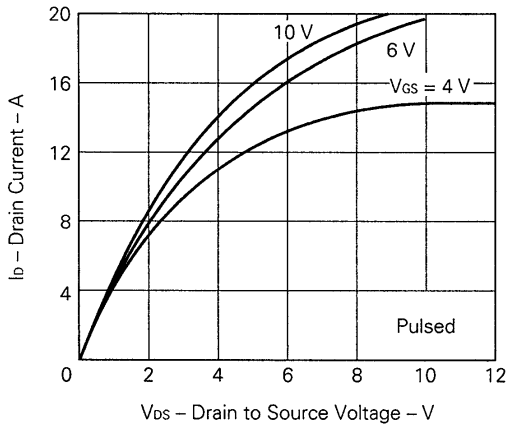
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



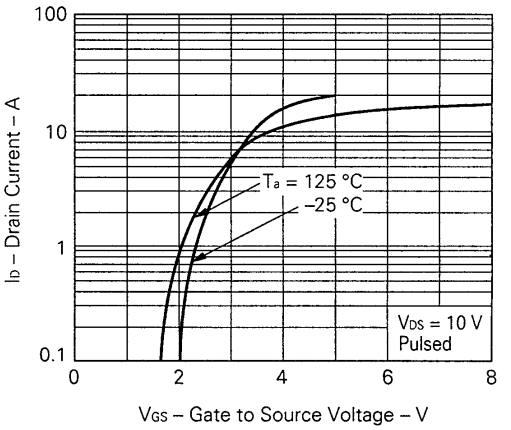
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



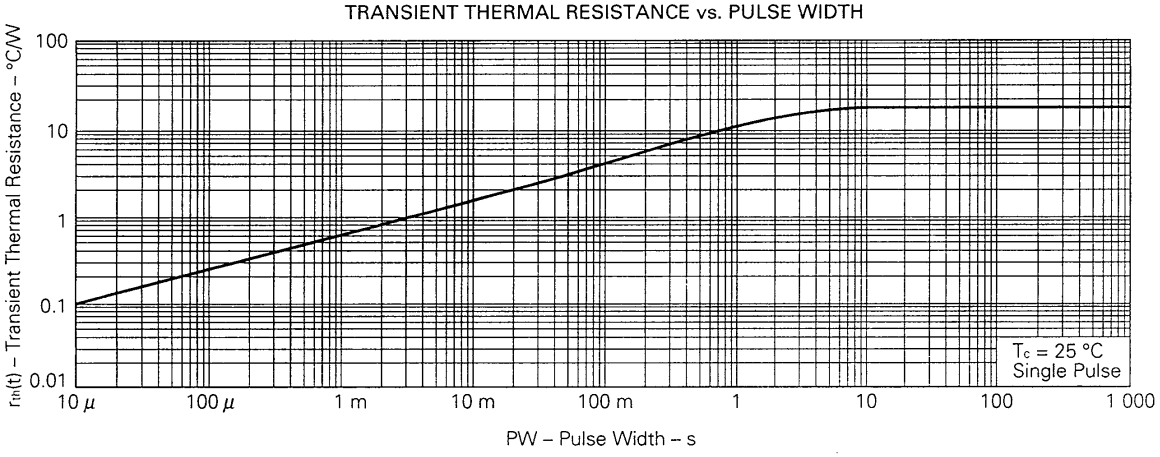
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



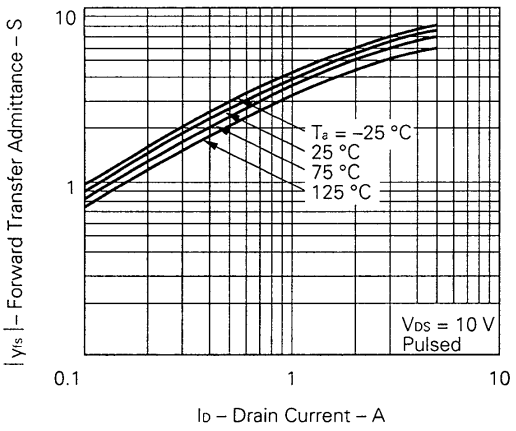
TRANSFER CHARACTERISTICS



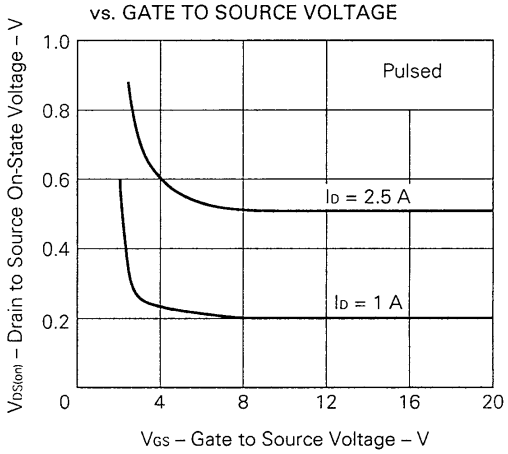
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



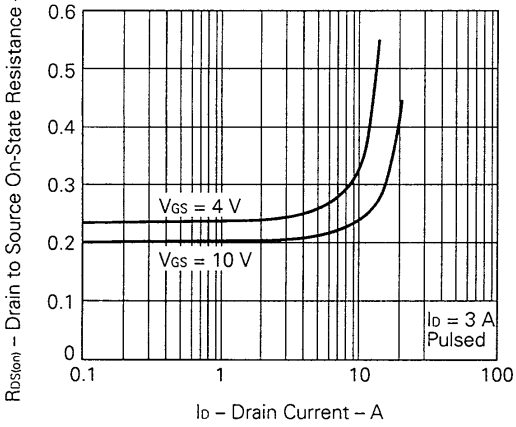
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



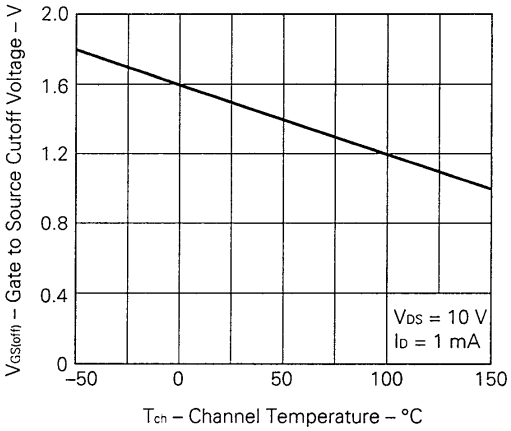
DRAIN TO SOURCE ON-STATE VOLTAGE vs. GATE TO SOURCE VOLTAGE

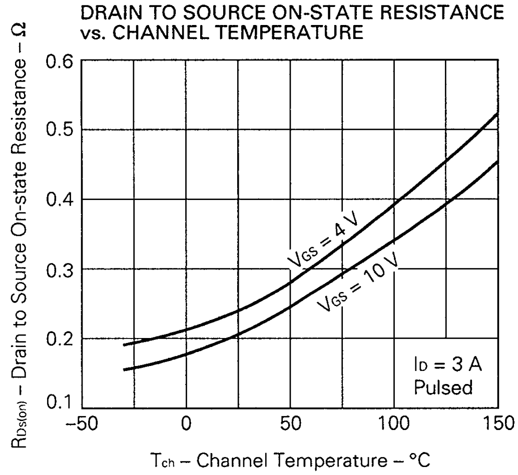


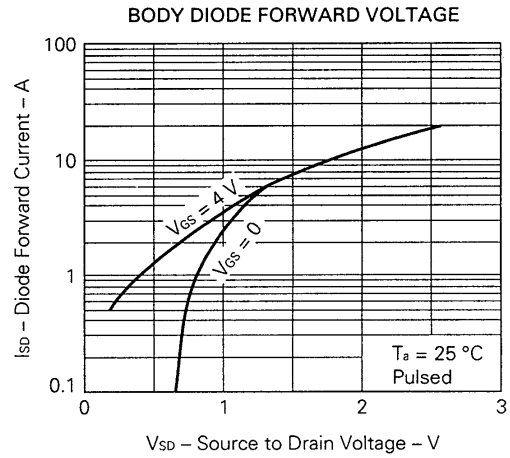
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

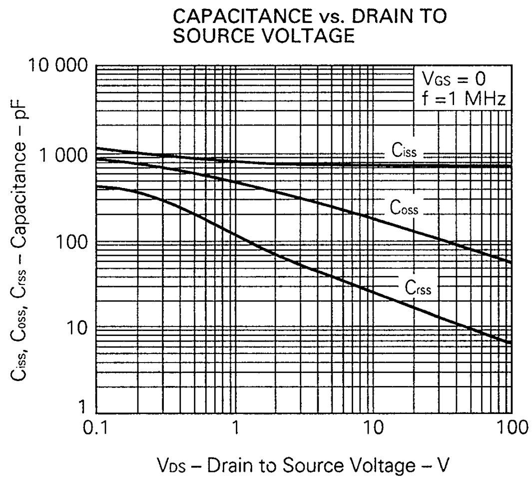


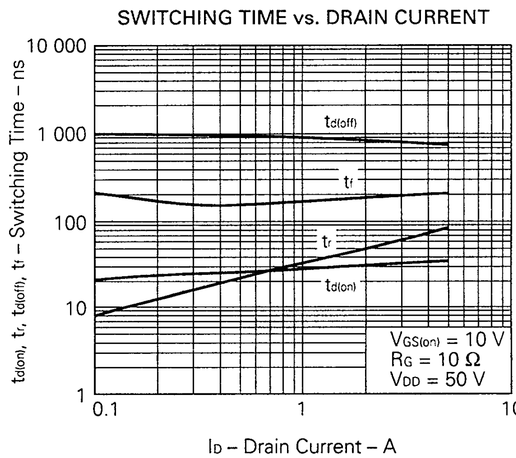
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

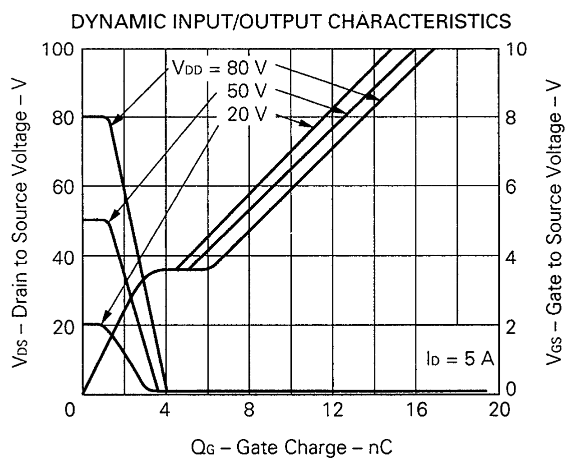


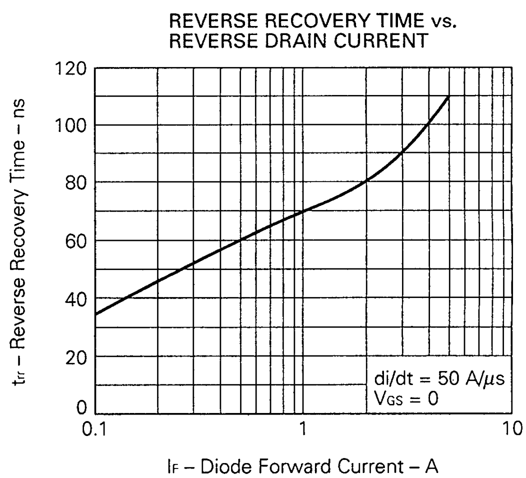












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Reference

Document name	Document No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Appication circuit using Power MOS FET	TEA-1035

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