

DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT
 μ PC4570

DUAL ULTRA LOW-NOISE, WIDEBAND, OPERATIONAL AMPLIFIER

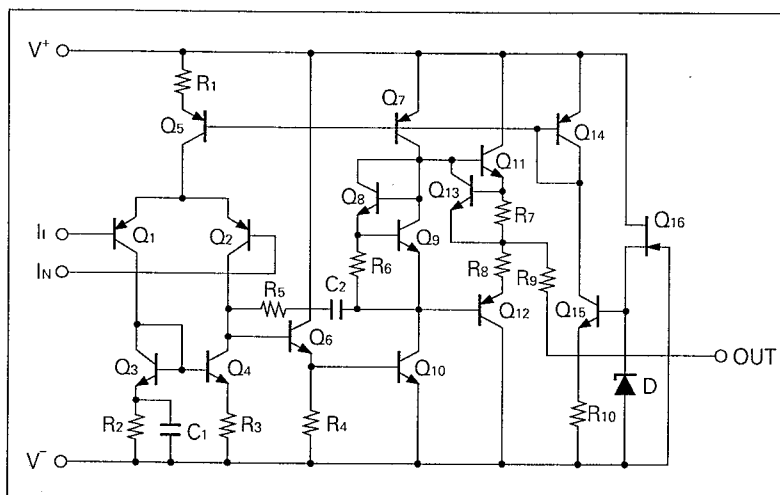
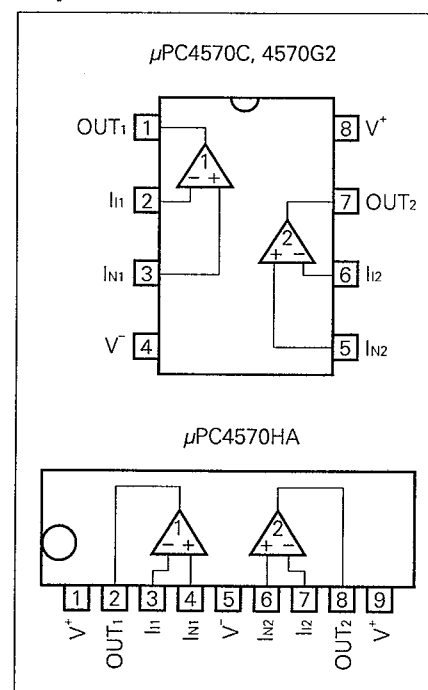
DESCRIPTION

The μ PC4570 is an ultra low-noise, wideband high slew-rate, dual operational amplifier. Input equivalent noise is three times better than the conventional 4558 type op-amps. The gain bandwidth products and the slew-rate are seven times better than 4558. In spite of fast AC performance, the μ PC4570 is extremely stable under voltage-follower circuit conditions. Supply current is also improved compared with conventional wideband op-amps. The μ PC4570 is an excellent choice for pre-amplifiers and active filters in audio, instrumentation, and communication circuits.

FEATURES

- Ultra low noise : $e_n = 4.5 \text{ nV}/\sqrt{\text{Hz}}$
- High slew rate: $7 \text{ V}/\mu\text{s}$
- High gain bandwidth product:
GBW = 15 MHz at 100 kHz
- Internal frequency compensation

EQUIVALENT CIRCUIT (1/2 Circuit)

CONNECTION DIAGRAM
(Top View)

ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μ PC4570C	8 PIN PLASTIC DIP (300 mil)	Standard
μ PC4570G2	8 PIN PLASTIC SOP (225 mil)	Standard
μ PC4570HA	9 PIN SLIM SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25\text{ }^\circ\text{C}$)

PARAMETER		SYMBOL	μ PC4570	UNIT
Voltage between V^+ and V^- (Note 1)		$V^+ - V^-$	-0.3 to +36	V
Differential Input Voltage		V_{ID}	± 30	V
Input Voltage (Note 2)		V_I	$V^- - 0.3$ to $V^+ + 0.3$	V
Output Voltage (Note 3)		V_O	$V^- - 0.3$ to $V^+ + 0.3$	V
Power Dissipation	C Package (Note 4)	P_T	350	mW
	G2 Package (Note 5)		440	mW
	HA Package (Note 4)		350	mW
Output Short Circuit Duration (Note 6)			10	sec
Operating Temperature Range		T_{opt}	-20 to +80	$^\circ\text{C}$
Storage Temperature Range		T_{stg}	-55 to +125	$^\circ\text{C}$

Note 1. Reverse connection of supply voltage can cause destruction.

Note 2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

Note 3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.

Note 4. Thermal derating factor is $-5.0\text{ mW} / ^\circ\text{C}$ when ambient temperature is higher than $55\text{ }^\circ\text{C}$.

Note 5. Thermal derating factor is $-4.4\text{ mW} / ^\circ\text{C}$ when ambient temperature is higher than $25\text{ }^\circ\text{C}$.

Note 6. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^{\pm}	± 4		± 16	V
Output Current	I_o			± 10	mA
Source Resistance	R_s			50	$k\Omega$
Capacitive Load ($A_v = +1$)	C_L			100	pF

ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^\circ\text{C}$, $V^\pm = \pm 15\text{ V}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Offset Voltage	V_{io}		± 0.3	± 5	mV	$R_s \leq 50\ \Omega$
* Input Offset Current (Note7)	I_{io}		± 10	± 100	nA	
* Input Bias Current (Note7)	I_B		100	400	nA	
Large Signal Voltage Gain	A_v	30	300		V/mV	$R_L \geq 2\ \text{k}\Omega$, $V_o = \pm 10\ \text{V}$
Supply Current	I_{cc}		5	8	mA	$I_o = 0\ \text{A}$, Both Amplifiers
Common Mode Rejection Ratio	CMR	80	100		dB	
Supply Voltage Rejection Ratio	SVR	80	100		dB	
Output Voltage Swing	V_{om}	± 12	± 13.4		V	$R_L \geq 10\ \text{k}\Omega$
Output Voltage Swing	V_{om}	± 10	± 12.8		V	$R_L \geq 2\ \text{k}\Omega$
Common Mode Input Voltage Range	V_{icm}	± 12	± 14		V	
Slew Rate	SR	5	7		V/ μ s	$R_L \geq 2\ \text{k}\Omega$
Gain Bandwidth Product	GBW	10	15		MHz	$f_o = \text{kHz}$
Unity Gain Frequency	f_{unity}		7		MHz	open loop
Phase Margin	ϕ_{unity}		50		degree	open loop
Total Harmonic Distortion	THD		0.002		%	$V_o = 3\ V_{r.m.s.}$, $f = 20\ \text{Hz}$ to $20\ \text{kHz}$ (Fig. 1)
* Input Equivalent Noise Voltage	V_n		0.9		$\mu V_{r.m.s.}$	RIAA (Fig. 2)
Input Equivalent Noise Voltage	V_n		0.53	0.65	$\mu V_{r.m.s.}$	FLAT + JIS A, $R_s = 100\ \Omega$ (Fig. 3)
Input Equivalent Noise Voltage Density	e_n		5.5		$\text{nV}/\sqrt{\text{Hz}}$	$f_o = 10\ \text{Hz}$, $R_s = 100\ \Omega$
Input Equivalent Noise Voltage Density	e_n		4.5		$\text{nV}/\sqrt{\text{Hz}}$	$f_o = 1\ \text{kHz}$, $R_s = 100\ \Omega$
Input Equivalent Noise Voltage Density	i_n		0.7		$\text{pA}/\sqrt{\text{Hz}}$	$f_o = 1\ \text{kHz}$
Channel Separation			120		dB	$f = 20\ \text{Hz}$ to $20\ \text{kHz}$

Note 7. Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

Note 8. For asterisk items, those spec was applied to the production lots mode after Jun. '87 by the effect of input PNP Tr's h_{fe} rise. Before spec is following.

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Offset Current (Note7)	I_{io}		± 10	± 200	nA	
Input Bias Current (Note7)	I_B		500	1000	nA	
Input Equivalent Noise Voltage	V_n		1.2		$\mu V_{r.m.s.}$	RIAA (Fig. 2)

MEASUREMENT CIRCUIT

Fig. 1 Total Harmonic Distortion Measurement Circuit

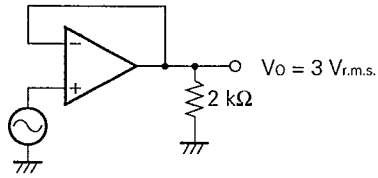


Fig. 2 Noise Measurement Circuit (RIAA)

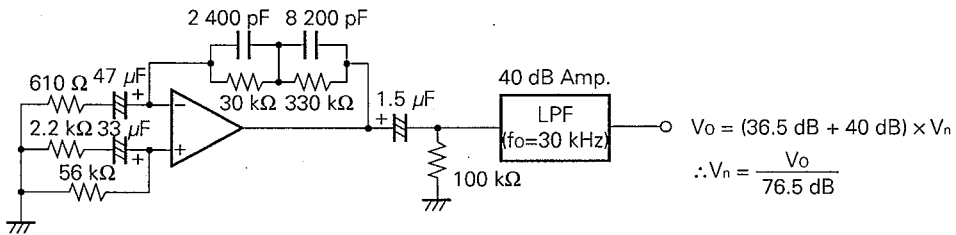
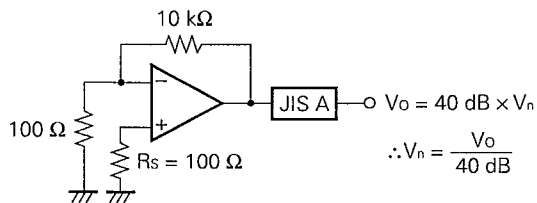
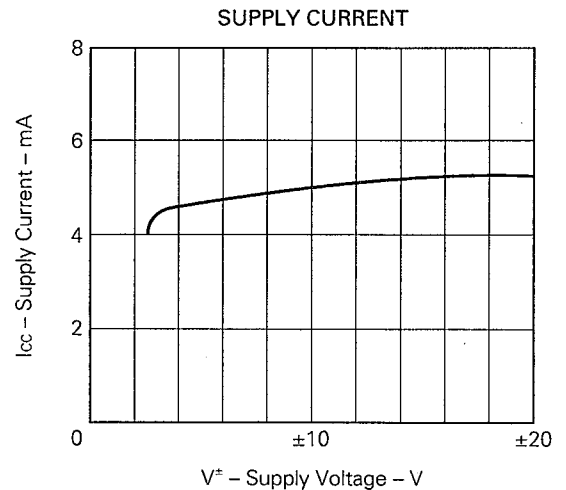
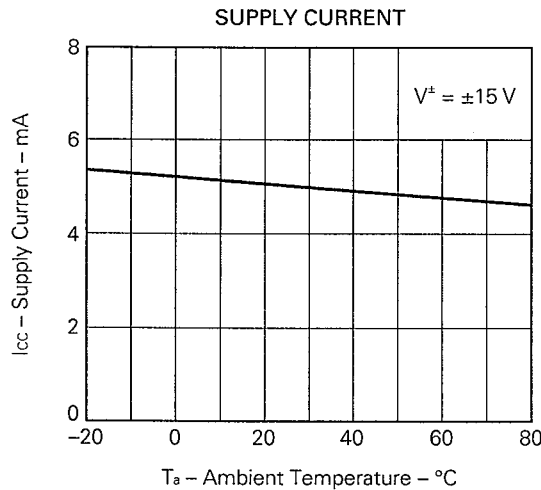
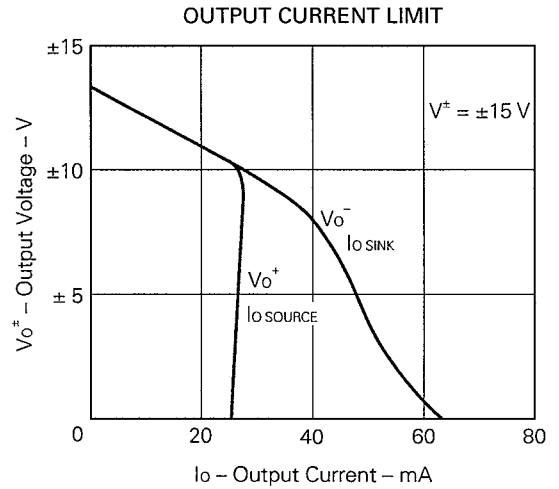
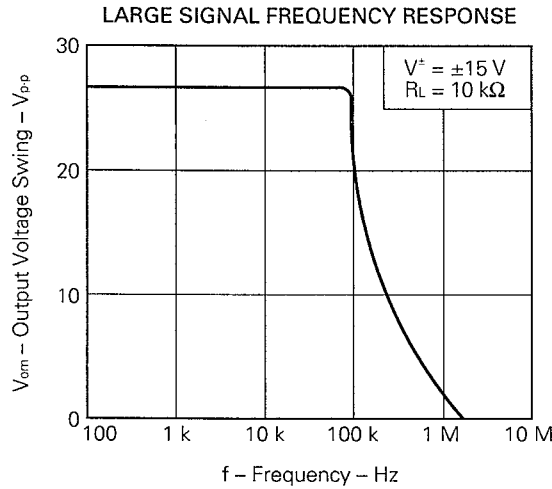
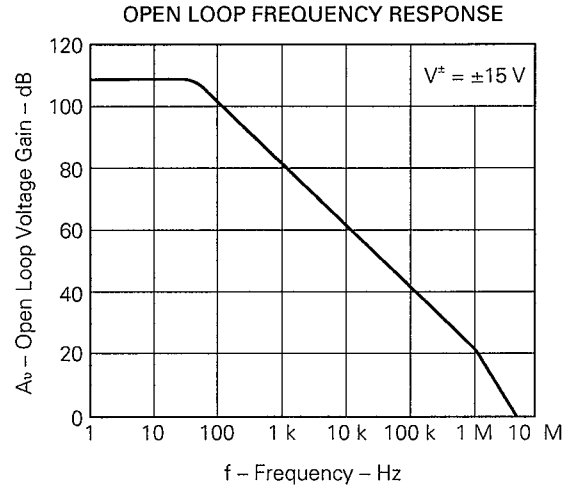
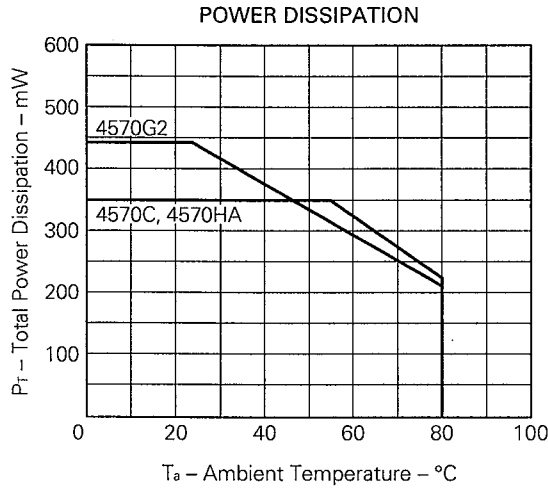
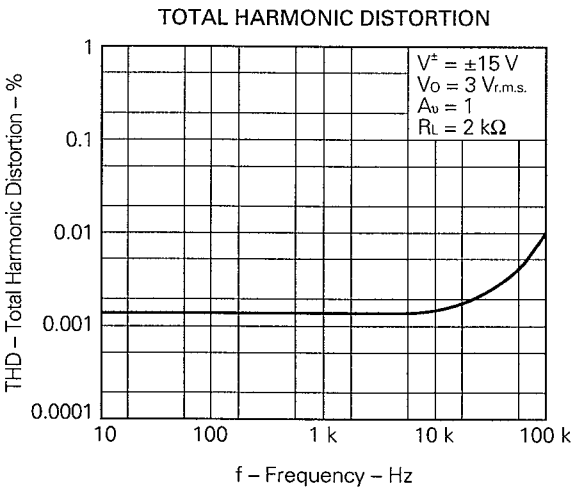
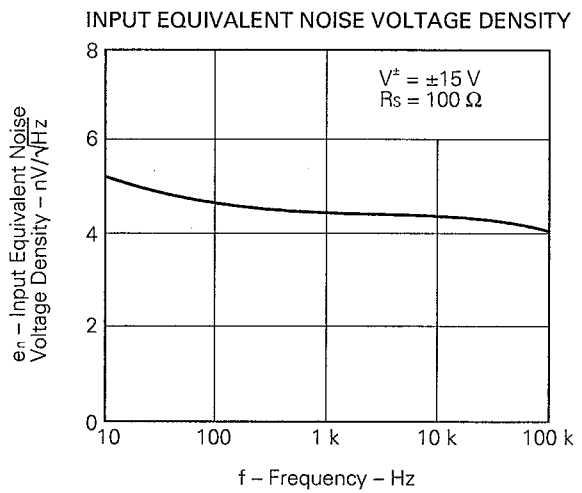
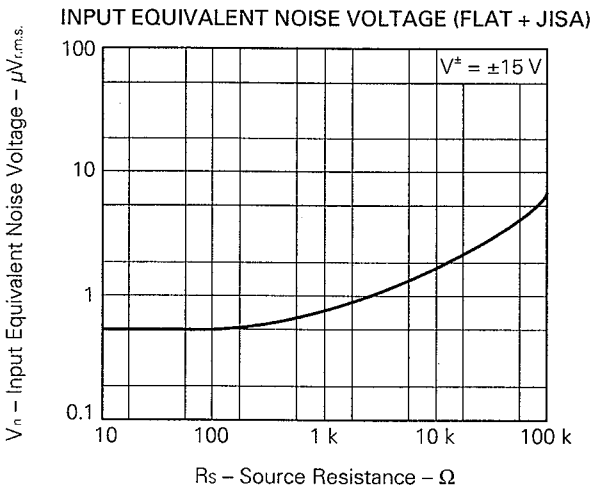
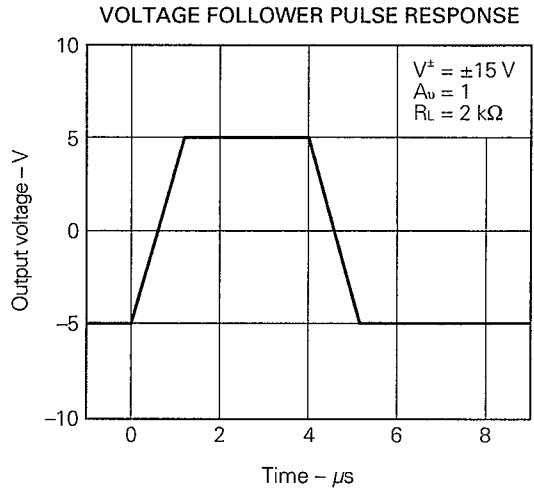
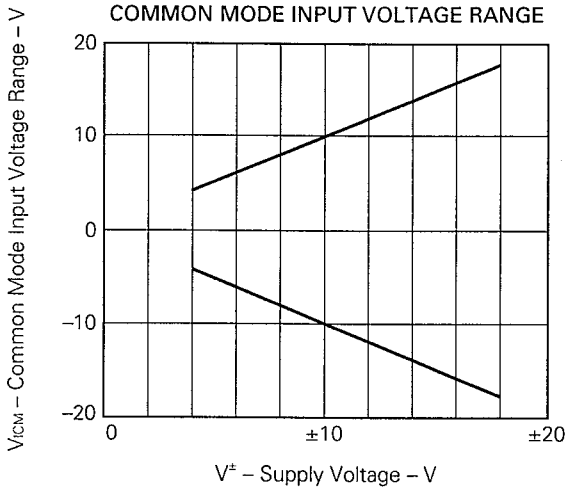


Fig. 3 Noise Measurement Circuit (FLAT + JIS A)

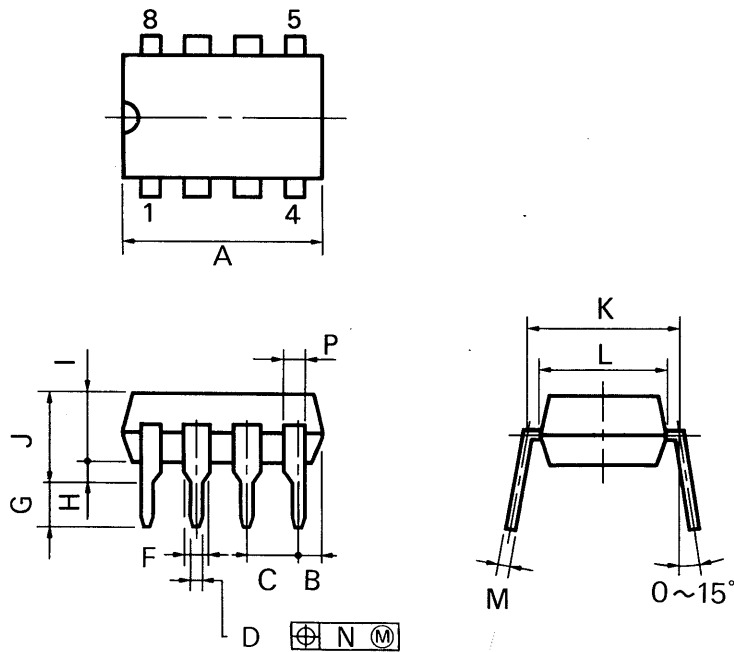


TYPICAL PERFORMANCE CHARACTERISTICS (T_a = 25 °C, TYP.)





8PIN PLASTIC DIP (300 mil)



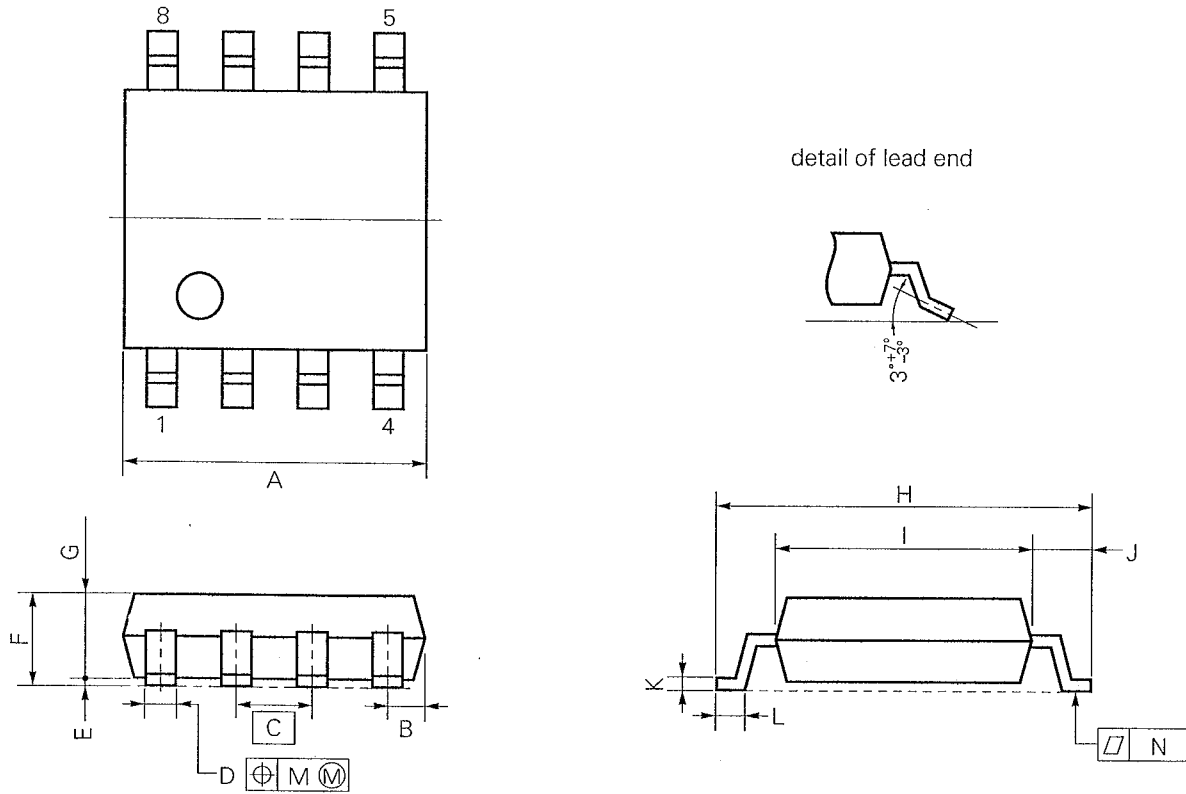
P8C-100-300B,C

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ^{±0.10}	0.020 ^{+0.004} _{-0.005}
F	1.4 MIN.	0.055 MIN.
G	3.2 ^{±0.3}	0.126 ^{±0.012}
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.005}
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

8 PIN PLASTIC SOP (225 mil)



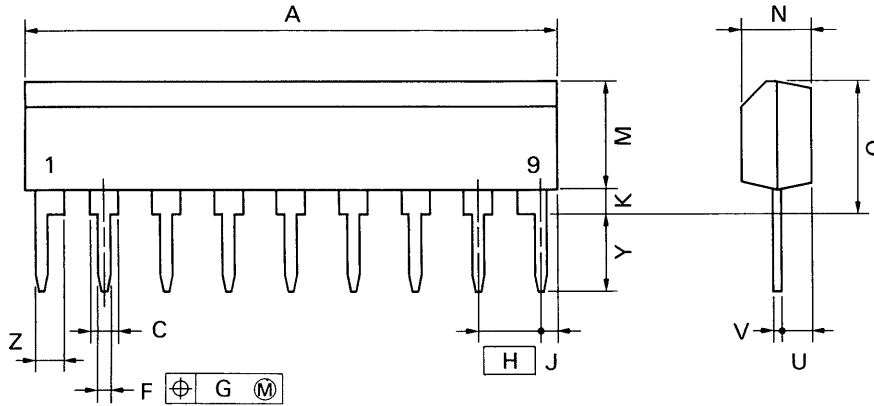
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S8GM-50-225B-2

ITEM	MILLIMETERS	INCHES
A	5.37 MAX.	0.212 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10} _{-0.05}	0.016 ^{+0.004} _{-0.003}
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.49	0.059
H	6.5±0.3	0.256±0.012
I	4.4	0.173
J	1.1	0.043
K	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.002}
L	0.6±0.2	0.024 ^{+0.008} _{-0.009}
M	0.12	0.005
N	0.15	0.006

9 PIN PLASTIC SLIM SIP



NOTE

Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

P9HA-254B

ITEM	MILLIMETERS	INCHES
A	22.86 MAX.	0.9 MAX.
C	1.1 MIN.	0.043 MIN.
F	0.5 ^{±0.1}	0.02 ^{±0.008}
G	0.25	0.01
H	2.54	0.1
J	1.27 MAX.	0.05 MAX.
K	0.51 MIN.	0.02 MIN.
M	5.08 MAX.	0.2 MAX.
N	2.8 ^{±0.2}	0.11 ^{±0.008}
Q	5.75 MAX.	0.227 MAX.
U	1.5 MAX.	0.059 MAX.
V	0.25 ^{±0.08}	0.01 ^{±0.003}
Y	3.2 ^{±0.5}	0.126 ^{±0.02}
Z	1.1 MIN.	0.043 MIN.

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

[μ PC4570G2]

Soldering method	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: None	IR30-00-1
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: None	VP15-00-1
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below Number of flow process: 1, Exposure limit*: None	WS15-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

*: Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Do not apply more than a single process at once, except for "Partial heating method."

TYPES OF THROUGH HOLE DEVICE

[μ PC4570C, μ PC4570HA]

Soldering method	Soldering conditions	Recommended condition symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	

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Application examples recommended by NEC Corporation.

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

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