

4096 BIT (1024 × 4 BITS) STATIC RAM

DESCRIPTION The NEC μPD2114L is a 4096 bit static Random Access Memory organized as 1024 words by 4 bits using N-channel Silicon-gate MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding. It therefore requires no clocks or refreshing to operate and simplifies system design. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

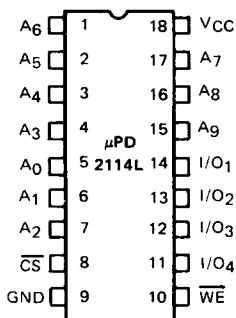
The μPD2114L is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The μPD2114L is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-Tied.

FEATURES

- Access Time: Selection from 150-450 ns
- Single +5 Volt Supply
- Directly TTL Compatible — All Inputs and Outputs
- Completely Static — No Clock or Timing Strobe Required
- Low Operating Power — Typically 0.06 mW/Bit
- Identical Cycle and Access Times
- Common Data Input and Output using Three-State Output
- High Density 18-pin Plastic and Ceramic Packages
- Replacement for 2114L and Equivalent Devices

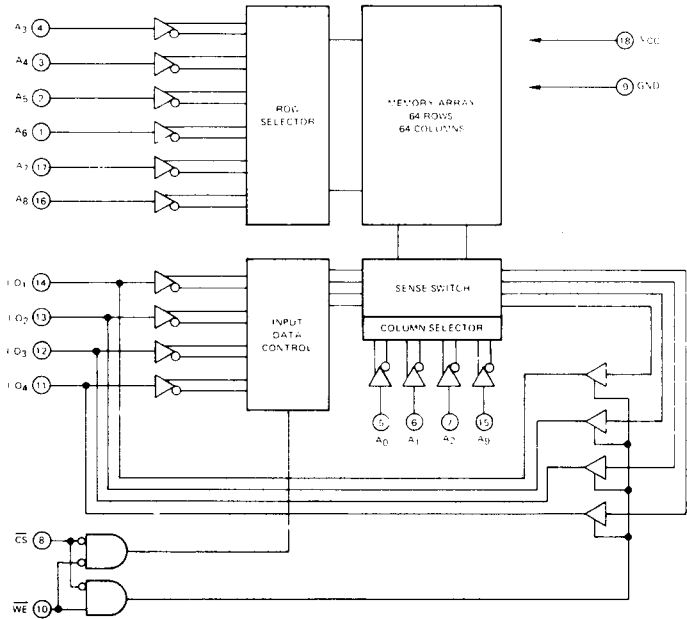
PIN CONFIGURATION



PIN NAMES

A ₀ -A ₉	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O ₁ -I/O ₄	Data Input/Output
VCC	Power (+5V)
GND	Ground

Rev/2



Operating Temperature -10°C to +80°C
Storage Temperature -65°C to +150°C
Voltage on any Pin -0.5 to 7 Volts ①

ABSOLUTE MAXIMUM RATINGS*

Note: ① With respect to ground.
T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T_a = 0°C to 70°C; V_{CC} = +5V ± 10% unless otherwise noted.

DC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Load Current (All Input Pins)	I _{LI}			10	μA	V _{IN} = 0 to 5.5V
I/O Leakage Current	I _{LO}			10	μA	$\overline{\text{CS}}$ = 2V, V _{I/O} = 0.4V to V _{CC}
Power Supply Current	I _{CC1}			65	mA	V _{IN} = 5.5V, I _{I/O} = 0 mA, T _a = 25°C
Power Supply Current	I _{CC2}			70	mA	V _{IN} = 5.5V, I _{I/O} = 0 mA, T _a = 0°C
Input Low Voltage	V _{IL}	-3.0		0.8	V	
Input High Voltage	V _{IH}	2.0		6.0	V	
Output Low Current	I _{OL}	3.2			mA	V _{OL} = 0.4V
Output High Current	I _{OH}			-1.0	mA	V _{OH} = 2.4V, V _{CC} = 4.75V
						V _{OH} = 2.2V, V _{CC} = 4.5V

T_a = 25°C; f = 1.0 MHz

CAPACITANCE

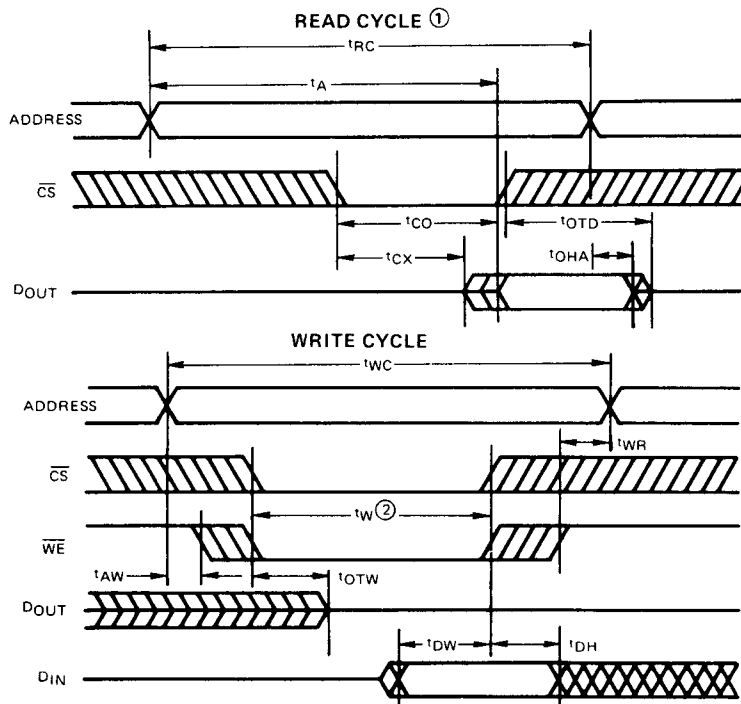
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input/Output Capacitance	C _{I/O}			8	pf	V _{I/O} = 0V
Input Capacitance	C _{IN}			5	pf	V _{IN} = 0V

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		2114L		2114L-1		2114L-2		2114L-3		2114L-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE													
Read Cycle Time	t _{RC}	450		300		250		200		150		ns	t _T = t _r = t _f = 10 ns C _L = 100 pF Load = 1 TTL gate Input Levels = 0.8 and 2.0V V _{ref} = 1.5V
Access Time	t _A		450		300		250		200		150	ns	
Chip Selection to Output Valid	t _{CO}		120		100		80		70		60	ns	
Chip Selection to Output Active	t _{CX}	20		20		20		20		20		ns	
Output 3-State from Deselection	t _{OTD}		100		80		70		60		50	ns	
Output Hold from Address Change	t _{OHA}	50		50		50		50		50		ns	
WRITE CYCLE													
Write Cycle Time	t _{WC}	450		300		250		200		150		ns	t _T = t _r = t _f = 10 ns C _L = 100 pF Load = 1 TTL gate Input Levels = 0.8 and 2.0V V _{ref} = 1.5V
Write Time	t _W	200		150		120		120		80		ns	
Write Release Time	t _{WR}	0		0		0		0		0		ns	
Output 3-State from Write	t _{OTW}		100		80		70		60		50	ns	
Data to Write Time Overlap	t _{DW}	200		150		120		120		80		ns	
Data Hold from Write Time	t _{DH}	0		0		0		0		0		ns	
Address to Write Setup Time	t _{AW}	0		0		0		0		0		ns	

TIMING WAVEFORMS

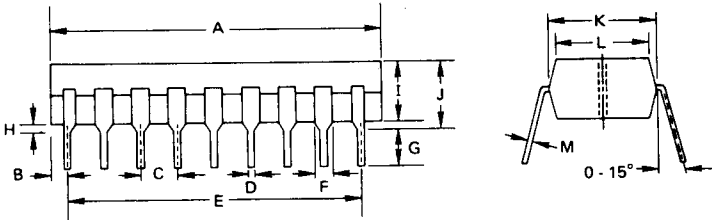


Notes: ① $\overline{WE}$ is high for Read Cycle

② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

μPD2114L

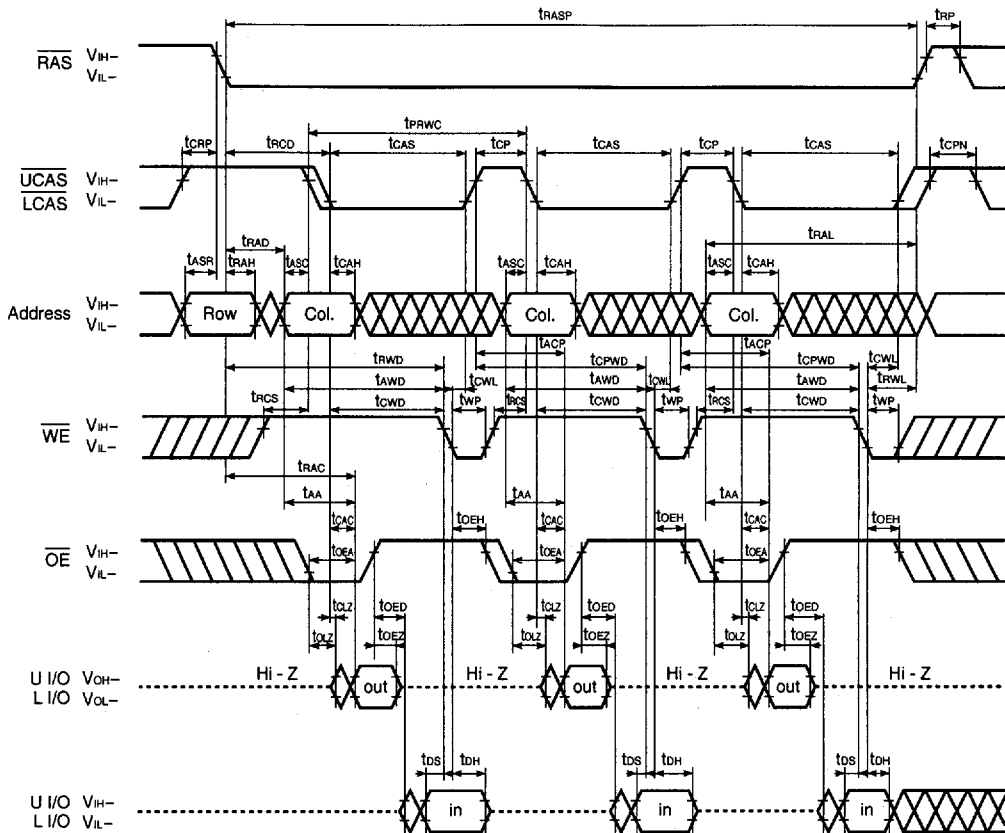
PACKAGE OUTLINES
μPD2114LC



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

Fast Page Mode Read Modify Write Cycle

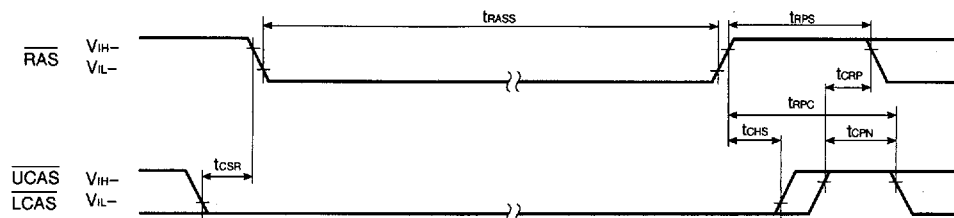


Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

[illegible]

- 764

CAS Before RAS Self Refresh Cycle (Only for the μ PD42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S18160: 1,024 times within a 16 ms interval

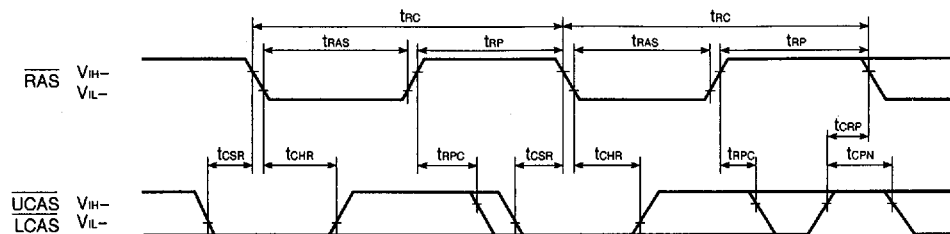
(3) If $t_{RASS} (MIN.)$ is not satisfied at the beginning of CAS before RAS self refresh cycles ($t_{RAS} < 100 \mu s$), CAS before RAS refresh cycles will be executed one time.

If $10 \mu s < t_{RAS} < 100 \mu s$, RAS precharge time for CAS before RAS self refresh (t_{RPS}) is applied. And refresh cycles as follows should be met.

μ PD42S18160: 1,024 times within a 128 ms interval

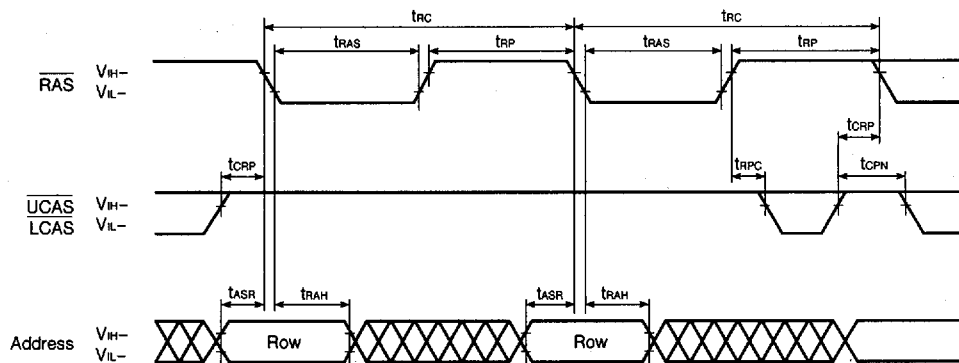
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

RAS Only Refresh Cycle



Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)

